

SYNC separator IC with AFC

BA7062F

The BA7062F separates the synchronization signals from a video signal and outputs the horizontal and vertical synchronization signals (H_D and V_D), and the composite synchronization signal (Sync-out).

The H_D and V_D pulse widths are different.

●Applications

TVs and VCRs

●Features

- 1) Built-in AFC circuit.
- 2) Low power dissipation (approx. 21mW).
- 3) Low external parts count.
- 4) SOP 8-pin package.
- 5) Horizontal free-run frequency does not require adjustment.

●Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

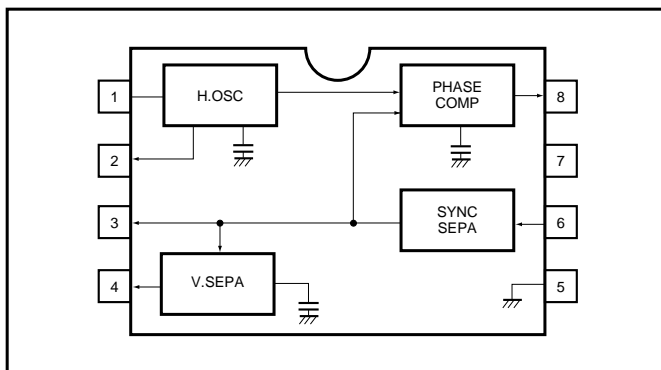
Parameter	Symbol	Limits	Unit
Power supply voltage	$V_{CC \text{ Max.}}$	8.0	V
Power dissipation	P_d	350*	mW
Operating temperature	T_{opr}	- 20 ~ + 75	$^\circ\text{C}$
Storage temperature	T_{stg}	- 55 ~ + 125	$^\circ\text{C}$

* When mounted on a 50mm × 50mm PCB, reduced by 3.5mW for each increase in T_a of 1 $^\circ\text{C}$ over 25 $^\circ\text{C}$.

●Recommended operating conditions ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{CC}	4.5	—	5.5	V

●Block diagram



●Pin descriptions

Pin No.	Function
1	Horizontal oscillator resistor
2	Hb output
3	SYNC output (open collector)
4	Vb output
5	GND
6	Video input
7	Power supply
8	Phase comparator output

●Input / output circuits

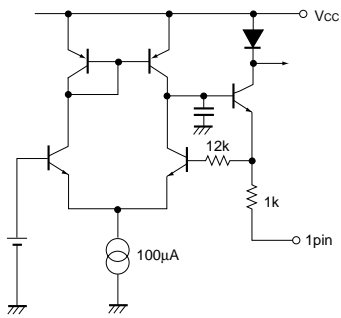


Fig. 1

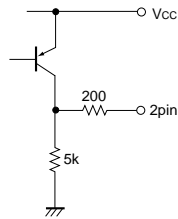


Fig. 2

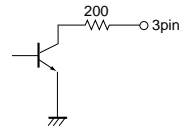


Fig. 3

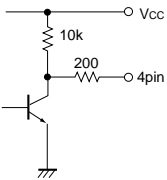


Fig. 4

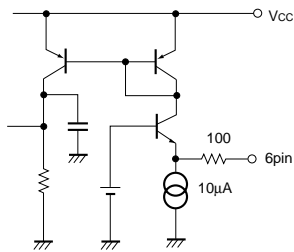


Fig. 5

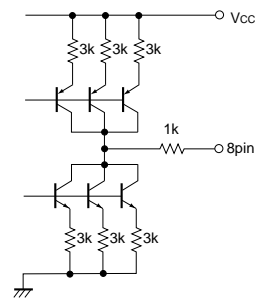


Fig. 6

● V_{IN} , H_D , and V_D timing charts

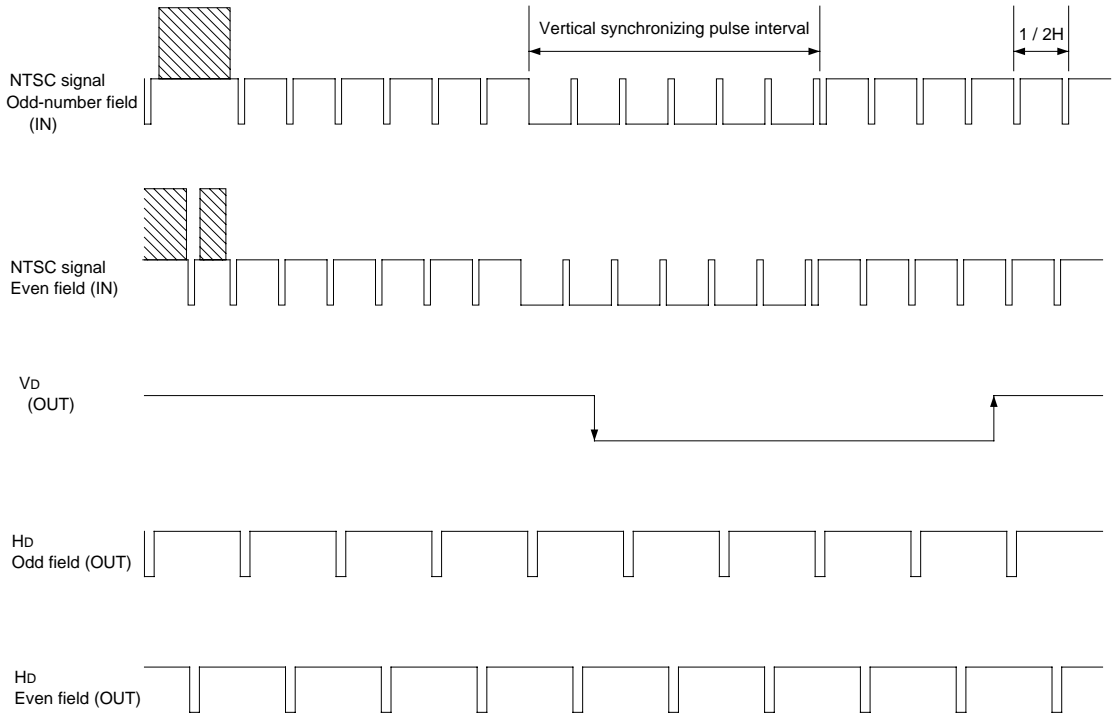
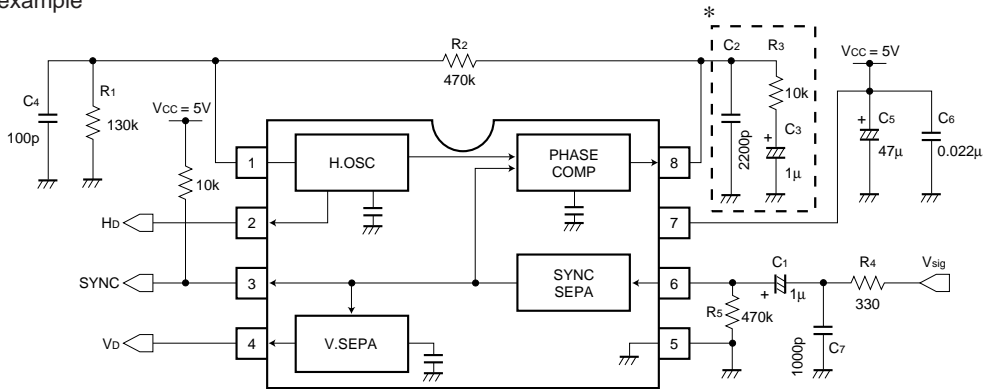


Fig. 8

- (1) The rise and fall positions for V_D are basically the same for both odd and even fields.
- (2) H_D shifts by $1/2H$ during the odd and even field interval.

●Application example



* By configuring the circuit enclosed in the dotted line to that in the diagram on the right, you can decrease the lock-in time and increase the capture range.

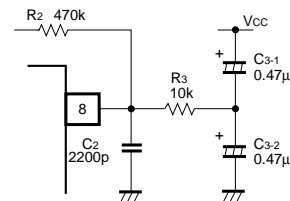


Fig. 9

• When SYNC SEPA output only is used. H_b and V_D unused.

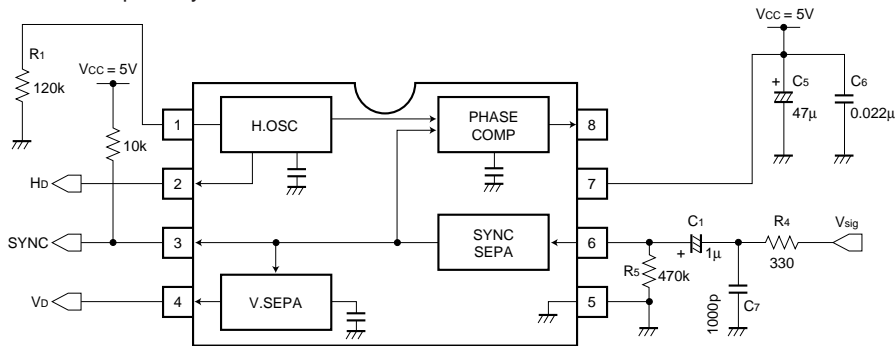


Fig. 10

- (1) Connect pin 1 to GND via a 120kΩ (approx.) resistor. Leave pins 2, 4 and 8 open.
- (2) SYNC output polarity (pin 3) is positive.
- (3) The delay time for rising edge of the SYNC output (pin 3) with respect to the falling edge of Sync for the V_{sig} input signal (pin 6) is 850ns (reference value).
- (4) The delay time for falling edge of the SYNC output (pin 3) with respect to the rising edge of Sync for the V_{sig} input signal (pin 6) is 450ns (reference value).

●Attached components

Resistor R₁ should have a tolerance of ± 2%, and a temperature coefficient of 100ppm or lower.

● Electrical characteristic curves

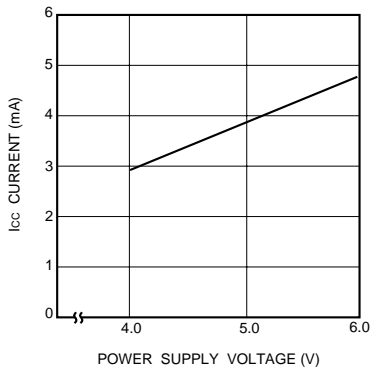


Fig. 11 Quiescent current vs. power supply voltage

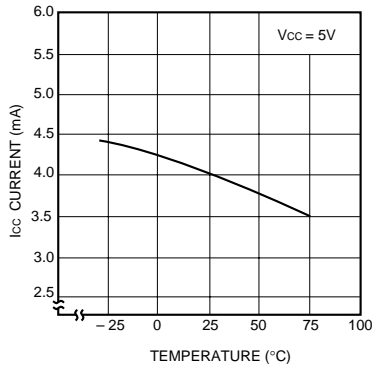


Fig. 12 Quiescent current vs. temperature

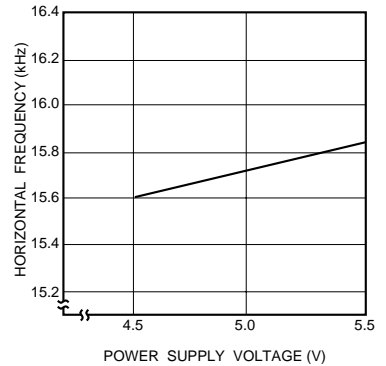


Fig. 13 Horizontal free-running frequency vs. power supply voltage

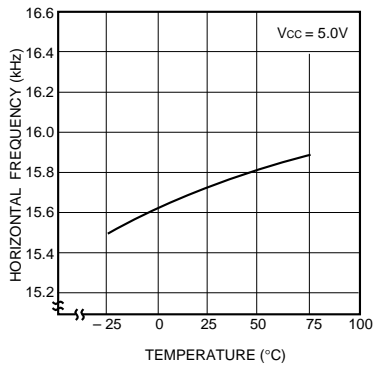


Fig. 14 Horizontal free-running frequency vs. temperature

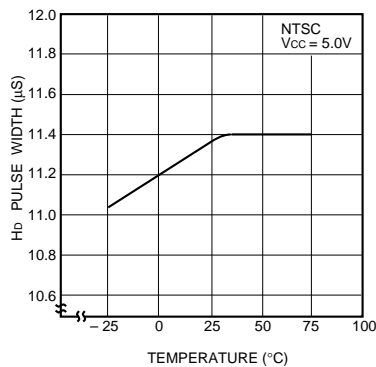


Fig. 15 H_b pulse width vs. temperature

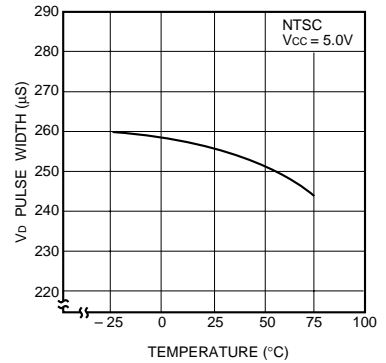


Fig. 16 V_d pulse width vs. temperature

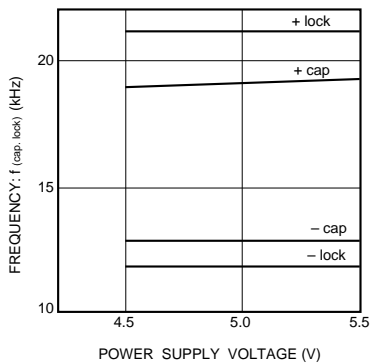


Fig. 17 Capture range / lock range vs. power supply voltage

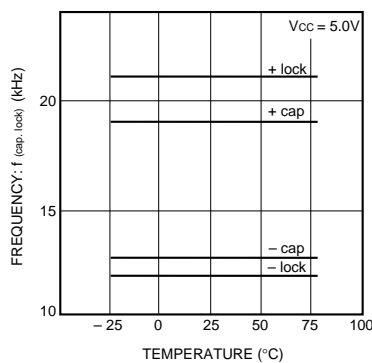


Fig. 18 Capture range / lock range vs. temperature

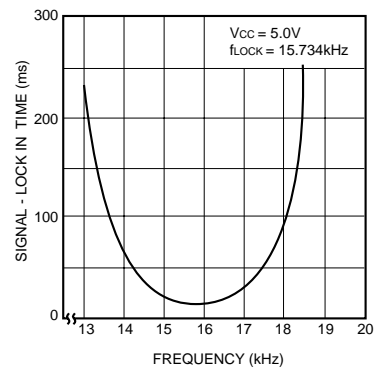


Fig. 19 Time from no signal to pull in

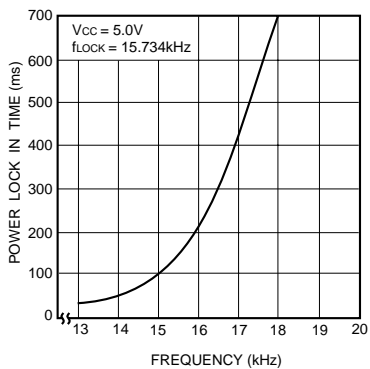
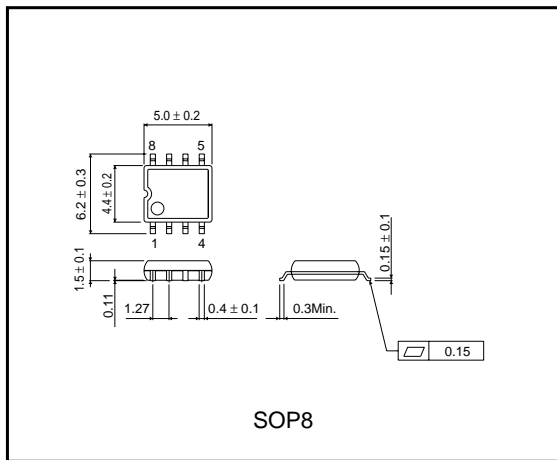


Fig. 20 Time from power on to pull in

● Operation notes

- Make the ground line as thick as possible.
- Keep power supply noise to a minimum.

● External dimensions (Units: mm)





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