GENERAL DESCRIPTION

The samsung analog front end(AFE) for CCD/CIS image signal is an integrated analog signal processor for color image signal.
The AFE converts CCD/CIS output signal to digital data. The AFE includes three-channel CDS(Correlated Double Sampling) circuit, PGA(Programmable Gain Amplifier), and 12-bit analog to digital converter with reference generator.
A parallel data bus provides a simple interface to 8-bit microcontroller.

APPLICATIONS

- Color and B/W Scanner
- Digital Copiers
- Facsimile
- General Purpose CCD/CIS imager

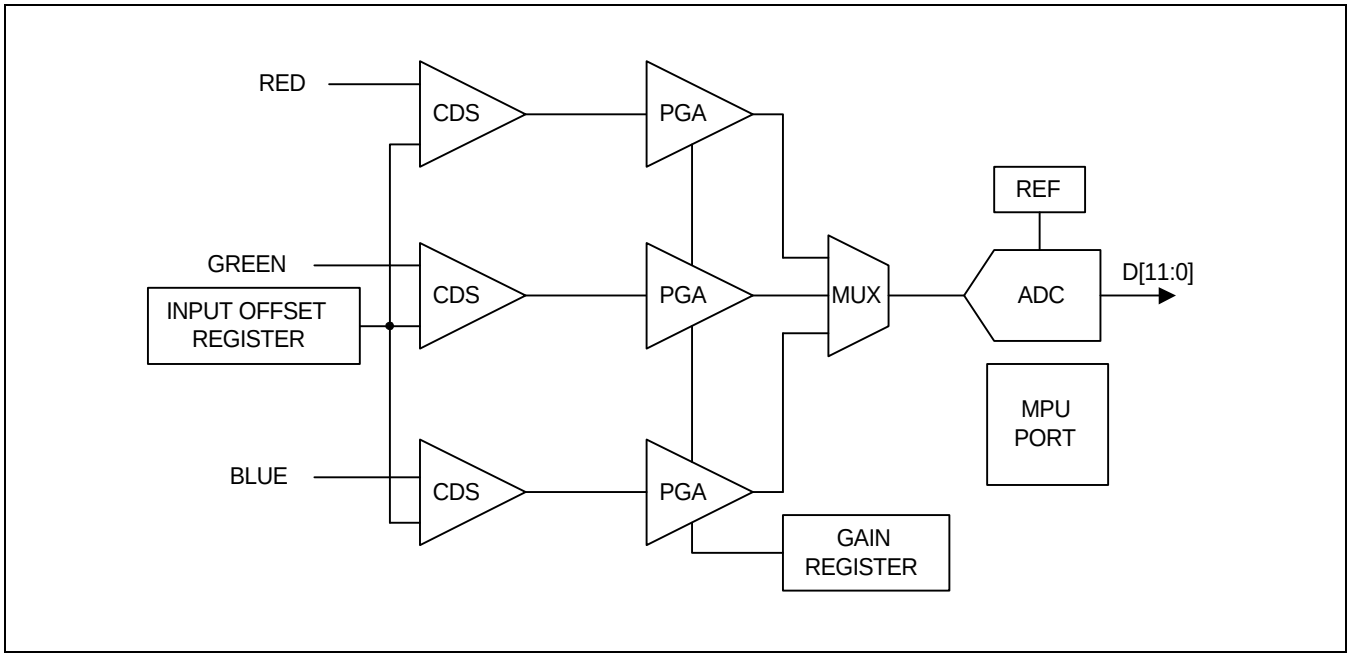
FETURES

- 12-bit 6MSPS A/D Converter
- Integrated Triple Correlated Double Sampler
- 3-Channel 2 MSPS Color Mode
- Analog Programmble Gain Amplifier
- Internal Voltage Reference
- Wide clamp level controllability for CIS sensor
- No Missing Code Guaranteed
- Microcontroller-Compatible Control Interface
- Operation by Single 5V Supply
- CMOS Low Power Dissipation

KEY SPECIFICATION

- Resolution: 12-bit
- Conversion Rate: 6 MHz(2 MHz*3)
- Supply Voltage: 5 V ± 5%
- Power Dissipation: 375 mW(Typical)

FUNCTIONAL BLOCK DIAGRAM



Ver 2.0 (Apr. 2002)

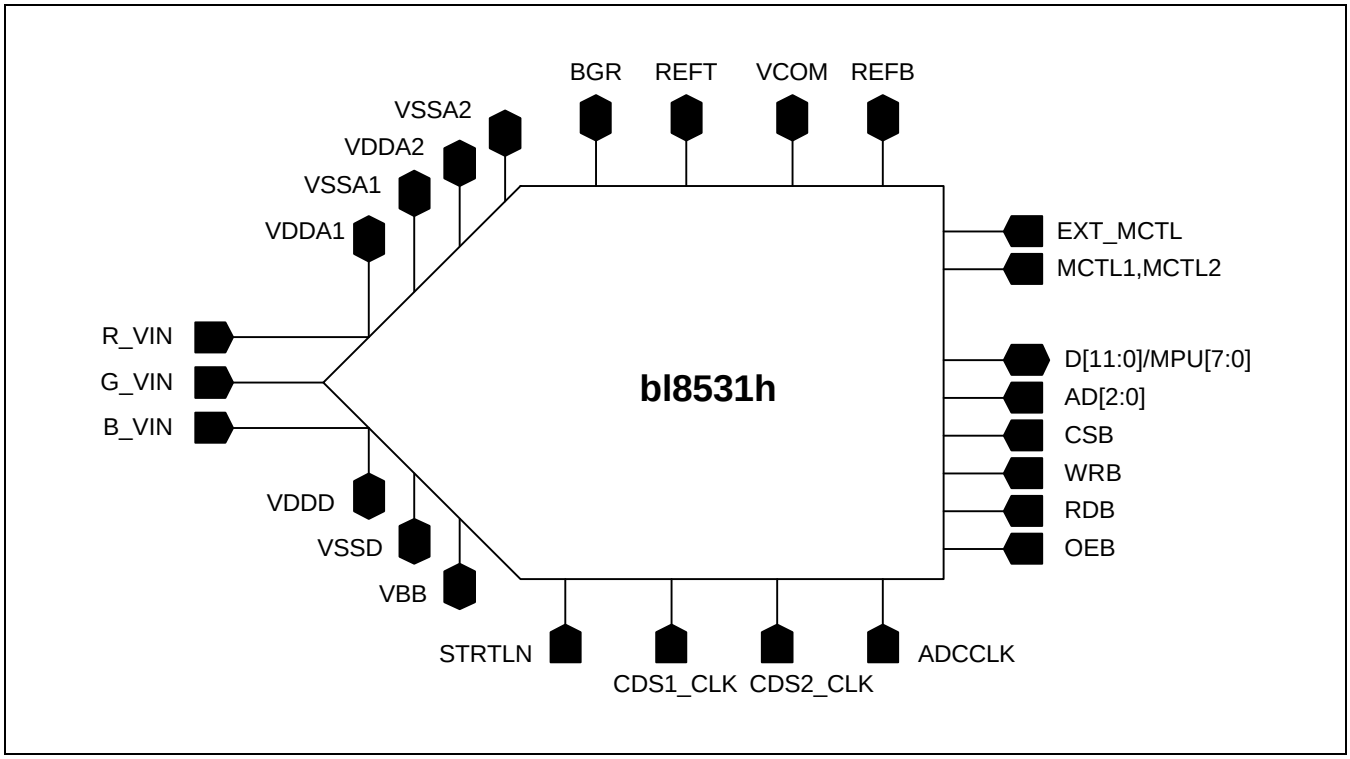
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VDDA1	AP	vdda	5 V Analog Supply
VSSA1	AG	vssa	Analog Ground
VDDA2	AP	vdda	5 V Analog Supply(for ADC)
VSSA2	AG	vssa	Analog Ground(for ADC)
VBB	AG	vbba	Substarte Ground
VDDD	DP	vddd	5 V Digital Supply
VSSD	DG	vssd	Digital Ground
REFT	AB	piar50_bb	Reference Decoupling
REFB	AB	piar50_bb	Reference Decoupling
VCOM	AB	piar50_bb	Analog Common Voltage
BGR	AB	piar50_bb	Bandgap Refernce Voltage
R_VIN	AI	piar10_bb	Analog Input; Red
G_VIN	AI	piar10_bb	Analog Input; Green
B_VIN	AI	piar10_bb	Analog Input; Blue
STRTLN	DI	picc_bb	STRTLN indicates beginning of line
CDS1_CLK	DI	picc_bb	CDS Reset Clock Pulse Input
CDS2_CLK	DI	picc_bb	CDS Data Clock Pulse Input
ADCCLK	DI	picc_bb	A/D Converter Sample Clock Input
CSB	DI	picc_bb	Chip Select; Active Low
WRB	DI	picc_bb	Write Strobe; Active Low
RDB	DI	picc_bb	Read Strobe; Active Low
OEB	DI	picc_bb	Output Enable; Active Low
D[11:0]/MPU[7:0]	DB	pia_bb	Data Inputs/Outputs
AD[2:0]	DI	picc_bb	Register Select
MCTL1, MCTL2	DI	picc_bb	Channel Select in External MUX Control
EXT_MCTL	DI	picc_bb	External MUX Control; Active Low

I/O TYPE ABBR.

- AI : Analog Input
- AO : Analog Output
- AP : Analog Power
- DP : Digital Power
- AB : Analog Bidirectional Port
- DI : Digital Input
- DO : Analog Output
- AG : Analog Ground
- DG : Digital Ground
- DB : Digital Bidirectional Port

CORE PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Charateritics	Symbol	Value	Units
Supply Voltage	VDD	6.5	V
Analog Input Voltage	AIN	VSS to VDD	V
Digital Input Voltage	CLK	VSS to VDD	V
Digital Output Voltage	$V_{OH, VOL}$	VSS to VDD	V
Reference Voltage	VRT/VRB	VSS to VDD	V
Storage Temperature Range	Tstg	-45 to 150	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

ANALOG SPECIFICATIONS

(VDDA = 5V, VDDD = 5V, ADCCLK = 6MHz, CDS1_CLK = 2MHz, CDS2_CLK = 2MHz, PGA Gain = 1 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Comment
Resolution		12			Bits	
Signal-to-Noise & Distortion Ratio	SNDR		60		dB	
Conversion Rate 3-Channel with CDS 1-Channel with CDS			 6 6		 MSPS MSPS	
Differential Nonlinearity	DNL		± 1		LSB	
Integral Nonlinearity	INL		± 2		LSB	
Unipolar Offset Error				1.0	%FSR	
Gain Error				2.0	%FSR	
Anlog Input Full-Scale Input Input Capacitance Reference Top Reference Bottom		 0.06	 8 3.5 1.5	 4.0	 Vp-p Pf V V	
Power Supply Analog Voltage Digital Voltage Analog Current Digital Current	 VDDA VDDD IDDA IDDD		 5 5 65 10		 V V mA mA	5V ±5% 5V ±5%
Power Consumption			375		mW	
Temperature Range		0		70	°C	

DIGITAL SPECIFICATIONS

(VDDA = 5V, VDDD = 5V, ADCCLK = 6MHz, CDS1_CLK = 2MHz, CDS2_CLK = 2MHz, CL = 20pF unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Comment
High Level Input Voltage	V_{IH}	3.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}		10		mA	
Low Level Input Current	I_{IL}		10		mA	
High Level Output Voltage	V_{OH}	4.5			V	I_{OH} = 0.5mA
Low Level Output Voltage	V_{OL}			0.5	V	I_{OL} = -0.5mA

TIMING SPECIFICATIONS

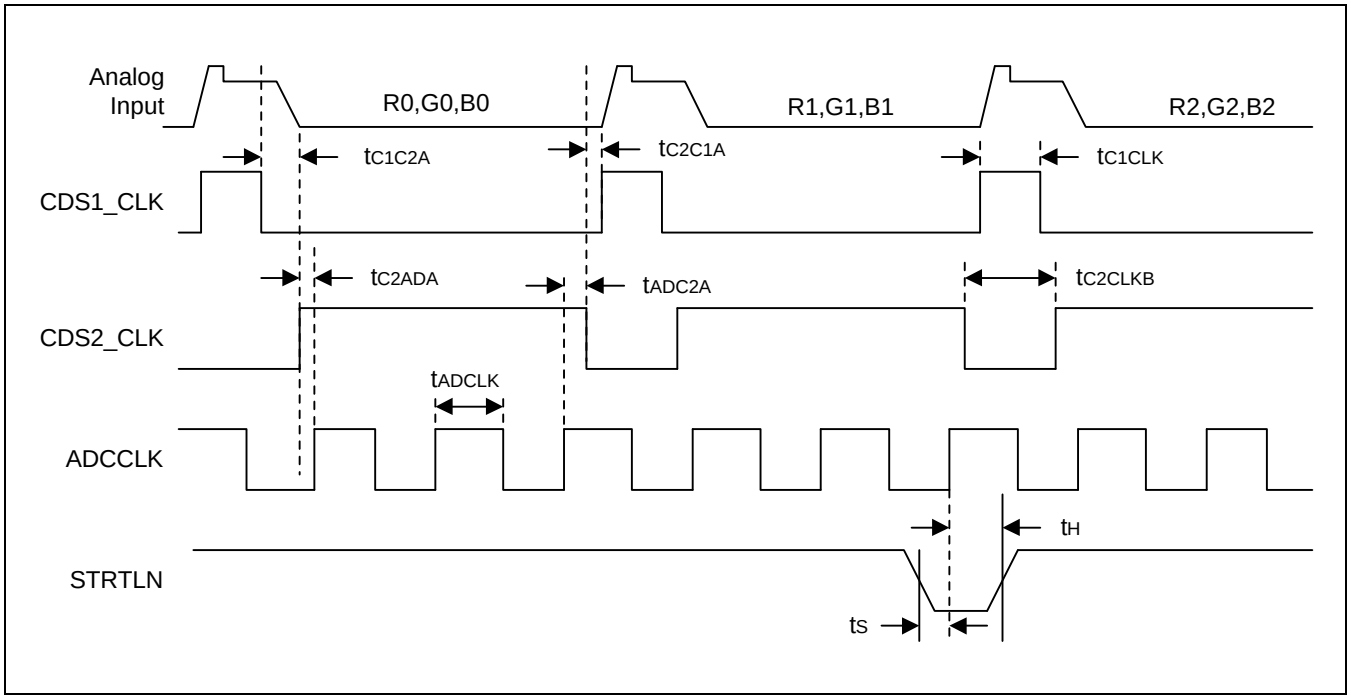
(VDDA = 5V, VDDD = 5V unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
3-Channel Conversion Rate		500			ns
1-Channel Conversion Rate		166			ns
CDSCLK1 Pulse Width	t_{C1CLK}	60			ns
CDSCLK2 Pulse Width	t_{C2CLK}	70			ns
CDSCLK2B Pulse Width	t_{C2CLKB}	70			ns
CDSCLK1 Falling to CDSCLK2 Rising	t_{C1C2A}	5			ns
CDSCLK2 Falling to CDSCLK1 Rising	t_{C2C1A}	5			ns
ADCCLK Pulse Width	t_{ADCLK}	70			ns
CDSCLK2 Rising to ADCCLK Rising	t_{C2ADA}	70			ns
CDSCLK2 Falling to ADCCLK Falling	t_{C2ADB}	5			ns
ADCCLK Rising to CDS2CLK Falling	t_{ADC2A}	5			ns
STRTLN Rising, Falling Setup & Hold	t_S, t_H	15			ns
ADC Output Delay	t_{ADDT}	20			ns
Register Address Setup Time	t_{AS}	15			ns
Register Address Hold Time	t_{AH}	15			ns
Data Hold Time	t_{DH}	15			ns
Register Chip Select Setup Time	t_{CSS}	15			ns
Register Chip Select Hold Time	t_{CSH}	15			ns
Register Read Pulse Width	t_{PWR}	50			ns
Write Pulse Width	t_{PWW}	25			ns
Register Read To Data Valid	t_{DD}	40			ns
Output Enable High to Tri-State	t_{HZ}	10			ns
Tri-State to Data Valid	t_{DEV}	15			ns
Aperture Delay	t_{AD}	2			ns
Latency for 1 Channel mode			4		ADCCLK Cycles

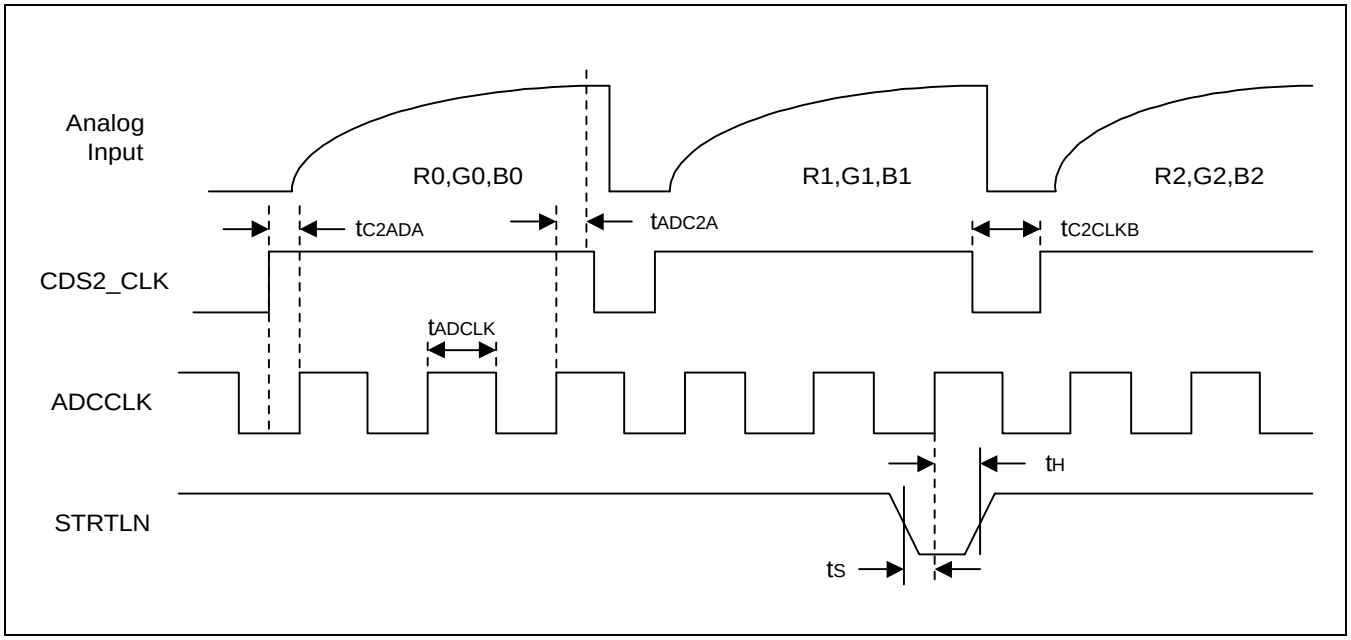
* Aperture delay is a timing measurement between the sampling clocks and CDS. It is measured from the falling edge of the CDS2_CLK input to when the input signal is held for data conversion

TIMING DIAGRAM

3-Channel CDS Mode

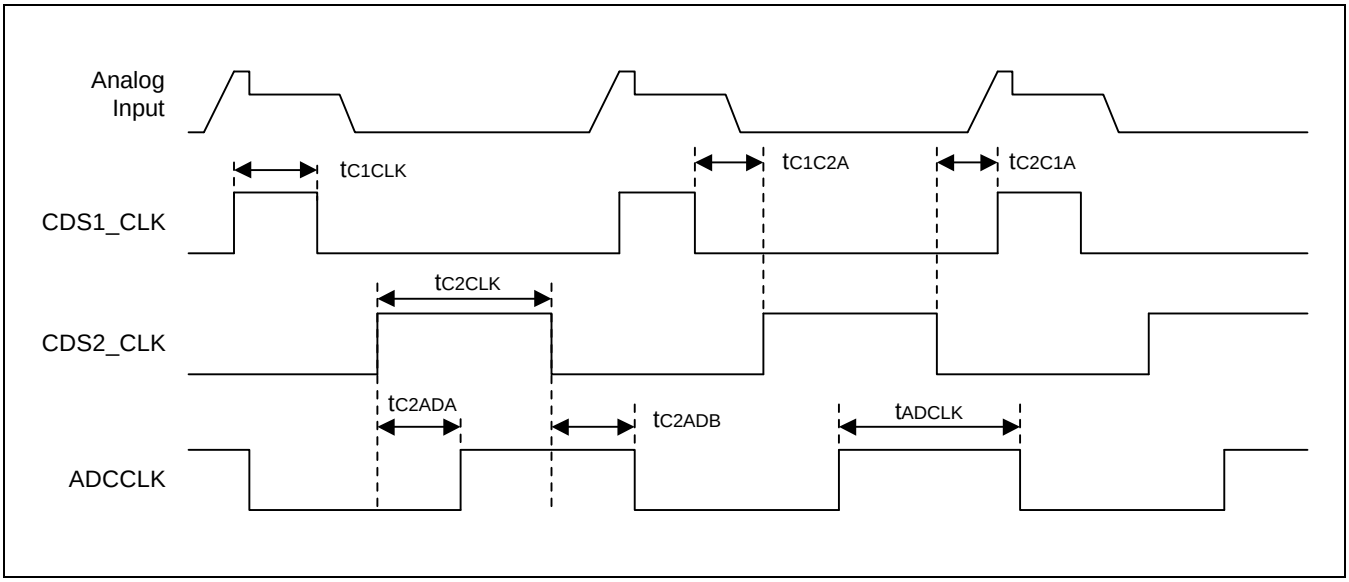


3-Channel SHA Mode



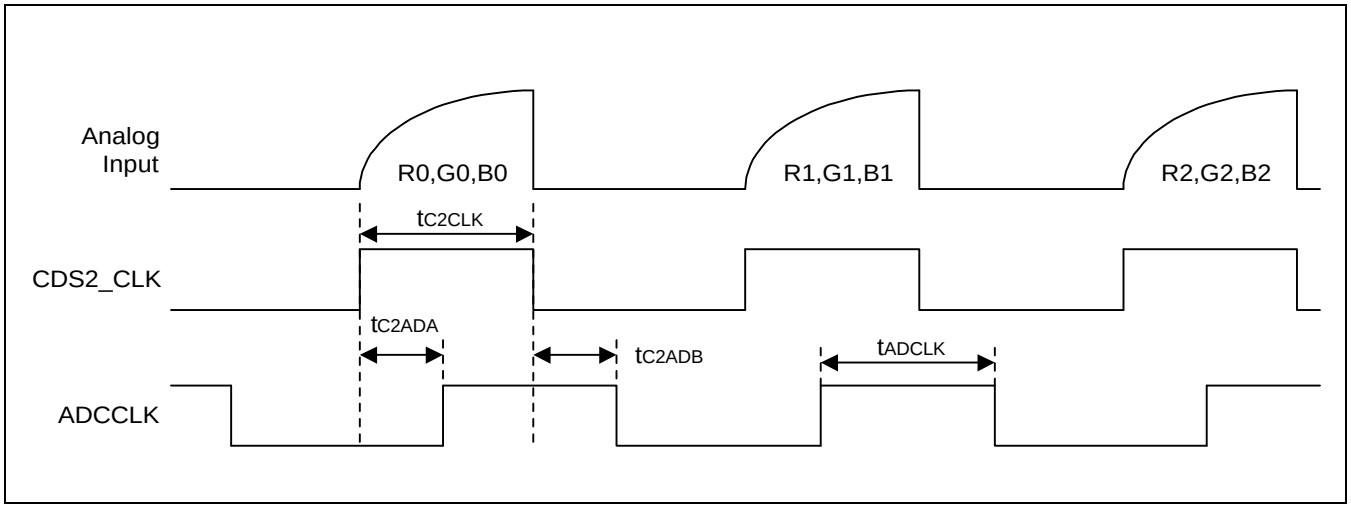
SAMSUNG ELECTRONICS

1-Channel CDS Mode

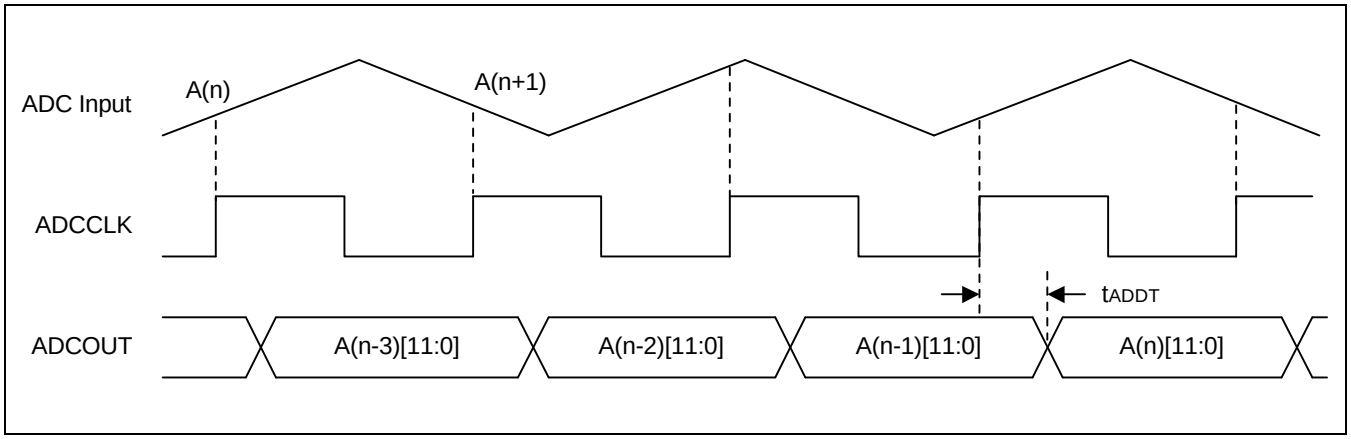


TIMING DIGRAM

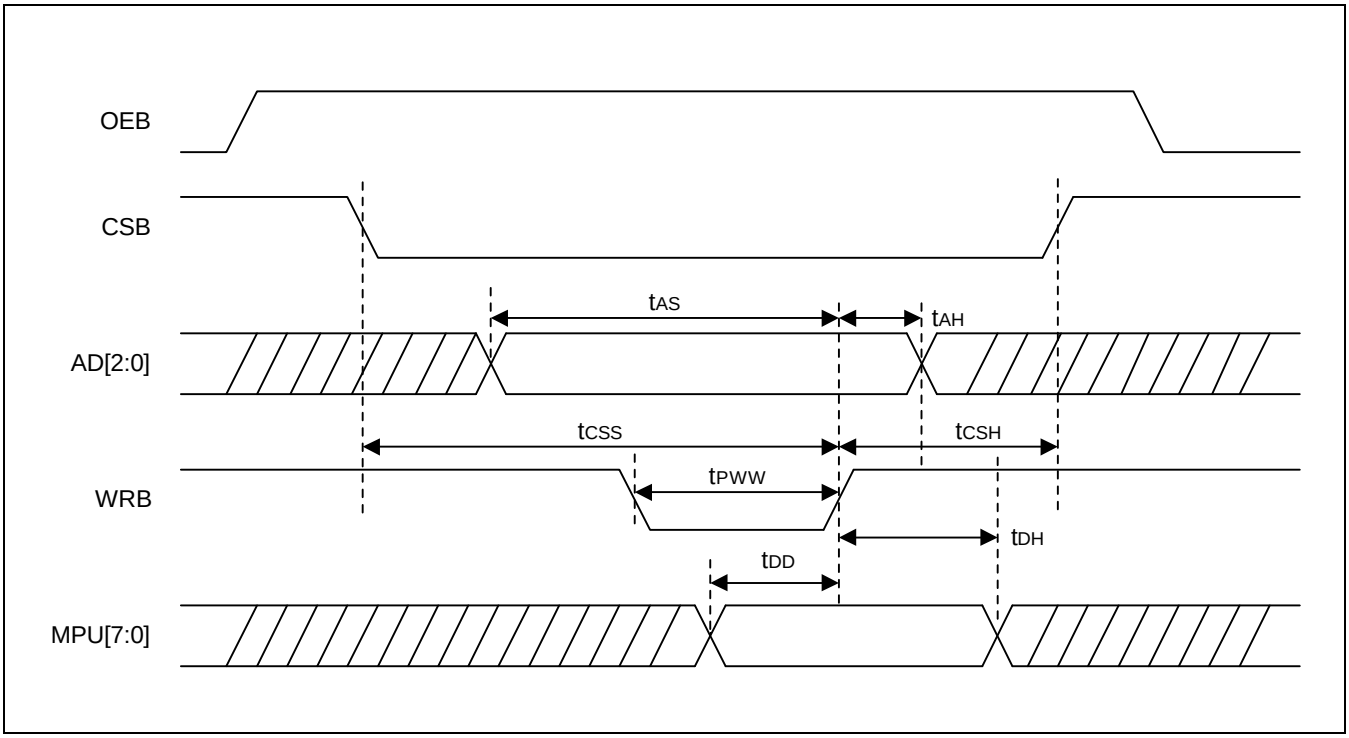
1-Channel SHA Mode



ADC Timing

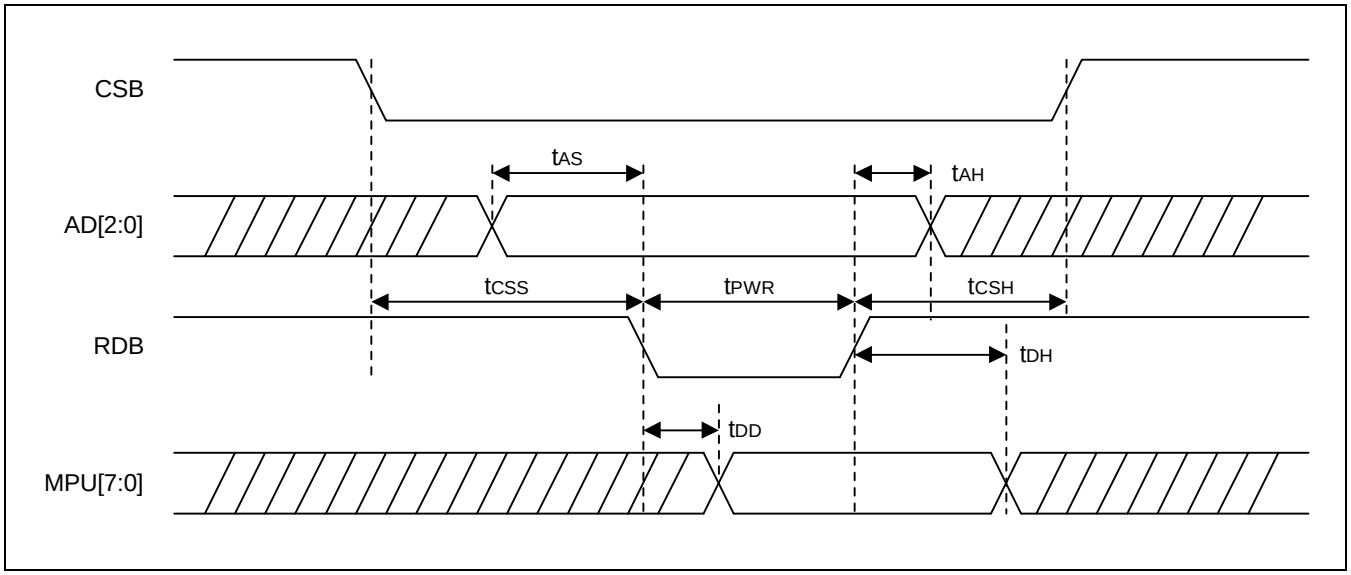


Write Timing



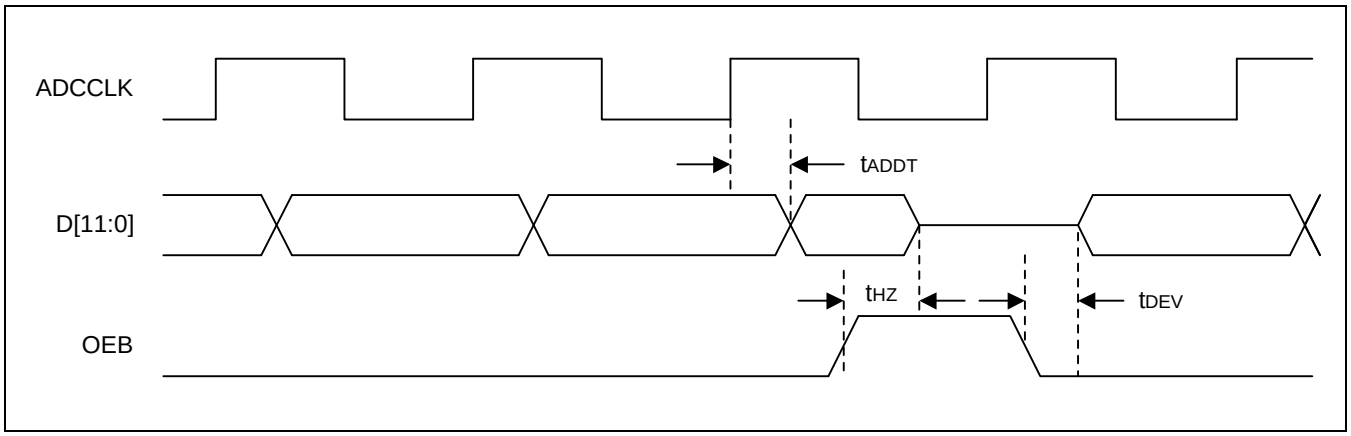
TIMING DIGRAM

Read (1) Timing



'Read(1)' means microcontroller reads MPU[7:0]
CSB should keep 'High' to read.

Read (2) Timing



FUNCTIONAL DESCRIPTION

1) 3-Channel Operation with CDS

This mode enables simultaneous sampling of a triple output CCD. The CCD waveforms are ac coupled to the VINR, VING and VINB pins where they are automatically biased at an appropriate voltage using the on-chip clamp. The internal CDSs take two samples of the incoming pixel data; the first samples are taken during the reset time while the second samples are taken during data portion of the input pixels. When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the multiplexer is switched to red channel.

2) 3-Channel SHA Operation

This mode enables simultaneous sampling of a triple output CIS or something like that. The CDS functions are replaced with the sample and hold amplifiers. The input waveforms are either dc coupled or dc restored to the VINR, VING and VINB pins. The input reference voltage in this mode will be defined by clamp level control register.

When STRTLN is low, the internal circuitry is reset on the next rising edge of ADCCLK; the multiplexer is switched to red channel.

3) 1-Channel Operation with CDS

This mode enables single channel or monochrome sampling. The CCD waveforms are ac coupled to the analog input pin where they are automatically biased at an appropriate voltage using the on-chip clamp.
Bit2 and bit3 in configuration register select the desired input among red, green and blue.

4) 1-Channel SHA Operation

This mode enables single-channel or monochrome sampling. The CDS function is replaced with the sample and hold amplifier.

The input waveforms are either dc coupled or dc restored to the analog input pin. The input reference voltage in this mode will be defined by clamp level control register.
Bit2 and bit2 in configuration register select the desired input among red, green and blue.

MAIN BLOCK DESCRIPTION

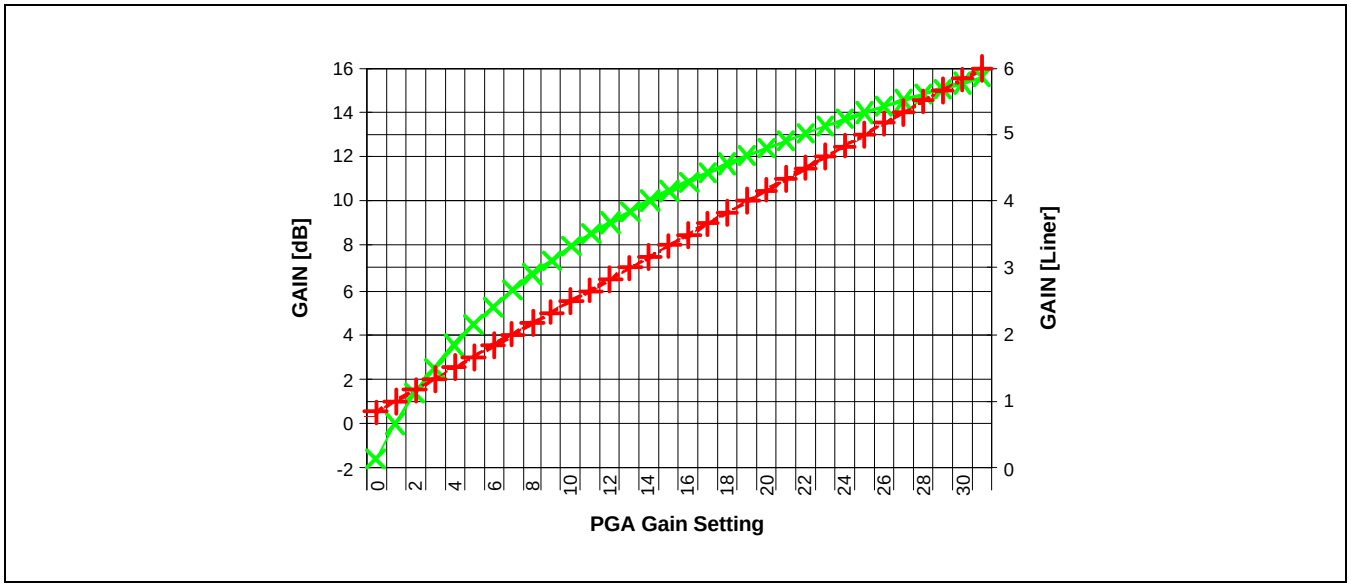
1) Programmable Gain Amplifier

The analog programmable gain can accommodate a wide range of input voltage spans. The transfer function of the PGA is as follows.

$$H(X) = 1/6*X + 5/6,$$

where the range of X is 0 to 31.

Thus, the minimum gain value is equal to 5/6, and the maximum gain value is equal to 6. The transfer function has linearity in linear scale. The overall gain is equal to analog gain multiplied by digital gain. So, the multiplier should be required in back end of AFE.



There is a gain boosting block before 12-bit ADC, which can muliply PGA's output signal by 1.5 (3.5dB) or pass it. This is controled by gain mode of configuration register.

BLOCK DIAGRAM

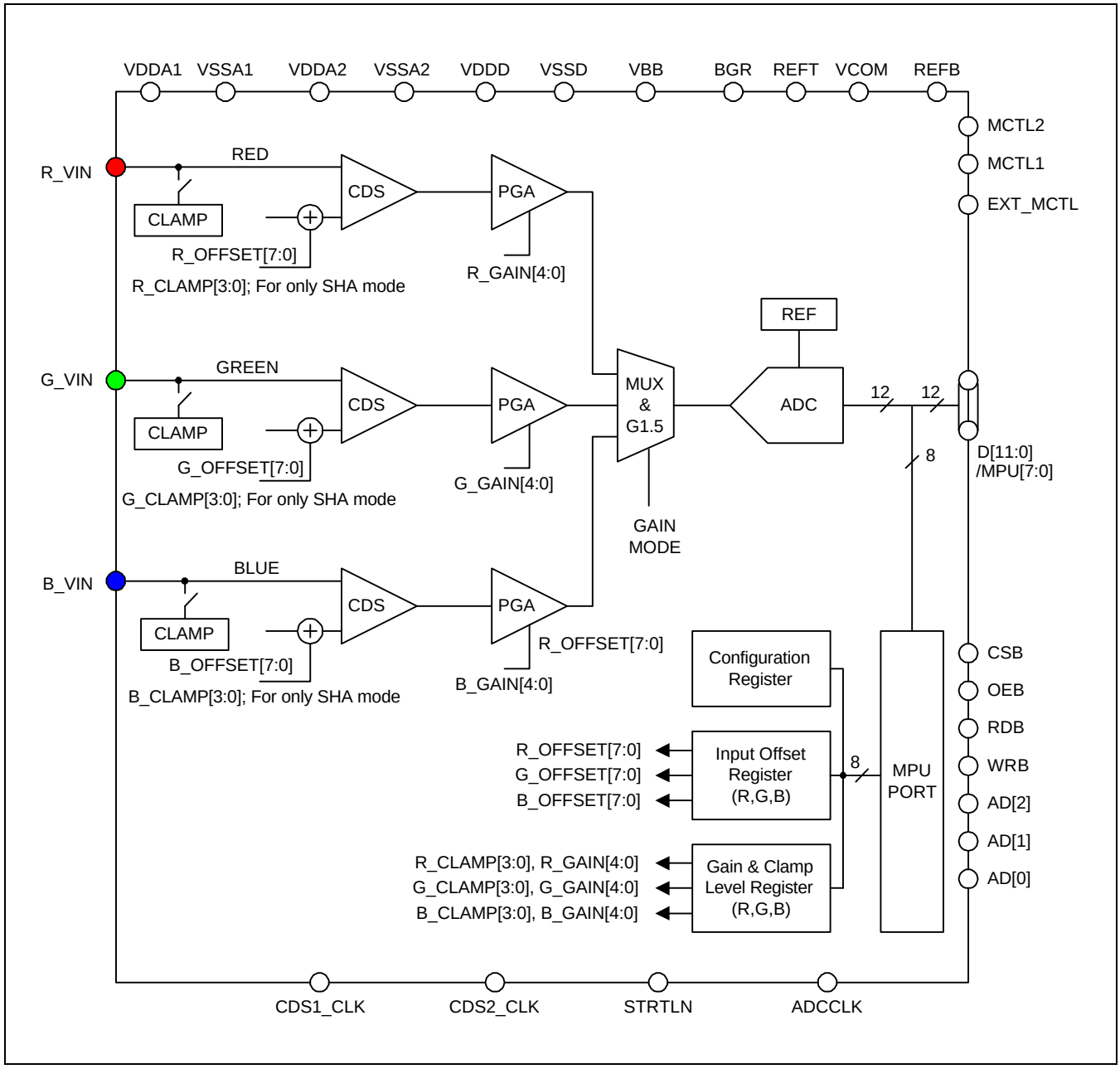


Table: MPU Port Map Format

A2	A1	A0	Register
0	0	0	Configuration Register
0	0	1	Input Offset register
0	1	0	PGA Gain Control Register
0	1	1	CIS Clamp Control Register
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

2) Register Overview

The MPU port map is accessed through pins A0, A1 and A2. See MPU port map format.(previous page)

Configuration Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clamp mode select1	Clamp mode select0	PGA Gain mode	External Reference	Color1	Color0	Single Channel	CDS Enable

Single Channel Color Pointer		
Bit3	Bit2	Color
0	0	Red
0	1	Green
1	0	Blue
1	1	Reserved

Clamp Mode Selection		
Bit7	Bit6	Clamp Mode
0	0	Line Clamp
0	1	Pixel Clamp
1	0	No Clamp
1	1	Reserved

Input Offset Register

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

PGA Gain Control Register

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	PGA4	PGA3	PGA2	PGA1	PGA0

CIS Clamp Control Register

MSB LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	CCC3	CCC2	CCC1	CCC0

* CCCn: CIS Clamp Control n

MULTIPLEXER CONTROL MODE

EXT_MCTL = "LOW"		
MCTL2	MCTL1	Color
0	0	Red
0	1	Green
1	0	Blue
1	1	Reserved

OVERRALL TRANSFER FUNCTION

The overall transfer function can be calculated as follows.

if gain mode = 0,
ADC_{out} = [(Vin+Input_Offset)* PGA_Gain]/(2*REF)*4096,

if gain mode = 1,
ADC_{out} = [(Vin+Input_Offset)* PGA_Gain * 1.5]/(2*REF)*4096,

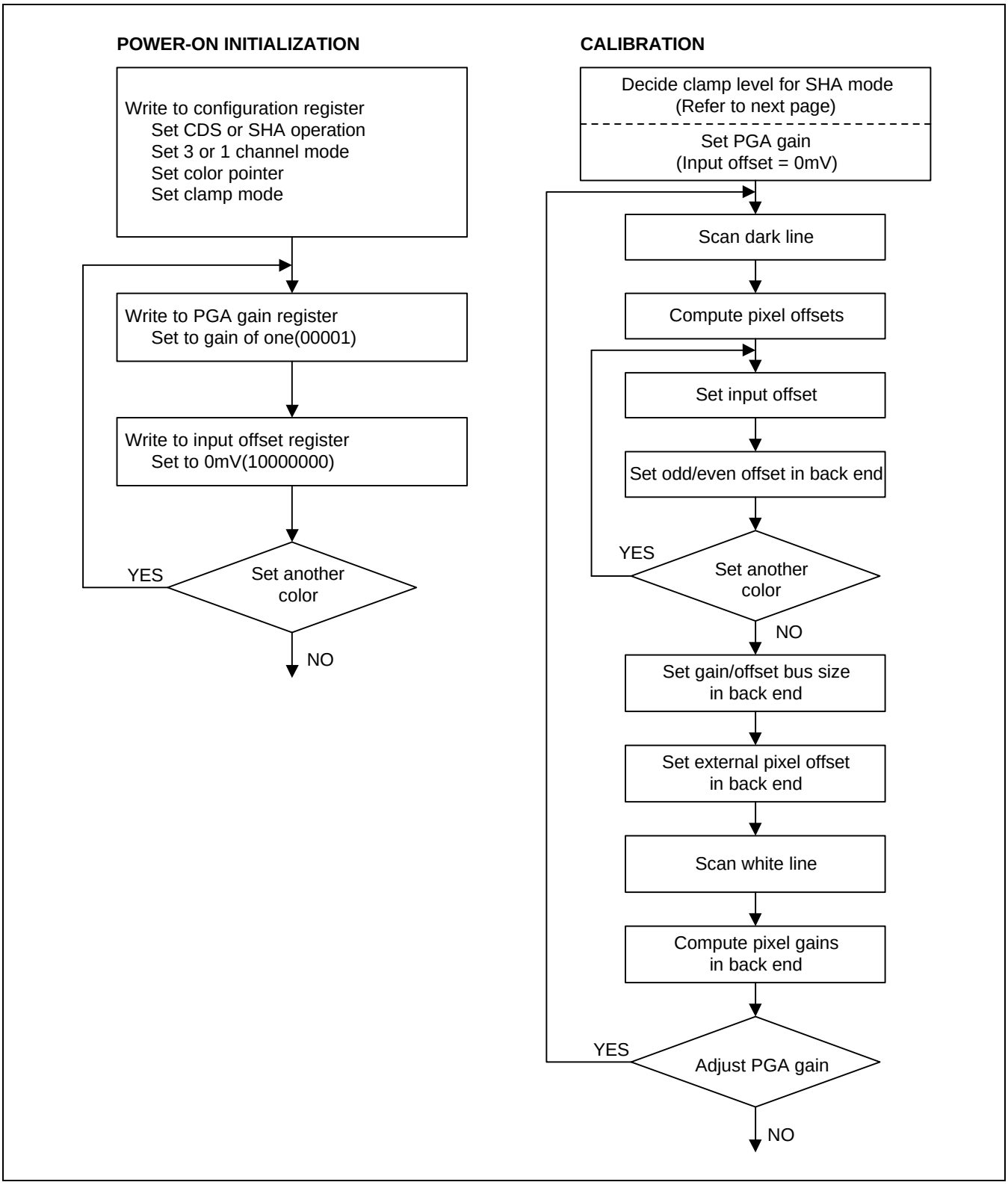
where REF is equal to (REFT-REFB) and Input _Offset means the DAC value of the input offset register. The analog offset range of the input offset register is varied between 150mV and -150 mV. The 8-bit data format for the input offset register is straight binary coding. Thus, an all 'zeros' data word corresponds to -150 mV. An all 'ones' data word corresponds to 150 mV.
To maximize the dynamic range of the ADC input, it is necessary to program the input offset register code to move the ADC code corresponding to the black level towards 'zero'.
In case of processing CIS signal, 4-bit of the gain & clamp control register are allocated to control CIS clamp level. Like the input offset register, the 4-bit data format is straight binary coding. An all 'zeros' data word corresponds to 0.1 V and an all 'ones' data word corresponds to 1.5 V.

INPUT COUPLING CAPACITOR

Because of the DC offset present at the output of CCD, some kind of DC restoration is required. In case of CDS enable mode, to simplify input level shifting, a DC decoupling capacitor is used in conjuction with the internal input circuitry.

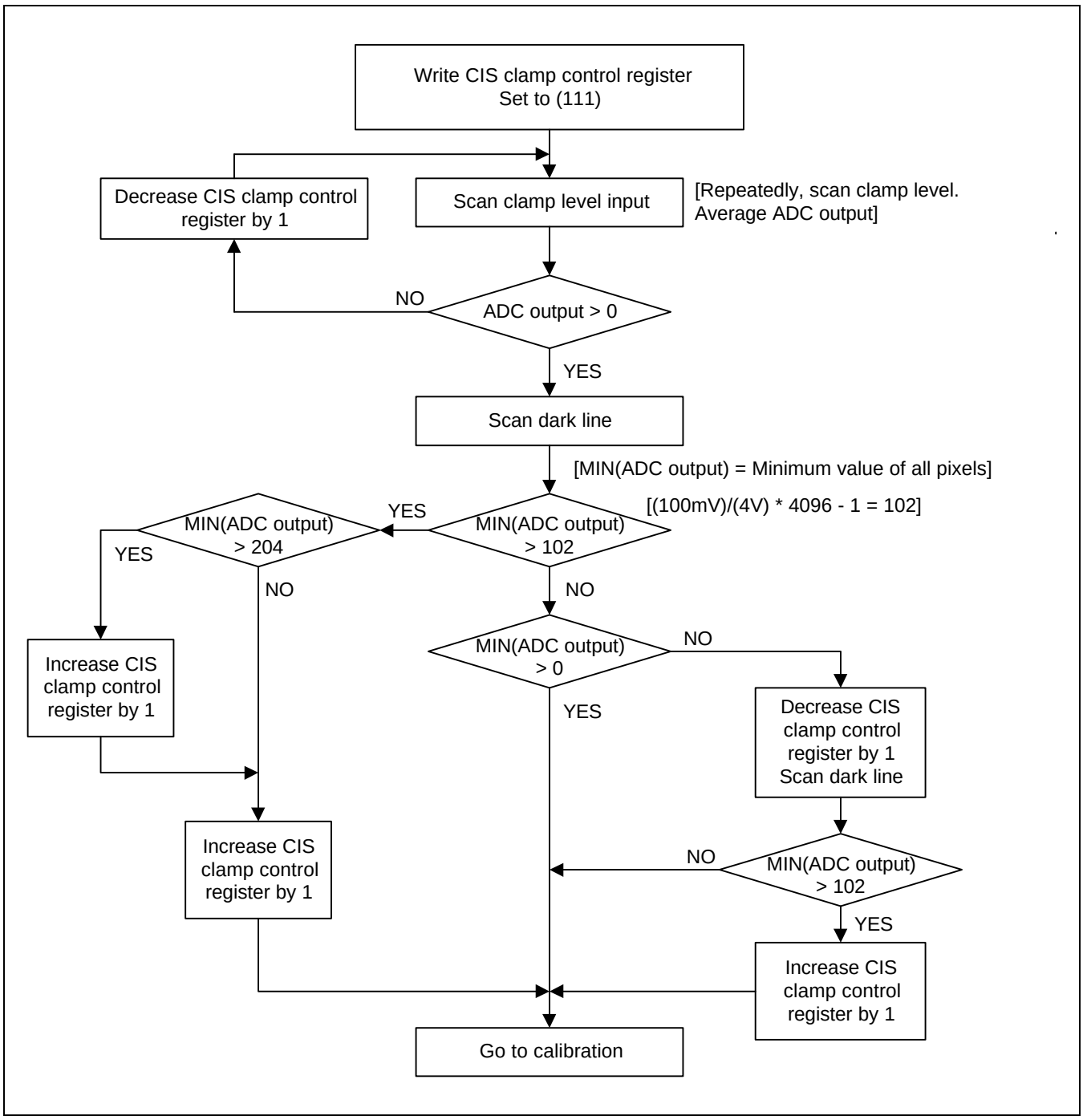
The capacitor charging or discharging depends on the clamping time, the analog input resistance of the AFE and the output resistance of the circuit driving the coupling capacitor.

The clamping time is typically (n*T), where n is the number of periods CDSCLK1 is asserted and T is the period of assertion. CDSCLK2 should not be asserted during clamping time. And, STRTLN must be low in line clamp mode for clamping operation. The analog input resistance of the AFE is equal to 1 kΩ. The recommended input coupling capacitor is more than 0.01uF. Thus, to extend the clamping time, the time a transport motor moves the scanner carriage can be available, for example.

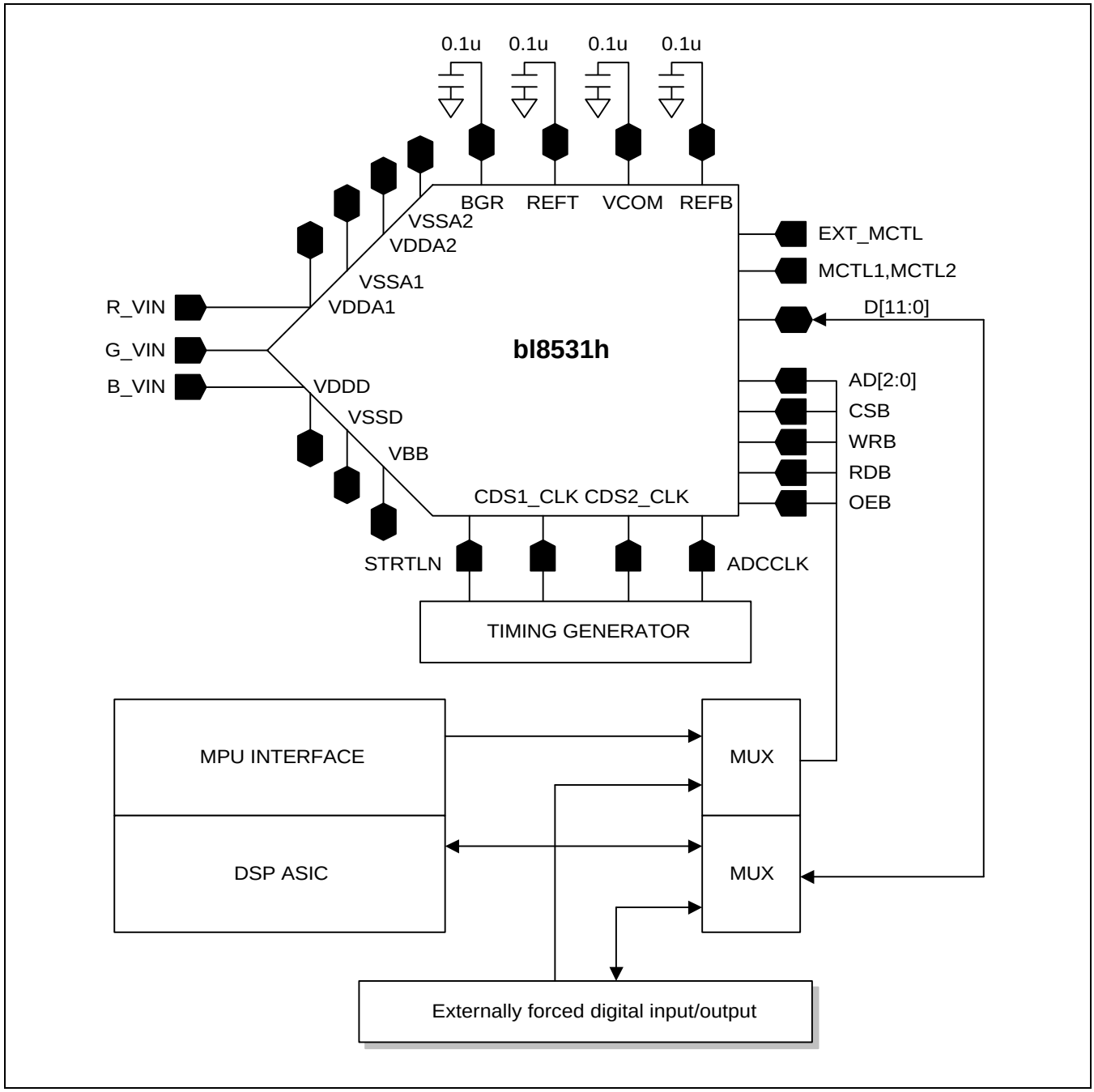

POWER-ON INITIALIZATION
Write to configuration register
Set CDS or SHA operation
Set 3 or 1 channel mode
Set color pointer
Set clamp mode
Write to PGA gain register
Set to gain of one(00001)
Write to input offset register
Set to 0mV(10000000)
YES
Set another color
NO
CALIBRATION
Decide clamp level for SHA mode
(Refer to next page)
Set PGA gain
(Input offset = 0mV)
Scan dark line
Compute pixel offsets
Set input offset
Set odd/even offset in back end
YES
Set another color
NO
Set gain/offset bus size in back end
Set external pixel offset in back end
Scan white line
Compute pixel gains in back end
YES
Adjust PGA gain
NO

CLAMP LEVEL DECISION FOR EACH INPUT

* Assume that PGA gain = 1
* This flow chart is not fixed, but recommended.
  User can modify this algorithm.

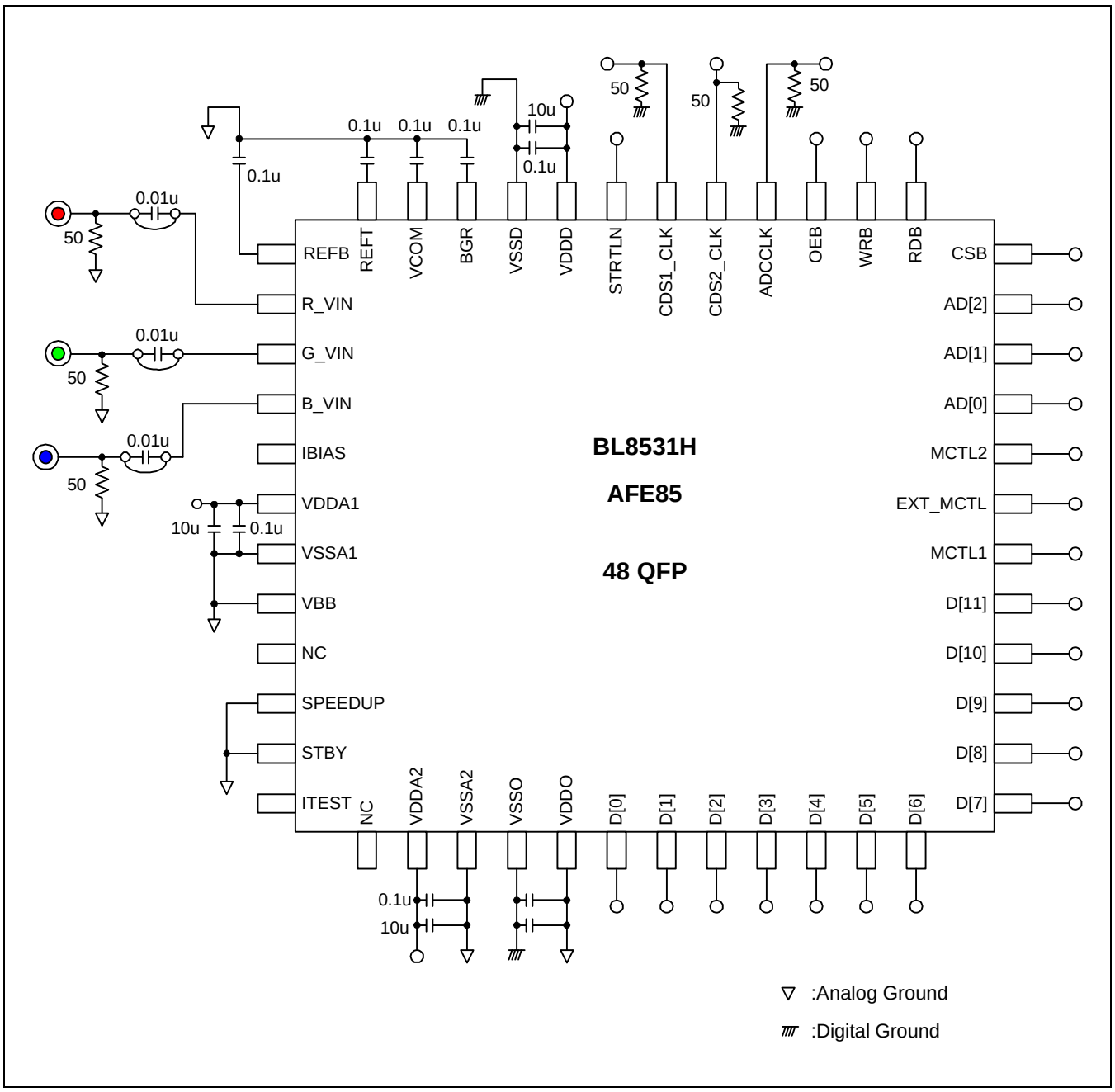


CORE EVALUATION GUIDE



PACKAGE CONFIGURATION

The digital pins should be well decoupled to the analog ground plane.



PACKAGE PIN DESCRIPTION

Pin No.	Pin Name	I/O Type	Description
1	NC	-	Not Connected
2	VDDA2	AP	Analog Power for A/D Converter
3	VSSA2	AG	Analog Ground for A/D Converter
4	VSSO	DG	Output Buffer Ground
5	VDDO	DP	Output Buffer Power
6	D[0]/MPU[0]	DB	Digital Output LSB/Register Input LSB
7	D[1]/MPU[1]	DB	Digital Output/Register Input
8	D[2]/MPU[2]	DB	Digital Output/Register Input
9	D[3]/MPU[3]	DB	Digital Output/Register Input
10	D[4]/MPU[4]	DB	Digital Output/Register Input
11	D[5]/MPU[5]	DB	Digital Output/Register Input
12	D[6]/MPU[6]	DB	Digital Output/Register Input
13	D[7]/MPU[7]	DB	Digital Output/Register Input MSB
14	D[8]	DB	Digital Output
15	D[9]	DB	Digital Output
16	D[10]	DB	Digital Output
17	D[11]	DB	Digital Output MSB
18	MCTL1	DI	Color Pointer for MUX Control
19	EXT_MUX	DI	MUX Control Mode Selection Low : by MCTL1, MCTL2 High : by Configuration Register
20	MCTL2	DI	Color Pointer for MUX Control
21	AD[0]	DI	Register Selection Pin
22	AD[1]	DI	Register Selection Pin
23	AD[2]	DI	Register Selection Pin
24	CSB	DI	Chip Selection (Active Low)

PACKAGE PIN DESCRIPTION (Continued)

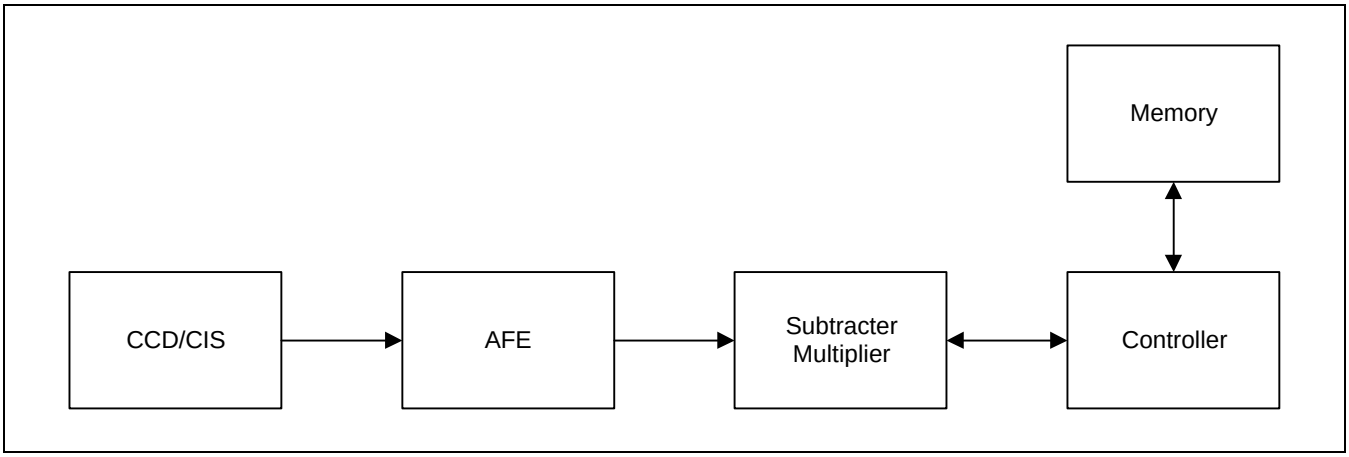
Pin No.	Pin Name	I/O Type	Description
25	RDB	DI	Read Strobe (Active Low)
26	WRB	DI	Write Strobe (Active Low)
27	OEB	DI	Output Enable (Active Low)
28	ADCCLK	DI	A/D Converter Clock Input
29	CDS2_CLK	DI	CDS Data Clock Input
30	CDS1_CLK	DI	CDS Reset Clock Input
31	STRTLN	DI	Start Line (Active Low)
32	VDDD	DP	Digital Power
33	VSSD	DG	Digital Ground
34	BGR	AB	Bandgap Reference Voltage
35	VCOM	AB	Reference Middle Voltage
36	REFT	AB	Reference Top Voltage
37	REFB	AB	Reference Bottom Voltage
38	R_VIN	AI	Red Analog Input
39	G_VIN	AI	Green Analog Input
40	B_VIN	AI	Blue Analog Input
41	IBIAS	AB	Analog Test Pin (Floating)
42	VDDA1	AP	Analog Power
43	VSSA1	AG	Analog Ground
44	VBB	AG	Analog Ground
45	NC	-	Not Connected
46	SPEEDUP	DI	Test Pin (Set to Low)
47	STBY	DI	Stand By (Power Down) Low = Normal High = Power Save
48	ITEST	AB	Analog Test Pin (Floating)

USER GUIDE

CONFIGURATION

It is necessary that output signal of analog front end be shading-compensated by back end logic block including subtracter and multiplier.

Shading-Compensation Block



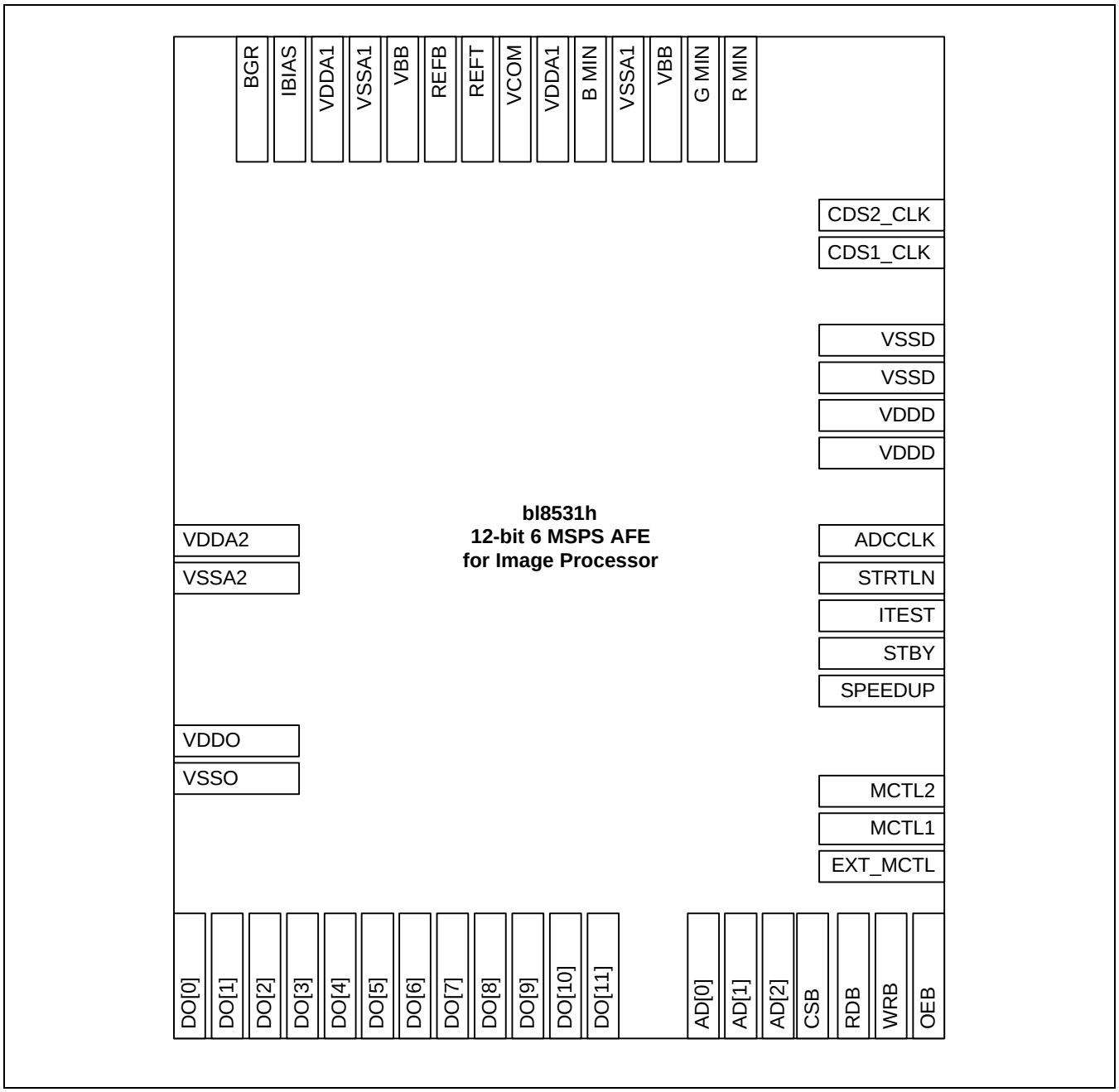
Output Bus Controls

CSB	0	0	0	0	1	1
WRB	0	1	1	1	x	x
RDB	1	x	0	x	x	x
OEB	1	0	x	1	0	1
DOUT	MPU Input	X	MPU Output	Z	ADC Output	Z

x: Don't Care X: Unknown (Not recommended)
Z: High Impedance

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
VDDA1	External	- Maintain the large width of lines as far as the pads. - Place the port positions to minimize the length of power lines. - Do not merge the analog powers with other power from other blocks. - Use good power and ground source on board.
VSSA1	External	
VDDA2	External	
VSSA2	External	
VDDD	External	
VSSD	External	
VDDO	External	
VSSO	External	
VBB	External	
R_VIN	External/Internal	- Do not overlap with digital lines. - Maintain the shortest path to pads.
G_VIN	External/Internal	
B_VIN	External/Internal	
ADCCLK	External/Internal	- Separate from all other analog signals
CDS1_CLK	External/Internal	
CDS2_CLK	External/Internal	
REFT	External/Internal	- Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
REFB	External/Internal	
VCOM	External/Internal	
BGR	External/Internal	
IBIAS	External/Internal	- Test pins - SPEEDUP = set to "LOW"
ITEST	External/Internal	
STBY	External/Internal	
SPEEDUP	External/Internal	
STRTLN	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
EXT_MCTL	External/Internal	
MCTL1,2	External/Internal	
OEB	External/Internal	
WRB	External/Internal	
RDB	External/Internal	
CSB	External/Internal	
AD[2:0]	External/Internal	
D[11:0]	External/Internal	

FEEDBACK REQUEST

It should be quite helpful to our AFE core development if you specify your system requirements on AFE in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

Characteristics	Symbol	Min	Typ	Max	Unit	Comment
Resolution					Bits	
Signal-to-Noise & Distortion Ratio	SNDR				dB	
Conversion Rate 3-Channel with CDS 1-Channel with CDS					 MSPS MSPS	
Differential Nonlinearity	DNL				LSB	
Integral Nonlinearity	INL				LSB	
Unipolar Offset Error					%FSR	
Gain Error					%FSR	
Anlog Input Full-Scale Input					Vp-p	
Power Supply Analog Voltage Digital Voltage	 VDDA VDDD				 V V	
Power Consumption					mW	
Temperature Range					°C	

— What do you want to choose as power supply voltages? For example, the analog VDD needs to be 5V. The digital VDD can be 3.3V/5V.

— Which modes of AFE do you use for overall system ? (Refer to page 9)
For example: 3channel operation with CDS / 3channel SHI(CIS) operation
1channel operation with CDS / 1channel SHI(CIS) operation

— Would you define the gain range and input offset range ?

— Could you explain external/internal pin configurations as required?

— Should the bus interface be compatible with TTL ?

— When STRTLN is low, the internal circuit is reset on the rising edge of ADCCLK.
Which channel is multiplexer switched to on the next rising edge of ADCCLK, after STRTLN goes high?

— If possible, present other requirements below.

HISTORY CARD

Version	Date	Modified Items	Comments
ver 1.0	98.11	Original version published (preliminary)	
ver 1.1	99.1	Release the formal data sheet	
ver 2.0	02.4.16	Change the data sheet format, phantom information added	

NOTES

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