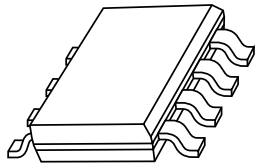


DATA SHEET



BLT71/8 UHF power transistor

Product specification
Supersedes data of 1996 Feb 06

1997 Oct 14

UHF power transistor

BLT71/8

FEATURES

- High efficiency
- Very high gain
- Internal pre-matched input
- Low supply voltage.

APPLICATIONS

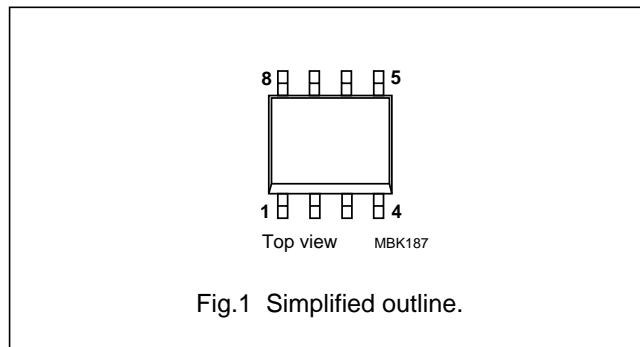
- Hand-held radio equipment in common emitter class-AB operation for the 900 MHz communication band.

DESCRIPTION

NPN silicon planar epitaxial power transistor encapsulated in a SOT96-1 (SO8) plastic SMD package.

PINNING - SOT96-1

PIN	SYMBOL	DESCRIPTION
1, 8	b	base
2, 4, 5, 7	e	emitter
3, 6	c	collector



QUICK REFERENCE DATA

RF performance at $T_s \leq 60\text{ °C}$ in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V _{CE} (V)	P _L (W)	G _p (dB)	η _c (%)
CW, class-AB	900	4.8	1.2	≥11 typ. 13	≥55 typ. 63

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	16	V
V _{CEO}	collector-emitter voltage	open base	–	8	V
V _{EBO}	emitter-base voltage	open collector	–	2.5	V
I _C	collector current (DC)		–	500	mA
P _{tot}	total power dissipation	T _s = 60 °C; V _{CE} ≤ 6.5 V; note 1	–	2.9	W
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	175	°C

Note

1. T_s is the temperature at the soldering point of the collector pin.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	$P_{dis} = 2.9\text{ W}; T_s = 60\text{ }^\circ\text{C}; \text{note 1}$	40	K/W

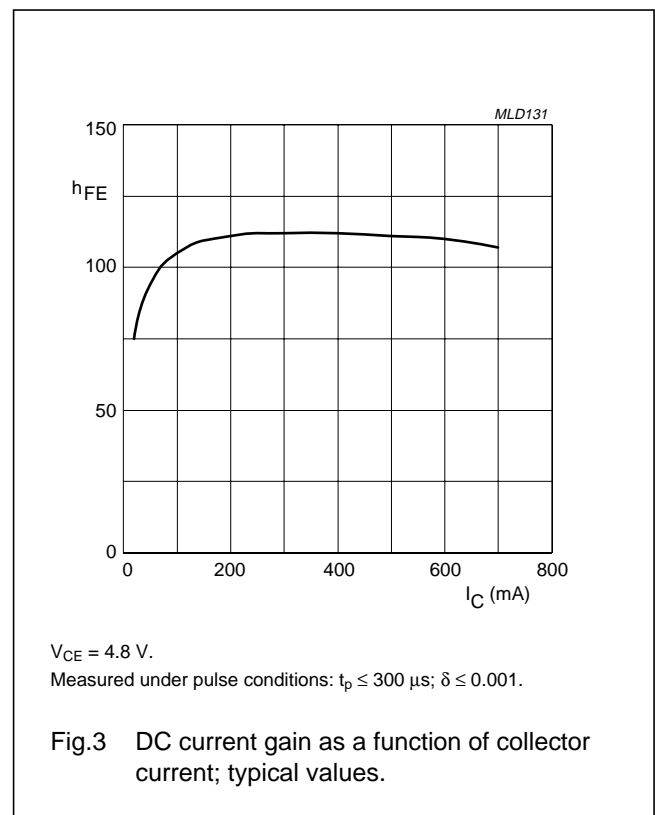
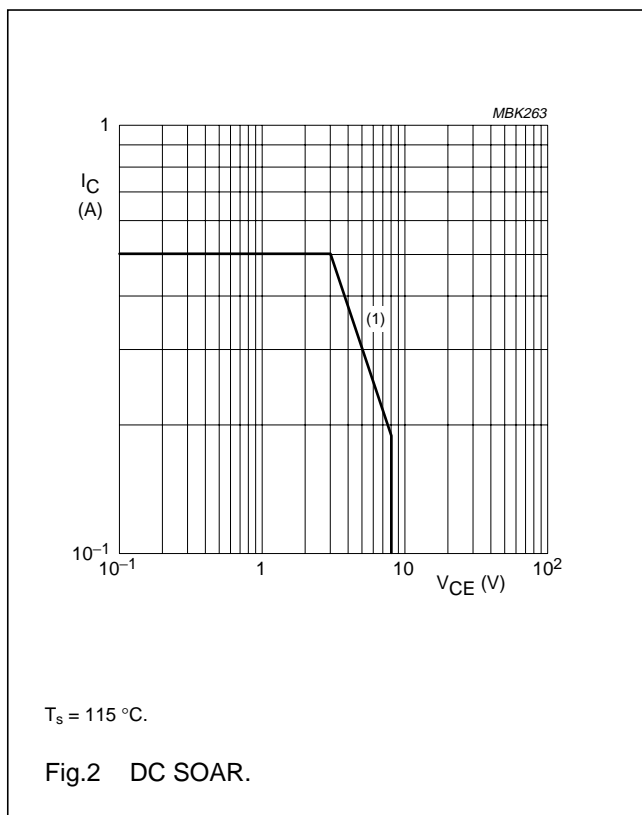
Note

- T_s is the temperature at the soldering point of the collector pin.

CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 0.5\text{ mA}$	16	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 10\text{ mA}$	8	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 0.1\text{ mA}$	2.5	–	V
I_{CES}	collector leakage current	$V_{CE} = 8\text{ V}; V_{BE} = 0$	–	0.1	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 100\text{ mA}$	25	–	
C_c	collector capacitance	$V_{CB} = 4.8\text{ V}; I_E = i_e = 0; f = 1\text{ MHz}$	–	7	pF
C_{re}	feedback capacitance	$V_{CE} = 4.8\text{ V}; I_C = 0; f = 1\text{ MHz}$	–	5	pF



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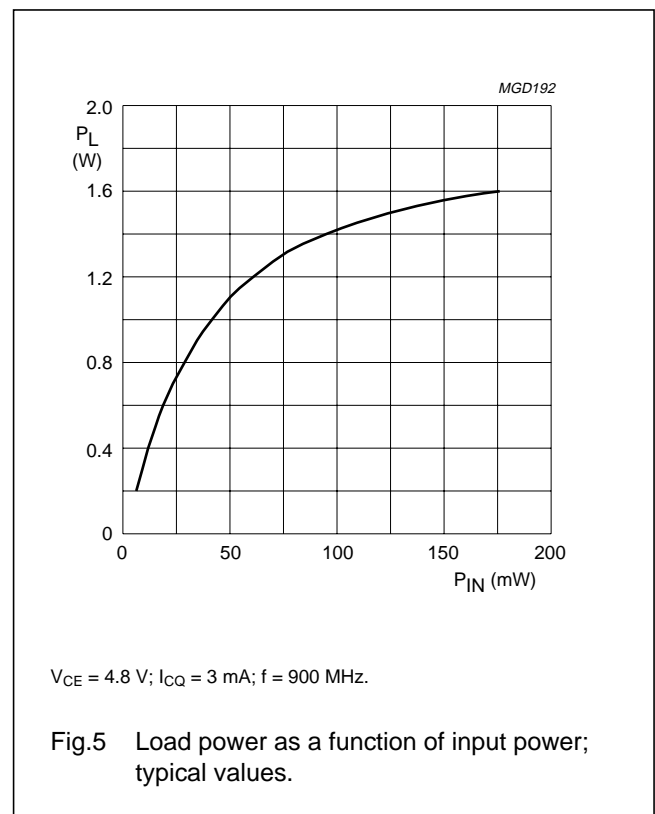
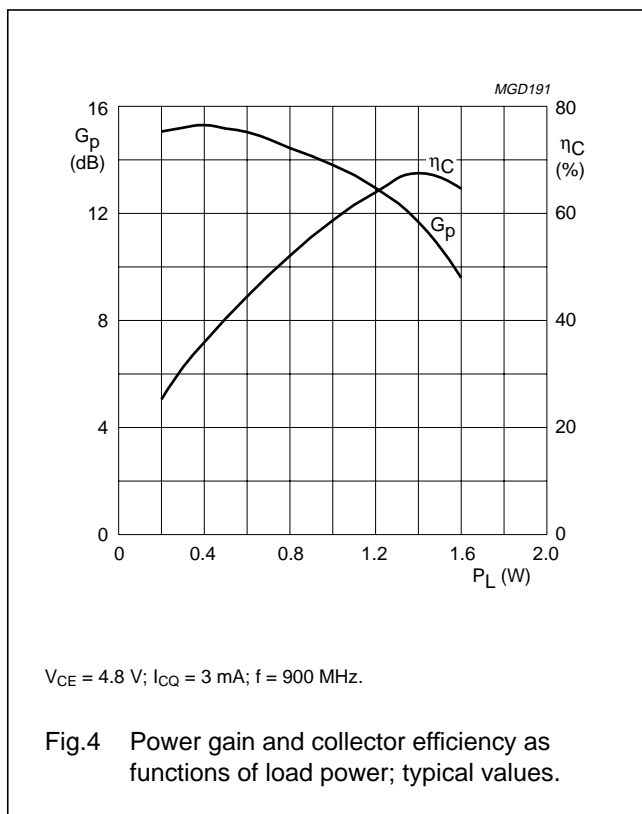
APPLICATION INFORMATION

RF performance at $T_s \leq 60^\circ\text{C}$ in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V _{CE} (V)	I _{CQ} (mA)	P _L (W)	G _p (dB)	η _c (%)
CW, class-AB	900	4.8	3	1.2	≥11 typ. 13	≥55 typ. 63

Ruggedness in class-AB operation

The BLT71/8 is capable of withstanding a load mismatch corresponding to VSWR = 6 : 1 through all phases under the following conditions: f = 900 MHz; V_{CE} = 6.5 V; I_{CQ} = 3 mA; P_L = 1.2 W; T_s = 60 °C.



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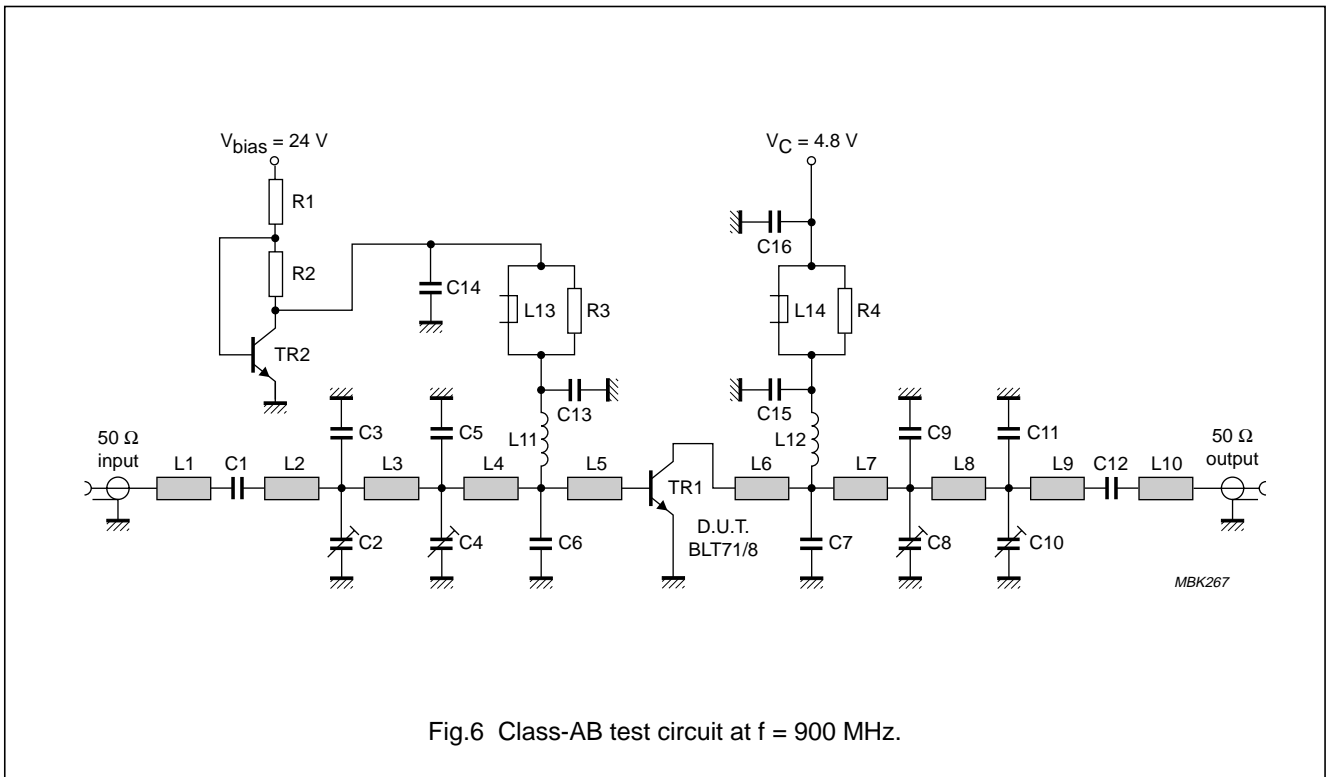
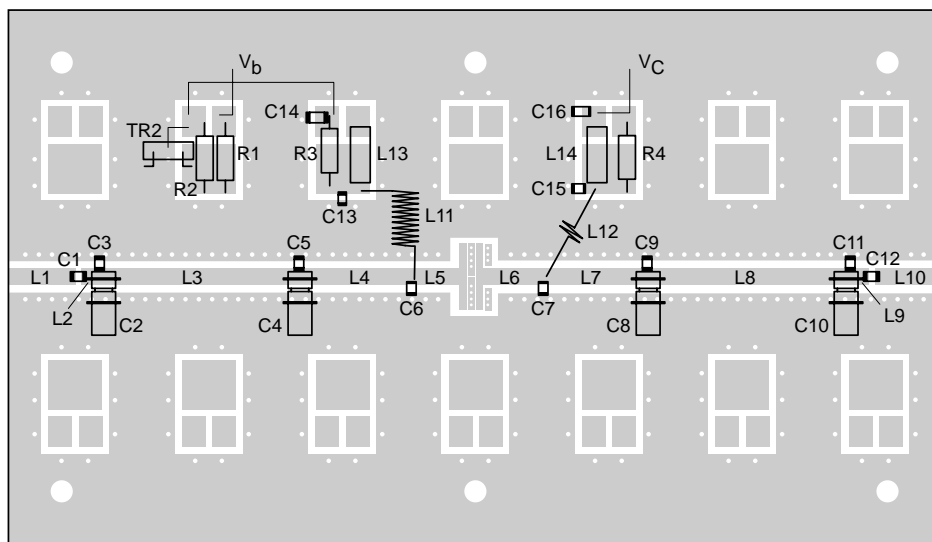
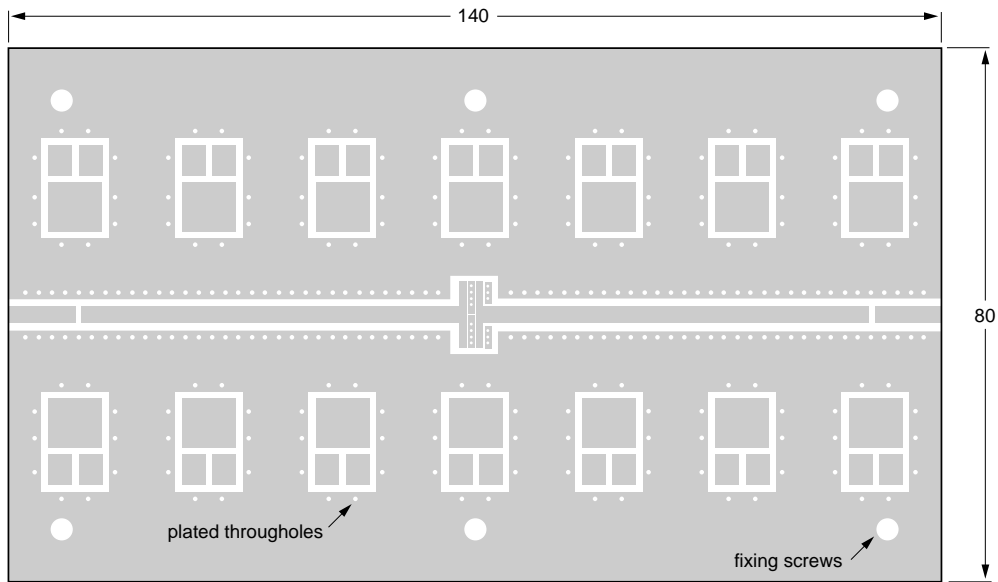


Fig.6 Class-AB test circuit at f = 900 MHz.

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Dimensions in mm

The components are situated on one side of the copper-clad printed circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.7 Printed-circuit board and component lay-out for the 900 MHz class-AB test circuit.

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List of components (see Figs 6 and 7).

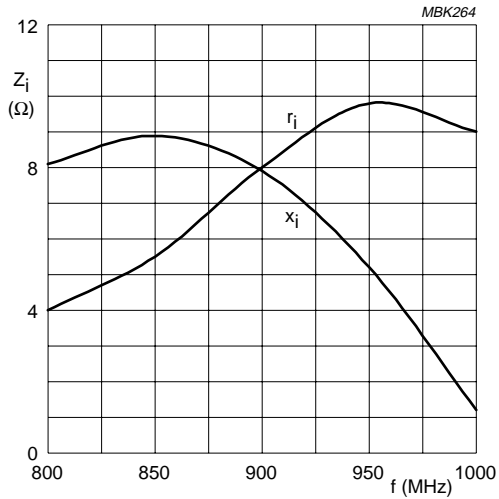
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12, C13, C15	multilayer ceramic chip capacitor; note 1	120 pF		
C2, C4, C8, C10	Giga-Trim capacitor; note 2	0.6 to 4.5 pF		
C3	multilayer ceramic chip capacitor; note 1	4.7 pF		
C5	multilayer ceramic chip capacitor; note 1	5.6 pF		
C6	multilayer ceramic chip capacitor; note 1	3.9 pF		
C7	multilayer ceramic chip capacitor; note 1	6.8 pF		
C9	multilayer ceramic chip capacitor; note 1	7.5 pF		
C11	multilayer ceramic chip capacitor; note 1	5.1 pF		
C14, C16	multilayer ceramic chip capacitor; note 1	10 nF		
L1, L10	stripline; note 3	50 Ω	10 x 2.4 mm	
L2	stripline; note 3	50 Ω	2 x 2.4 mm	
L3	stripline; note 3	50 Ω	30.4 x 2.4 mm	
L4	stripline; note 3	50 Ω	17.4 x 2.4 mm	
L5	stripline; note 3	50 Ω	6.8 x 2.4 mm	
L6	stripline; note 3	50 Ω	8 x 2.4 mm	
L7	stripline; note 3	50 Ω	19 x 2.4 mm	
L8	stripline; note 3	50 Ω	28 x 2.4 mm	
L9	stripline; note 3	50 Ω	1.6 x 2.4 mm	
L11	10 turns 1 mm enamelled copper wire	140 nH	int. dia. = 4 mm; lead 1 = 2.5 mm; lead 2 = 11 mm	
L12	2 turns 1 mm enamelled copper wire	60 nH	int. dia. = 2 mm; leads = 2 x 7.5 mm	
L13, L14	4S2 wideband RF choke			4330 030 36301
R1	metal film resistor	1.4 k Ω ; 0.6 W		2322 156 11402
R2, R3, R4	metal film resistor	10 Ω ; 0.6 W		2322 156 11009
TR1	device under test	BLT71/8		
TR2	NPN transistor	BD139		9330 912 20112

Notes

- American Technical Ceramics type 100A or capacitor of same quality.
- Tekelec Giga-trim, type 37271.
- The striplines are on a double copper-clad printed-circuit board, with DUROID dielectric ($\epsilon_r = 2.2$); thickness 0.79 mm, thickness of the copper sheet 2 x 35 μm .

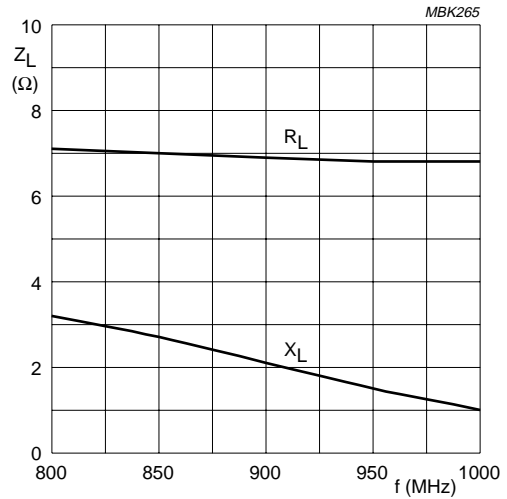
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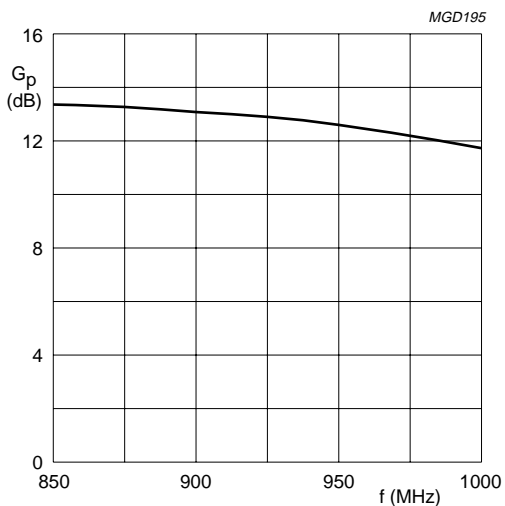
$V_{CE} = 4.8$ V; $I_{CQ} = 3$ mA; $P_L = 1.2$ W; $T_{amb} = 25$ °C.

Fig.8 Input impedance as a function of frequency (series components); typical values.



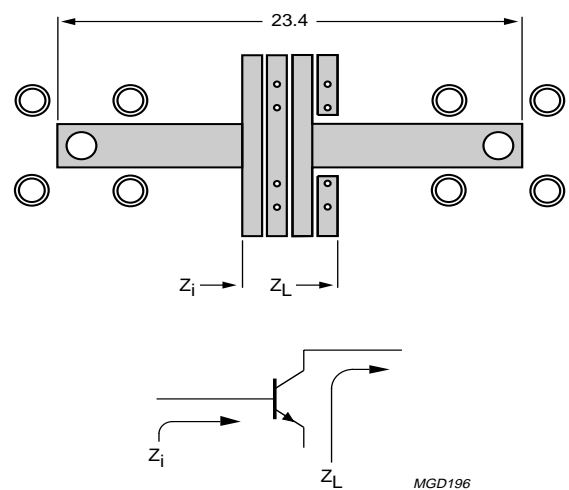
$V_{CE} = 4.8$ V; $I_{CQ} = 3$ mA; $P_L = 1.2$ W; $T_{amb} = 25$ °C.

Fig.9 Load impedance as a function of frequency (series components); typical values.



$V_{CE} = 4.8$ V; $I_{CQ} = 3$ mA; $P_L = 1.2$ W; $T_{amb} = 25$ °C.

Fig.10 Power gain as a function of frequency (series components); typical values.



Dimensions in mm.

Fig.11 RF test print and definition of transistor impedance.

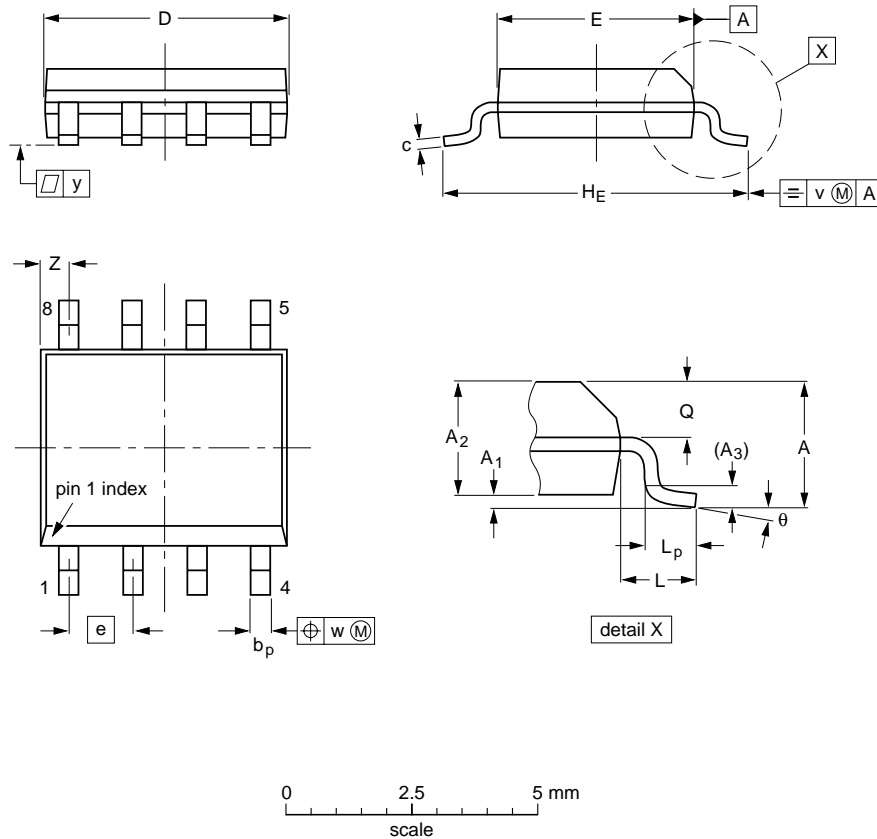
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PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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