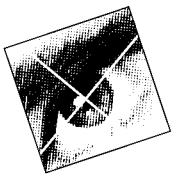


CIRCUIT DESCRIPTION

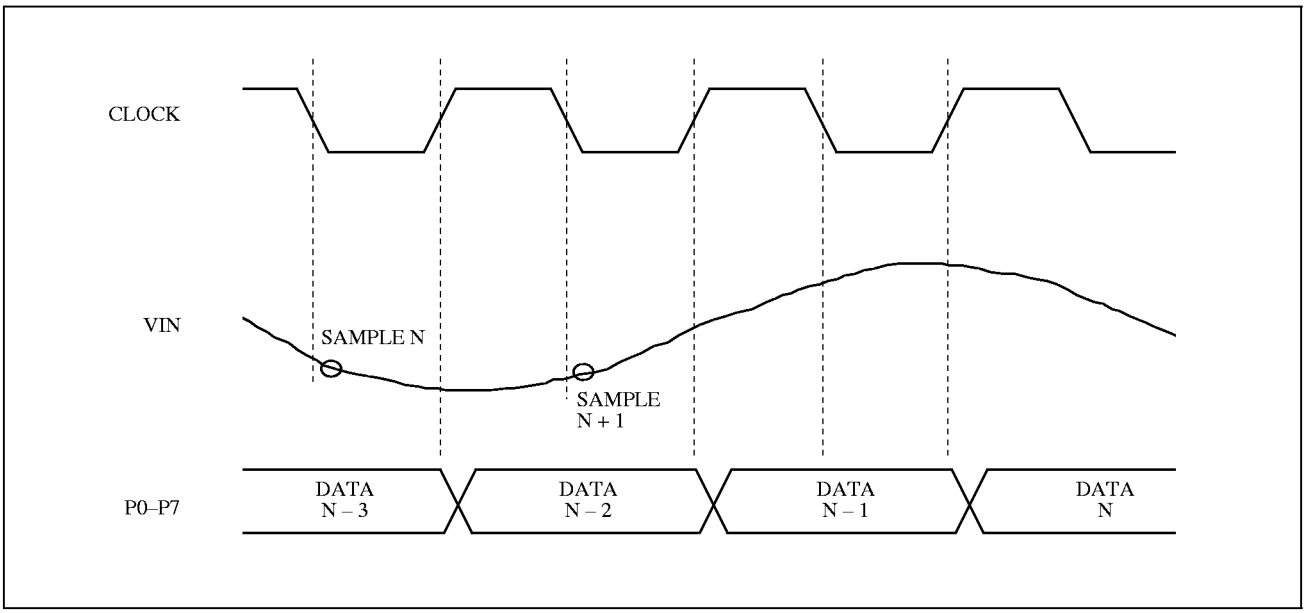
General Operation

The Bt252 uses an 8-bit flash A/D converter to digitize the video signal. The A/D digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+).

The values of REF+ and REF– are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Application Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt252. The sample is taken following the falling edge of CLOCK. Two positive CLOCK edges later, after the lookup table is addressed, the registered data is output on P0–P7.

Figure 1. General Operation



MPU Interface

As shown in the functional block diagram, the Bt252 supports a standard MPU interface (D0–D7, RD*, WR*, A0, and A1). MPU operations are asynchronous to the clock.

An internal 8-bit address register, in conjunction with A0 and A1, is used to specify which control register or RAM location the MPU is accessing, as shown in Table 1. All registers and RAM locations may be written to or read by the MPU at any time; however, while digitizing a video signal, the MPU should not access the RAM, as this will corrupt the digitized data.

When the MPU accesses the RAM, the address register increments after each MPU access (read or write cycle). After writing to RAM location $FF, the address register resets to $00.

When the address register or control registers are accessed, the address register does not increment after an MPU read or write cycle. Data written to reserved locations is ignored; data read from reserved locations returns invalid data. ADDR0 corresponds to D0 and is the least significant bit.

Table 1. Address Register Operation

A1	A0	ADDR7-ADDR0	Addressed by MPU
0	0	xxxx xxxx	address register
0	1	0000 0000	RAM location $00
0	1	0000 0001	RAM location $01
:	:	:	:
0	1	1111 1111	RAM location $FF
1	0	xxxx xx00	command register
1	0	xxxx xx01	IOUT0 data register
1	0	xxxx xx10	IOUT1 data register
1	0	xxxx xx11	reserved
1	1	xxxx xxxx	reserved

Analog Input Selection

The Bt252 supports four analog input sources, VID0–VID3. The MPU specifies which of these is to be digitized through the command register.

The selected video signal is output onto VOUT. VOUT may be connected directly to VIN if no filtering or gain of the video signal is required.

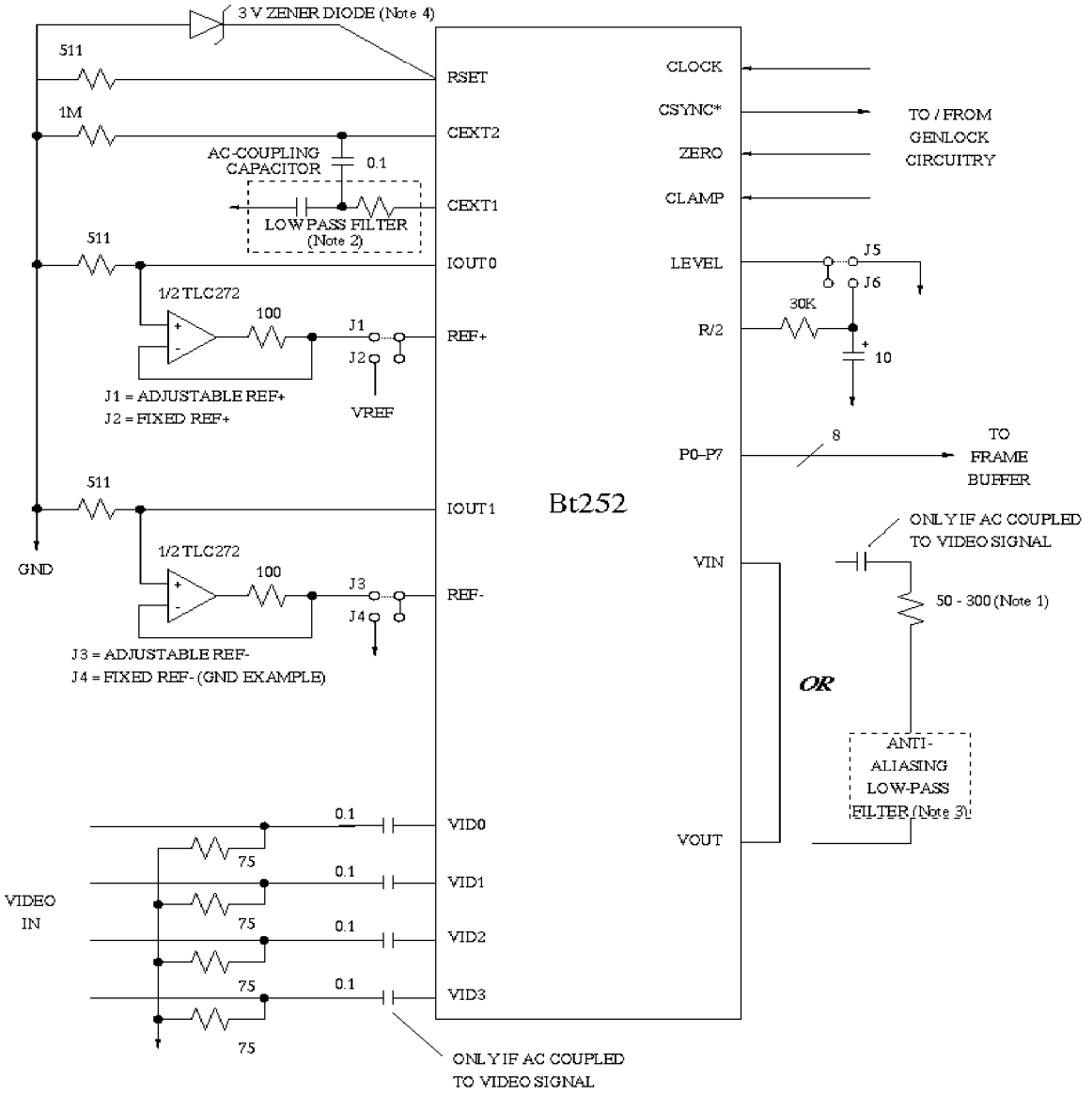
If only the luminance information of a video signal containing color subcarrier information is being digitized, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Sync information (if present) will still be present on VOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

The 75 Ω resistors to ground (Figure 2) provide the typical 75 Ω termination required by video signals.

Figure 2. Typical Bt252 External Circuit



Notes: (1). Needed only if active filter is used. Adjust for minimum clock kickback.
(2). Filter to remove colorburst, preventing false sync detection.
(3). If the antialiasing filter if located here, only the filter is required. Otherwise, each video input must have an antialiasing filter.
(4). See RSET pin name definition for discussion of zenor diode.
5. J5 = DC restore to GND
6. J6 = Color Difference DC restore

A/D Reference Generation

As shown in Figure 2, the Bt252 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, REF+ is connected to a 0.7–1.2 V reference (VREF) and REF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7–1.2 V and no adjustment of gain or offset.

If jumpers J1 and J3 are selected, the MPU-adjustable outputs IOUT0 and IOUT1 may be used for gain and offset of the video signal. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations, such as contrast enhancement or level adjustments, may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation. However, because single-supply op-amps are limited, REF– may not be able to achieve a voltage below 300 mV with a single 5 V supply. Using an External Reference in the Application Information section contains further information.

IOUT0 and IOUT1 are current outputs (0–2.5 mA) generated by two 6-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0–1.2 V level that drives the REF+ and REF– inputs through voltage followers.

The DAC outputs should not drive the top of the reference ladder directly. The reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of REF– is desired, the DAC output must drive REF– with a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the P0–P7 outputs are not updated. They retain the data loaded before the ZERO cycle.

AC-coupled Video and A/D Input Clamping

When video is AC coupled, capacitors are required on all video inputs. A capacitor may also be needed between VIN and VOUT, depending on the filtering implementation (see to Figure 2). The video mux will DC adjust the input video to prevent channel- to-channel crosstalk through the video mux.

If VIN is AC coupled to the video signal, the CLAMP and LEVEL controls may be used to DC restore the video signal. While CLAMP is a logical one, the video signal is clamped to the voltage level present on the LEVEL pin. CLAMP should be asserted during static intervals and at least 200 ns before or after a video transition. During clamping, the resistances of the mux and clamp are approximately 100 and 50 Ω, respectively. Incorporation of the 0.1 µF clamp capacitor yields an RC time constant of 15 µs. On power-up or after a transition of the video input, approximately three to five time constants will be required to completely DC restore the video signal. When the clamp is asserted on the back porch for 0.5–1.5 µs, several lines of video will be required to properly DC restore the signal. For example, clamping the video signal for 1 µs during each line of video will require 75 lines of video for proper DC restoration. This is assuming five time constants are needed.

When RGB or luminance video signals are DC restored, LEVEL is typically connected to the same potential as REF–.

When color difference video signals are DC restored, LEVEL is typically at the midpoint between REF+ and REF–. The Bt252 provides an R/2 reference ladder tap that may be used to generate the proper DC voltage (jumper J6 in Figure 2). The R/2 tap should drive a high-impedance load while capturing an image to maintain optimum linearity of the A/D converter.

DC-Coupled Video

When video is DC coupled, the video levels must be within the digitization range of the A/D. To avoid channel-to-channel crosstalk through the video mux, nonsynchronized video sources must not drop more than 100 mV below ground. For example, if the black/blank level of the DC-coupled video is at ground, an external sync clipper must be used to guarantee that the sync tip does not drop below –100 mV. If VIN is DC coupled to the video signal, the level should float or the clamp should be a logical zero.

Antialiasing Filtering and VIN Input Considerations

The input video must be passed through an antialiasing filter to meet Nyquist criteria. The filter can be placed between VIN and VOUT to filter all video sources or on each video input before the MUX.

The 50–300 Ω resistor, shown in Figure 2 after the low-pass filter, is required only if an active low-pass filter is used. The resistor provides isolation from any clock kickback noise on VIN, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on VIN. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

If DC restoration and low-pass filtering between VOUT and VIN are implemented, a 0.1 µF capacitor is required after the low-pass filter. If no filter between VOUT and VIN is used, the capacitor is not required, as the DC restoration can still be implemented with the 0.1 µF capacitors on the VIDx inputs.

Multiplexer Considerations

DC level maintenance within the rated compliance range is necessary to obtain the best linearity and crosstalk performance.

Lookup Table RAM

A 256 x 8 lookup table RAM is provided on-chip to implement simple imaging operations such as gamma manipulation, contrast enhancement, data inversion, or a nonlinear transfer function of the A/D converter. Data from the A/D is used to address the RAM; the addressed data is output onto P0–P7.

The RAM may be effectively bypassed by loading each location with its corresponding address. As the lookup table RAM is not dual ported, MPU accesses have priority over digitized data passing through the RAM. During MPU accesses to the RAM, P0–P7 are undefined.

Sync Detect Circuitry

The Bt252 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. CSYNC* is output asynchronously to the clock, and there are no pipeline delays. (The output delay from VIN to CSYNC* is approximately 25 ns.)

The MPU specifies from which analog input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC couples the video signal to the sync detection circuit. The sync tip is internally clamped to a DC level. The sync detect value determines the threshold above this DC level where the Bt252 detects sync. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero. A low-pass filter removes the colorburst signal.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 2).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA (CEXT1 may float), or an unused (grounded) video input should be selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA, and the CSYNC* output should be left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Pin Description

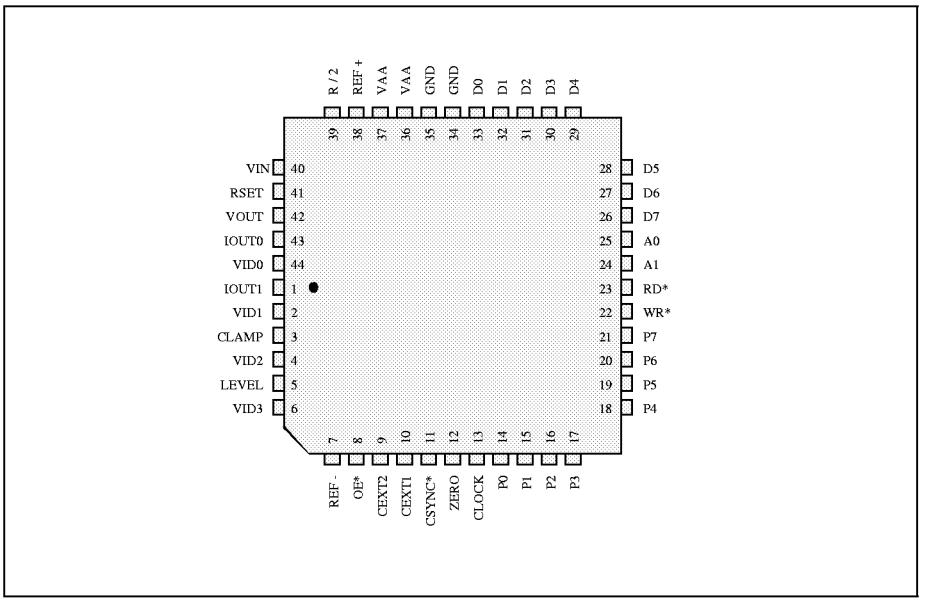
Table 2. Pin Descriptions Grouped by Pin Function *(1 of 2)*

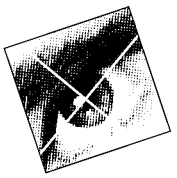
Pin name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. RSET is used to provide reference information to the internal D/A converters (See Figure 2). At cold operating temperatures, the RSET pin might power up with a voltage of 4 V. (This is a threshold below the supply voltage.) A minimum of perturbation on the RSET pin or an increase in temperature will change states on the bandgap reference to the normal 1.2 V operating point.
	RSET can be forced to a power up with the correct voltage by adding a 3 V zener diode in parallel with the RSET resistor. If the Bt252 powers up in the wrong state, the zener will activate and toggle the bandgap reference voltage to the correct state.
	The alternative is to leave the part configured without the diode. This might necessitate resequencing the power for initial operation of the boards at cold temperatures.
IOUT0, IOUT1	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between each pin and GND (See Figure 2). The relationship between full-scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND (See Figure 2).
A/D Functions	
REF+	Top of resistor ladder (voltage input). REF+ sets the VIN voltage level that corresponds to $FF from the A/D converter. For noise immunity reasons, a decoupling capacitor is not recommended on REF+.
REF-	Bottom of resistor ladder (voltage input). REF– sets the VIN voltage level that generates $00 from the A/D converter.
R/2	Reference ladder midpoint tap. If not used, this pin should remain floating. For noise immunity reasons, a decoupling capacitor is not recommended on R/2. External loading should be less than 1 µA to obtain the best linearity.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. ZERO is latched on the rising edge of CLOCK. During zeroing cycles, P0–P7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN input is forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. In applications where VIN is DC coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.

Table 2. Pin Descriptions Grouped by Pin Function *(2 of 2)*

Pin name	Description
LEVEL	Level control input (voltage input). This input is used to specify the voltage level for DC restoration while CLAMP is a logical one. In applications where VIN is DC coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.
VIN	A/D converter input. The analog signal to be digitized should be connected to this analog input pin. It may be either DC or AC coupled to the video signal being digitized.
VID0-VID3, VOUT	Analog inputs and analog output. VID0–VID3 are connected to the video signals to be digitized. The signal selected to be digitized is output onto VOUT. Unused inputs should be connected to GND.
CLOCK	Clock input (TTL compatible). CLOCK should be driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected on the VID0–VID3 input specified by the command register, converted to TTL levels, and output onto this pin. CSYNC* is output asynchronously to the clock, and there are no pipeline delays.
Digital Control Functions	
P0-P7	Digitized video data outputs (TTL compatible). Digitized video data is output onto these pins following the second rising edge of CLOCK. P0 is the least significant bit. P0–P7are three-stated if OE* is a logical one.
OE*	Output enable control input (TTL compatible). A logical one three-states the P0–P7 outputs asynchronously to CLOCK.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device through D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0-D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0, A1	Address control inputs (TTL compatible). A0 and A1 are used to specify the operation the MPU is performing, as indicated in Table 1. They are latched on the falling edge of either RD* or WR*.
Power and Ground	
VAA	+5 V power. All VAA pins must be connected together on the same PCB plane and as close to the device as possible to prevent latchup. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible. (Ceramic chip capacitors are preferred.)
GND	Ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Figure 3. Bt252 Pinout Diagram





INTERNAL REGISTERS

Command Register

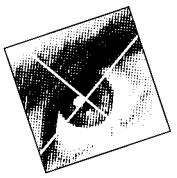
The command register may be written to or read by the MPU at any time and is not initialized. D0 is the least significant bit.

D7, D6	Digitize select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify which analog input is to be digitized. The selected signal is output onto VOUT.
D5, D4	Sync detect select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify from which analog input sync information is to be detected. The selected signal is output onto CEXT1.
D3, D2	Sync detect level select (00) 50 mV (01) 75 mV (10) 100 mV (11) 125 mV	These bits specify the amount above the sync tip to slice CEXT2 for sync detection.
D1, D0	Reserved (logical zero)	The MPU must write a logical zero to these bits to ensure proper operation.

IOUT Data Registers

These two 6-bit registers specify the output current on the IOUT0 and IOUT1 outputs, from 0 mA ($00) to full scale ($FC). The 6 MSBs of data are used to drive the DACs. D0 and D1 (the 2 LSBs) must be programmed to be a logical zero.

These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.



PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

For optimum performance, before PCB layout is begun, the CMOS digitizer layout examples in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, Application Notes AN-13, 14, and 15, respectively, should be studied. These Application Notes can be found in the Brooktree Applications Handbook.

The layout should be optimized for lowest noise on the Bt252 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

A single common ground plane covering both analog and digital logic should be used.

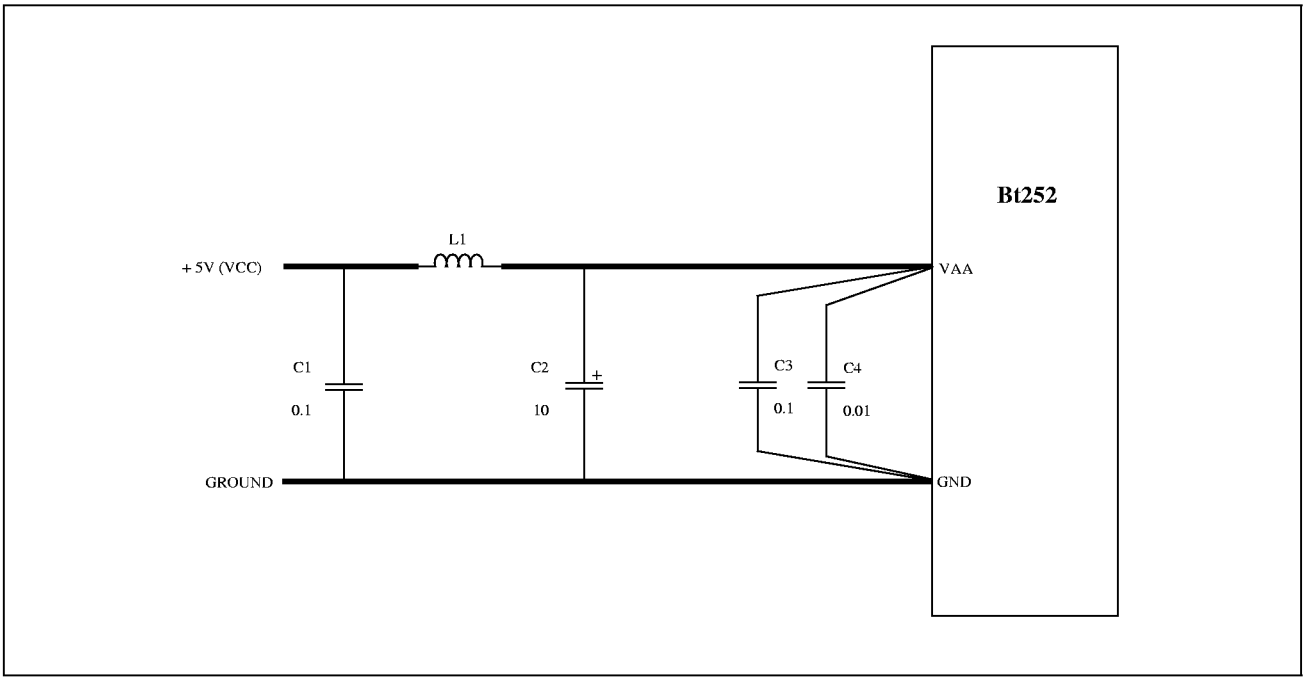
Power Planes

The Bt252 and any associated analog circuitry should have their own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt252.

The regular PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt252 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that the regular PCB power plane does not overlay the analog power plane.

Figure 4. Typical Power Supply Connection Diagram and Parts List



Location	Description	Vendor Part Number
C1, C3	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2	10 µF tantalum capacitor	Mallory CSR13G106KM
C4	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
L1	ferrite bead	Fair-Rite 2743001111
Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt252.		

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

The VAA and GND pins should have a 0.1 µF ceramic chip capacitor located as close as possible to the device pins. The capacitors should be connected directly to the VAA and GND pins with short, wide traces.

Digital Signal Interconnect

The digital signals of the Bt252 must be isolated as much as possible from the analog signals and other analog circuitry to prevent crosstalk. Also, the digital signals should not overlay the analog power plane.

Termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs. Microstrip techniques should be employed to keep video trace impedance at 75 Ω, to match standard coax impedance.

Also, high-speed TTL signals should not be routed close to the analog signals, to minimize noise coupling.

Application Information

Zeroing

As the comparators on the Bt252 must be periodically zeroed, it is convenient to assert ZERO during each horizontal blanking interval.

Before the Bt252 is used after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications, this will be transparent because of the number of horizontal scan lines that will have occurred before the Bt252 was used.

While the recommended zeroing interval is maintained, the Bt252 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0 and IOUT1) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

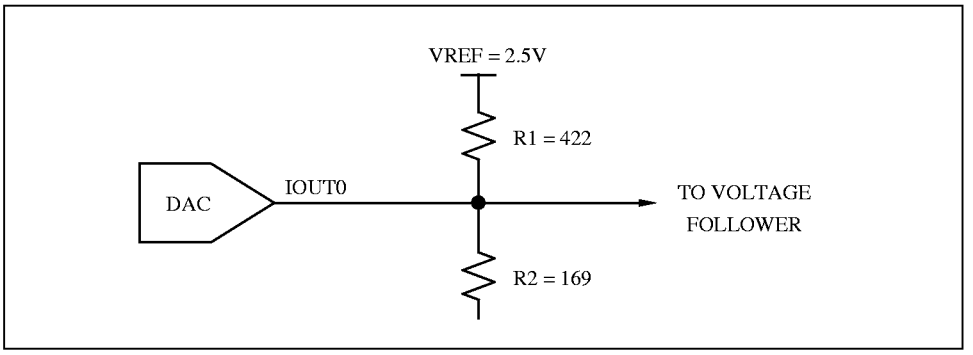
Figure 5 shows a circuit that allows adjustment of the REF+ inputs from 0.714–1 V with 4.5 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FC, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2 as follows:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF–) may be adjusted from 0–0.286 V with 1.125 mV resolution with a 121 Ω resistor to ground rather than a 511 Ω resistor. While the minimum range is 0 V, the resistor to ground may be used to adjust the total range and, thus, the resolution.

Figure 5. Increasing DAC Output Resolution

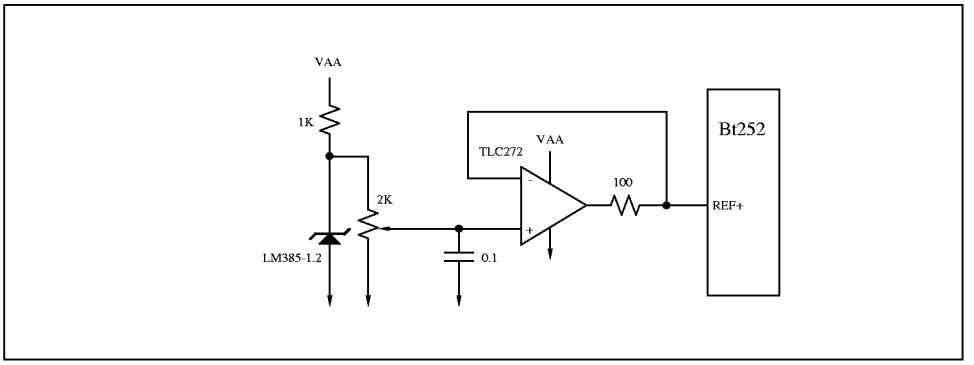


Using An External Reference

Figure 6 illustrates the use of a 1.2 V LM385 and a TLC272 to generate a 0–1.2 V reference for applications that require a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that can of operate from a single +5 V supply.

To prevent ringing in the TLC272 from clock kickback, a 100 Ω resistor as shown in Figure 5 is recommended. If an op-amp is chosen that has a better transient response than the TLC272, the resistor may not be needed. This circuit may also be used to drive the REF– if a value other than ground is desired. Because single-supply op-amps are limited, REF– may not be set below ~300 mV. To drive REF– to true 0 V in the op-amp configuration, a dual supply must be used. Extreme care must be used in power sequencing to ensure all positive supplies (op-amp and A/D) power on before the negative supply. This will prevent latchup of the A/D.

Figure 6. Using an External Reference



Input Ranges

Table 3 lists some common video signal amplitudes. Signals that exceed 1.2 V should be attenuated with a resistor divider network.

When a signal is digitized with a full-scale range less than 0.7 V, the Bt252's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will, therefore, produce larger integral linearity errors in terms of LSBs.

For example, when the reference difference is set to 0.6 V, 0.6 V video signals may be digitized. However, the integral linearity error will increase to about ±1.8 LSB, and the SNR will be about 40 db. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB and an SNR of about 39 db.

Table 3. Video Signal Tolerances

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Output Noise

Although the A/D exhibits some output noise for a DC input, the output noise remains relatively constant for any input bandwidth (see AC Characteristics section). Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641747-2.

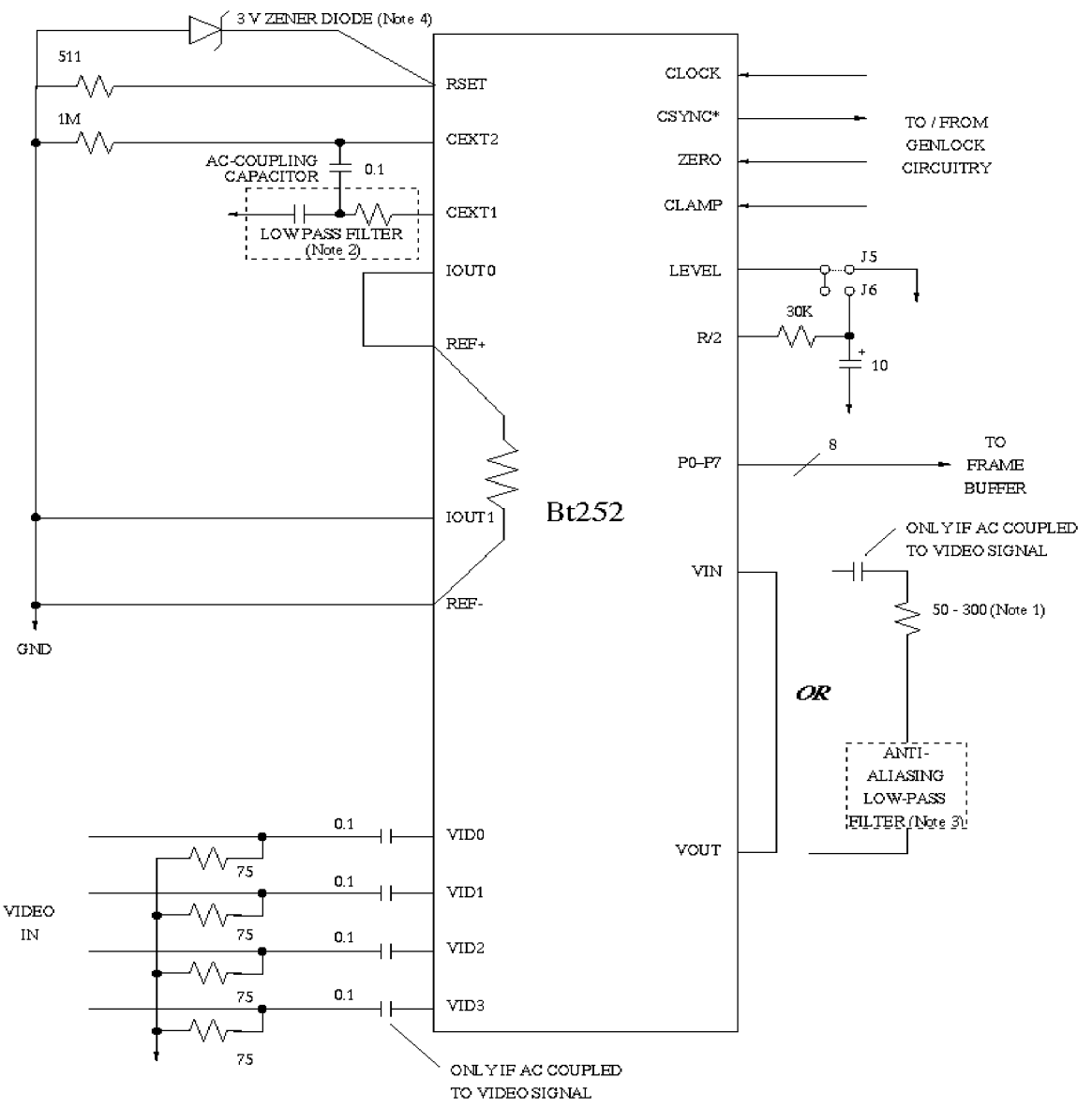
Bt252 with Minimal External Circuitry

Figure 7 shows the Bt252 in an application requiring that 1 V video signals be digitized.

In this instance, the IOUT0 output is driving the top of the reference ladder (REF+) directly, without being buffered by a voltage follower. The internal 500 Ω resistor between IOUT0 and GND develops a 0–1.2 V reference voltage for the A/D (based on the contents of the IOUT0 data register). IOUT1 and REF– are connected to GND.

Although this implementation is not as temperature stable as that shown in Figure 2 (because of some variation in the reference ladder resistance over temperature), it will probably suffice for most applications.

Figure 7. Bt252 Minimal External Circuitry



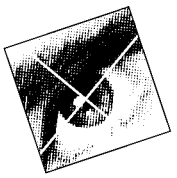
Notes: (1). Needed only if active filter is used. Adjust for minimum clock kickback.
(2). Filter to remove colorburst, preventing false sync detection.
(3). If the antialiasing filter if located here, only the filter is required. Otherwise, each video input must have an antialiasing filter.
(4). See RSET pin name definition for discussion of zener diode.
5. J5 = DC restore to GND
6. J6 = Color Difference DC restore

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors can cause a power supply time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that signal pin voltage will never exceed the power supply voltage by more than +0.5 V.



PARAMETRIC INFORMATION

DC Electrical Parameters

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Voltage References					
Top	REF+	0.7	1	2.0	V
Bottom	REF-	0	0	1.3	V
Difference (Top–Bottom)		0.7	1	1.2	V
VID0–VID3 Amplitude Range		0.5		VAA-0.5	V
Multiplexer Compliance (DC)		-0.2		+2.2	V
VIN Input Amplitude Range		0.7	1	1.2	V
VIN Input Range			REF- to REF+		V
CEXT AC Amplitude		0.2 Vp-p		2.0Vp-p	V
LEVEL Input Voltage	TA	GND-0.5	REF-60	REF+	V
Zeroing Interval				150	µs
Ambient Operating Temperature		0		+70	°C

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin (1)	VIN, VIDx	GND–0.5		VAA + 0.5	V
Analog Input Voltage		GND–0.5		VAA + 0.5	V
R/2 Output Current				25	µA
Ambient Operating Temperature	TA				
Storage Temperature	TS	–55		+125	°C
Junction Temperature	TJ	–65		+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			+150	°C
				220	°C

Notes: (1). This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Coding (Table 3)					
No Missing Codes			guaranteed		Binary
VIN Analog Input (2)					
CLAMP = 0					
Input Current Leakage	IB			1	µA
Input Capacitance	CAIN		35		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
VID0–VID3 Analog Inputs (3)					
Input Impedance to VOUT					
Input Selected			100		Ω
Input Deselected (Leakage)			10		MΩ
Input Capacitance			15		pF
REF+ Reference Input					Ω
Input Impedance			500		

Table 6. DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0			V
Input Low Voltage	VIL			0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			-1	µA
Input Capacitance	CIN		10		pF
P0–P7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	V
Output Capacitance	COUT		10		
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0 and IOUT1 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Accuracy					
Differential Linearity Error	DL			±1	LSB
Integral Linearity Error	IL			±1	LSB
Monotonicity			guaranteed		

Notes: (1). Best-fit linearity. Linearity is tested with RAM transparent (data = address).
(2). LEVEL = GND.
(3). VOUT connected to GND.
4. Test conditions (unless otherwise specified):"Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Table 7. A/D Coding

Vin (V) (1)	P0-P7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

Notes: (1). With REF+ = 1.000 V and REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV. RAM transparent (data = address).

AC Electrical Parameters

Table 8. AC Characteristics *(1 of 3)*

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			20	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time Clock Low Time Clock High Time	1 2 3	50 20 20			ns ns ns
P0–P7 Output Delay Time *(Figure 7)* P0–P7 Output Hold Time OE* Asserted to P0–P7 Valid OE* Negated to P0–P7 3-Stated	4 5 6 7	 9 		40 20 20	ns ns ns ns
ZERO Setup Time ZERO Hold Time ZERO, CLAMP High Time *(1)*	8 9	0 20 1			ns ns Clock
Aperture Delay Aperture Jitter Full Power Input Bandwidth	10 BW		10 50 	 Fs/2	ns ps MHz
Transient Response *(2)* Overload Recovery *(3)* Zero Recovery Time *(4)*			1 1 1		Clock Clock Clock
RMS Signal-to-Noise Ratio Fin = 4.20 MHz, Fs = 12.27 MHz Fin = 4.20 MHz, Fs = 13.50 MHz Fin = 4.20 MHz, Fs = 14.32 MHz Fin = 5.75 MHz, Fs = 13.50 MHz Fin = 5.75 MHz, Fs = 14.75 MHz Fin = 5.75 MHz, Fs = 17.72 MHz Fin = 10.0 MHz, Fs = 20.00 MHz	SNR		 44 44 44 43 43 43 39		 db db db db db db db
RMS Signal & Distortion-to-Noise Ratio Fin = 4.20 MHz, Fs = 12.27 MHz Fin = 4.20 MHz, Fs = 13.50 MHz Fin = 4.20 MHz, Fs = 14.32 MHz Fin = 5.75 MHz, Fs = 13.50 MHz Fin = 5.75 MHz, Fs = 14.75 MHz Fin = 5.75 MHz, Fs = 17.72 MHz Fin = 10.0 MHz, Fs = 20.00 MHz	SINAD		 42 42 42 41 41 41 37		 db db db db db db db

Table 8. AC Characteristics *(2 of 3)*

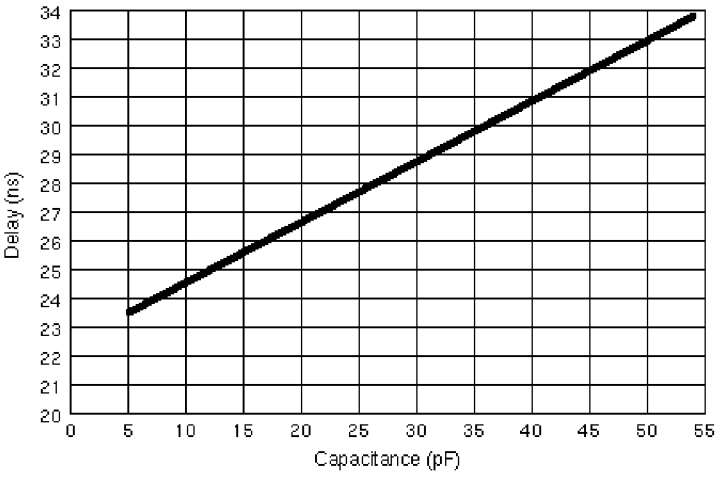
Parameter	Symbol	Min	Typ	Max	Units
Total Harmonic Distortion	TDH				
Fin = 4.20 MHz, Fs = 12.27 MHz			47		db
Fin = 4.20 MHz, Fs = 13.50 MHz			47		db
Fin = 4.20 MHz, Fs = 14.32 MHz			47		db
Fin = 5.75 MHz, Fs = 13.50 MHz			47		db
Fin = 5.75 MHz, Fs = 14.75 MHz			47		db
Fin = 5.75 MHz, Fs = 17.72 MHz			47		db
Fin = 10.0 MHz, Fs = 20.00 MHz			44		db
Spurious Free Dynamic Range	SFDR				
Fin = 4.20 MHz, Fs = 12.27 MHz			50		db
Fin = 4.20 MHz, Fs = 13.50 MHz			50		db
Fin = 4.20 MHz, Fs = 14.32 MHz			50		db
Fin = 5.75 MHz, Fs = 13.50 MHz			50		db
Fin = 5.75 MHz, Fs = 14.75 MHz			50		db
Fin = 5.75 MHz, Fs = 17.72 MHz			50		db
Fin = 10.0 MHz, Fs = 20.00 MHz			47		db
Analog Multiplexer Crosstalk					
All-Hostile Crosstalk *(Figure 8)*			-50		db
Single-Channel Crosstalk *(Figure 9)*			-50		db
Adjacent-Input Crosstalk *(Figure 10)*			-50		db
Differential Gain Error *(5)*	DG		2		%
Differential Phase Error *(5)*	DP		1		Degree
Supply Current *(6)* (Excluding REF+)	IAA		120	185	mA
A0, A1 Setup Time	11	10			ns
A0, A1 Hold Time	12	10			ns

Table 8. AC Characteristics *(3 of 3)*

Parameter	Symbol	Min	Typ	Max	Units
RD*, WR* High Time	13	50			ns
RD* Asserted to Data Bus Driven	14	1			ns
RD* Asserted to Data Valid	15			40	ns
RD* Negated to Data Bus 3-Stated	16			20	ns
WR* Low Time	17	70			ns
Write Data Setup Time	18	10			ns
Write Data Hold Time	19	10			ns
Pipeline Delay (7)		3	3	3	Clocks

Notes: (1). The number of clock cycles that ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
(2). For full-scale step input, full accuracy is attained in specified time.
(3). Time to recover to full accuracy after a > 1.2 V input signal.
(4). Time to recover to full accuracy following a zero cycle.
(5). 4x NTSC subcarrier, unlocked.
(6). IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, and Fs = 14.32 MHz, TCASE = Ambient.
IAA (max) at VAA = 5.25 V, Fin = 10 MHz, and Fs = 20 MHz, TCASE = 0° C.
(7). Pipeline delay is defined as discrete clock period delays in addition to the half-cycle analog sampling delay.
8. Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0–3 V with input rise/fall times ≤ 4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 1.5 V for digital inputs and outputs. D0–D7, P0–P7, CSYNC* output load ≤ 40 pF. VOUT, IOUT0, IOUT1 output load ≤ 40 pF. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V. See timing waveforms (Figures 11 and 12).

Figure 8. Bt252KPJ Output Delay vs. Capacitive Loading



Note: Nominal device at ambient, timing reference points = 1.4 V

Test Circuits

Figure 9. All-Hostile Crosstalk Test Circuit

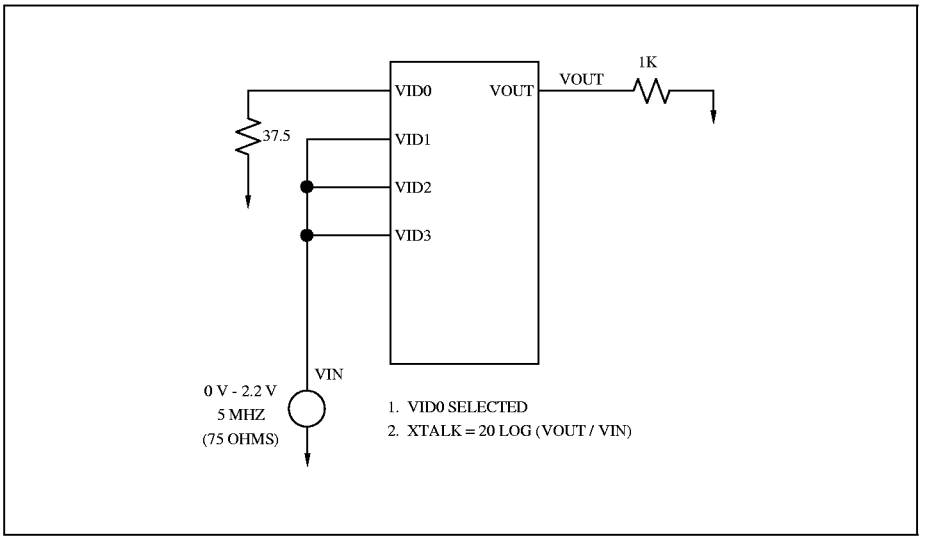


Figure 10. Single-Channel Crosstalk Test Circuit

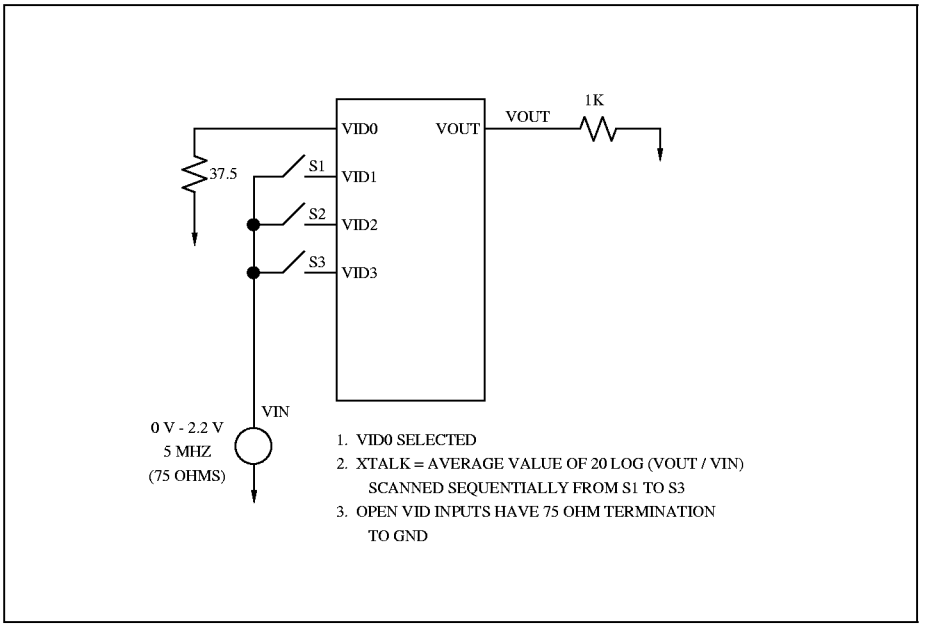
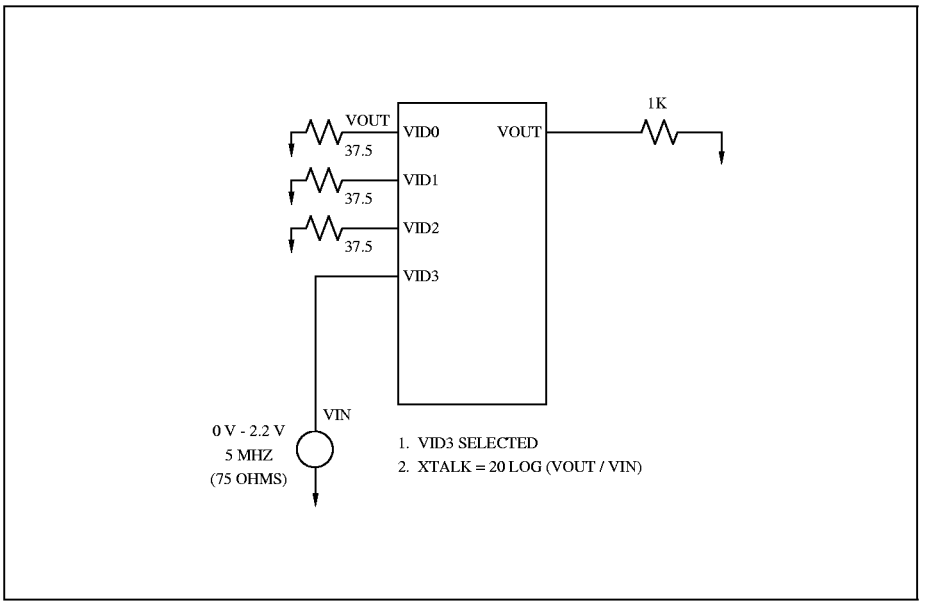


Figure 11. Adjacent-Input Crosstalk Test Circuit



Timing Waveforms

Figure 12. MPU Read/White Timing

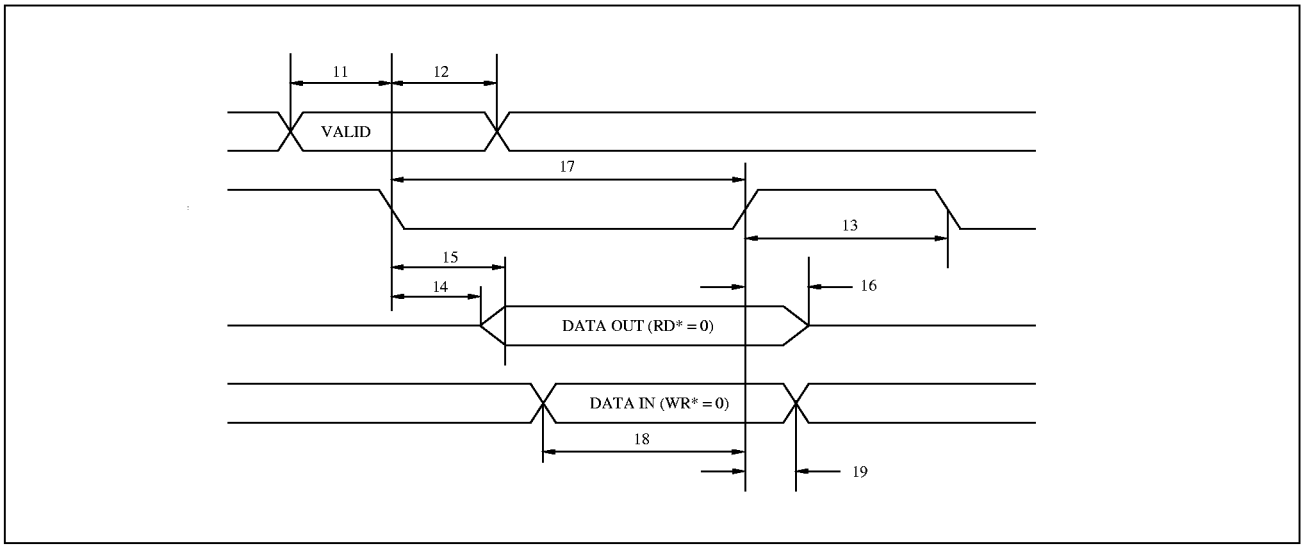
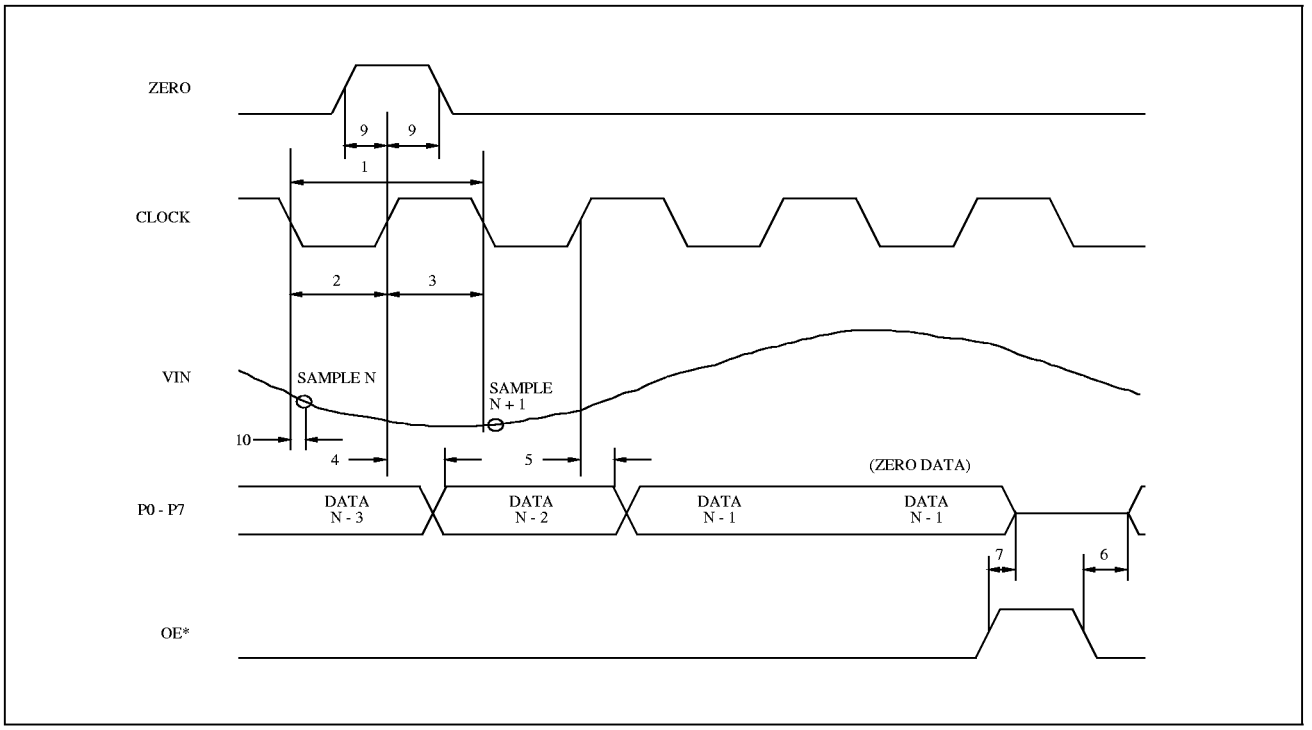
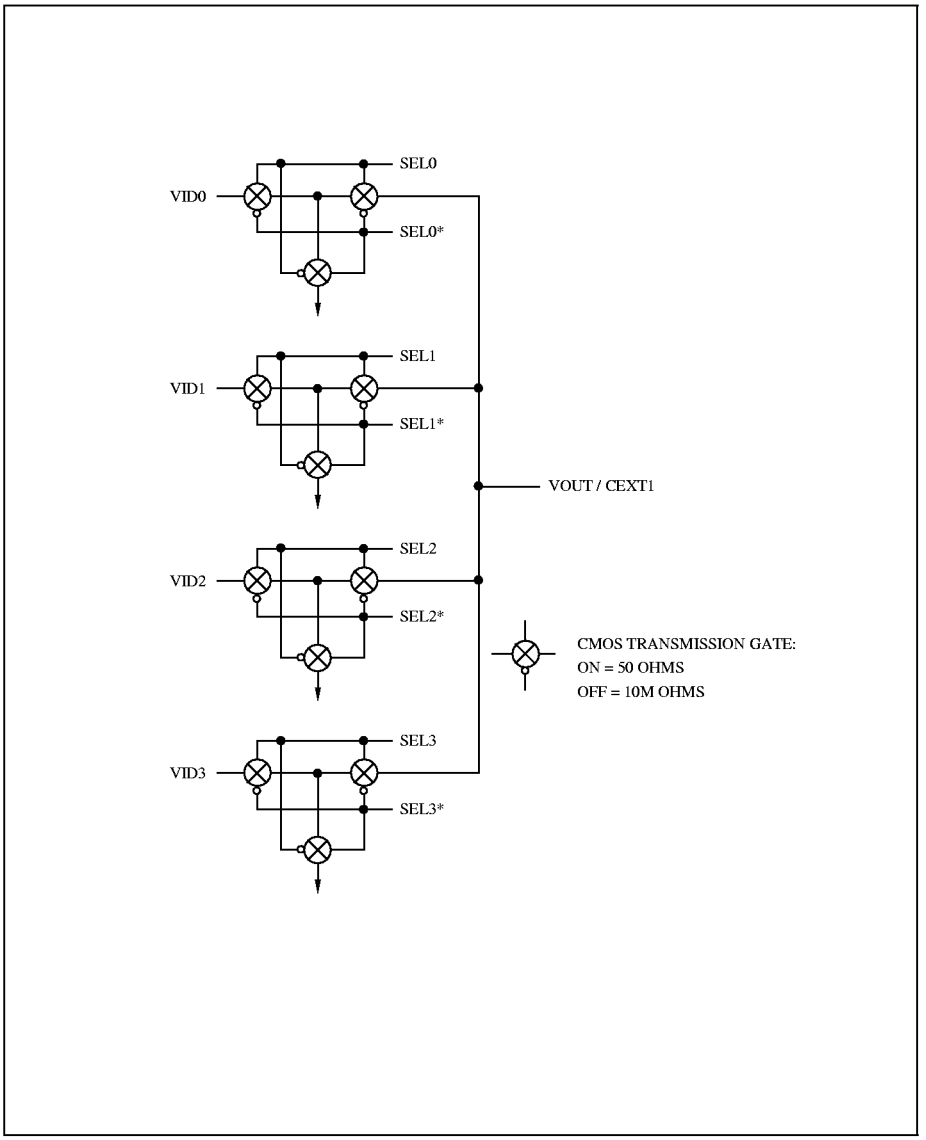


Figure 13. Video Input/Output Timing



Analog Multiplexer Circuit



Revision History

Table 9. Bt252 Datasheet Revision History

Revision	Date	Description

littlediode
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