

Smart High-Side Power Switch

Two Channels: 2 x 30mΩ

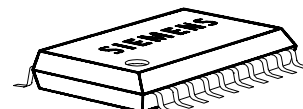
Current Sense

Product Summary

Operating Voltage	$V_{bb(on)}$	5.0...34V	
Active channels		one	two parallel
On-state Resistance	R_{ON}	30mΩ	15mΩ
Nominal load current	$I_{L(NOM)}$	5.5A	8.5A
Current limitation	$I_{L(SCr)}$	24A	24A

Package

P-DSO-20-9



General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input, diagnostic feedback and proportional load current sense monolithically integrated in Smart SiPMOS® technology.
- Providing embedded protective functions

Applications

- μ C compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

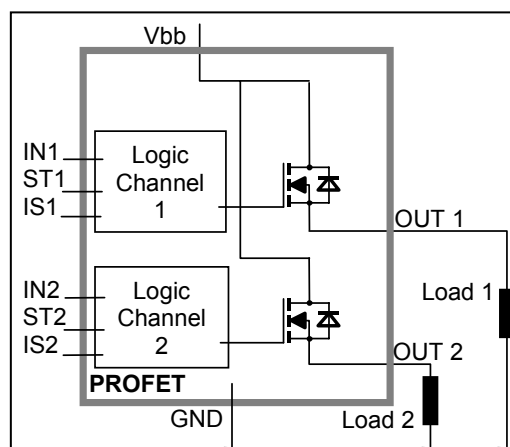
- CMOS compatible input
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Fast demagnetization of inductive loads
- Logic ground independent from load ground

Protection Functions

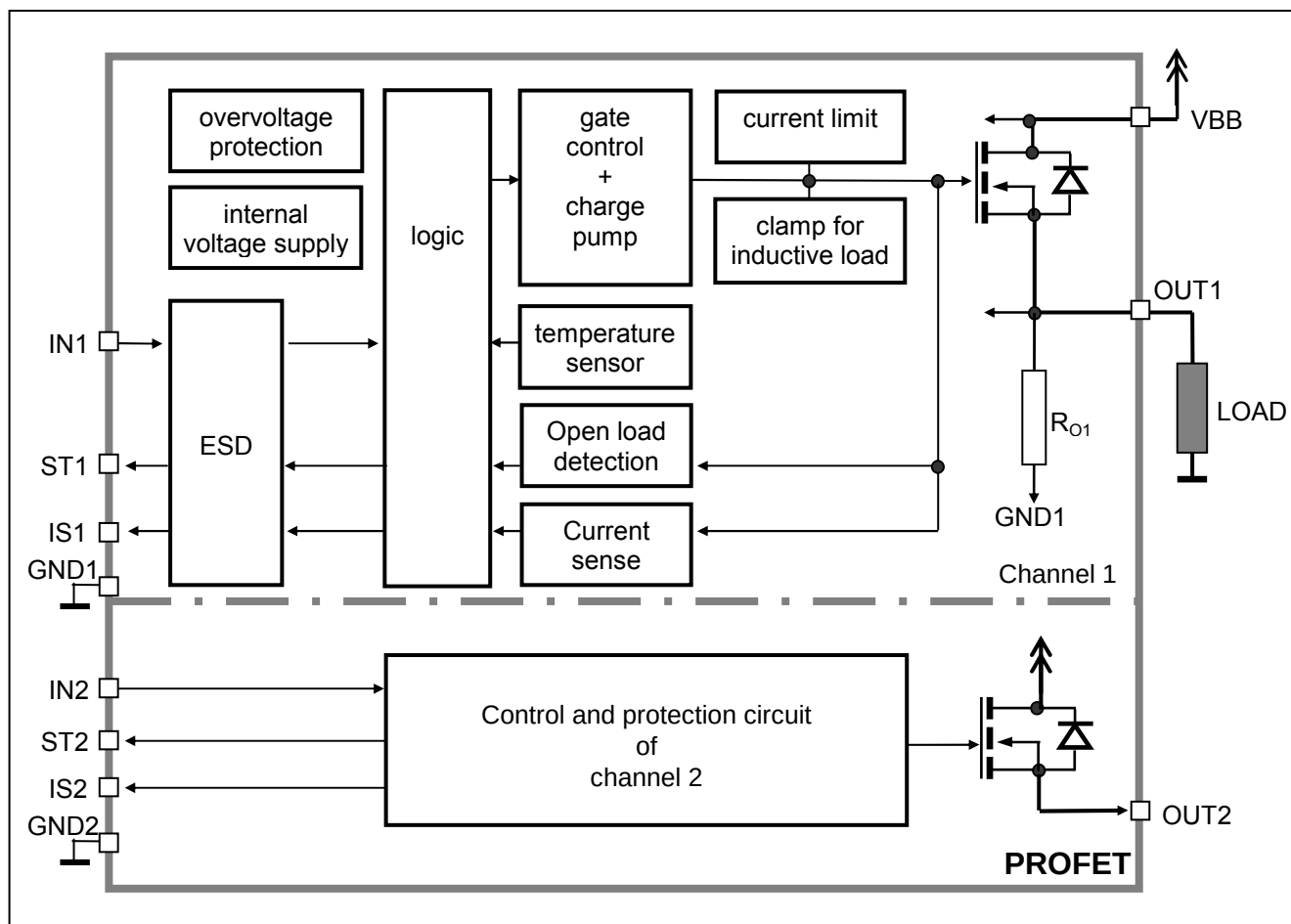
- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Proportional load current sense
- Diagnostic feedback with open drain output
- Open load detection in OFF-state with external resistor
- Feedback of thermal shutdown in ON-state



Functional diagram



Pin Definitions and Functions

Pin	Symbol	Function
1,10,11,12,15,16,19,20	V_{bb}	Positive power supply voltage. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	Input 1,2 , activates channel 1,2 in case of logic high signal
7	IN2	
17,18	OUT1	Output 1,2 , protected high-side power output of channel 1,2. Both pins of each output have to be connected in parallel for operation according this spec (e.g. k_{TjIS}). Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	Diagnostic feedback 1,2 of channel 1,2, open drain, invers to input level
8	ST2	
2	GND1	Ground 1 of chip 1 (channel 1)
6	GND2	Ground 2 of chip 2 (channel 2)
5	IS1	Sense current output 1,2 ; proportional to the load current, zero in the case of current limitation of the load current
9	IS2	

Pin configuration

(top view)

V_{bb}	1	20	V_{bb}
GND1	2	19	V_{bb}
IN1	3	18	OUT1
ST1	4	17	OUT1
IS1	5	16	V_{bb}
GND2	6	15	V_{bb}
IN2	7	14	OUT2
ST2	8	13	OUT2
IS2	9	12	V_{bb}
V_{bb}	10	11	V_{bb}

Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 5)	V_{bb}	43	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150^\circ\text{C}$	V_{bb}	34	V
Load current (Short-circuit current, see page 5)	I_L	self-limited	A
Load dump protection ¹⁾ $V_{LoadDump} = V_A + V_S$, $V_A = 13.5\text{ V}$ $R_l^{2)} = 2\ \Omega$, $t_d = 200\text{ ms}$; IN = low or high, each channel loaded with $R_L = 7.0\ \Omega$,	$V_{Load\ dump}^{3)}$	60	V
Operating temperature range	T_j	$-40 \dots +150$	$^\circ\text{C}$
Storage temperature range	T_{stg}	$-55 \dots +150$	$^\circ\text{C}$
Power dissipation (DC) ⁴⁾ (all channels active)	$T_a = 25^\circ\text{C}$: $T_a = 85^\circ\text{C}$: P_{tot}	3.8 2.0	W
Maximal switchable inductance, single pulse $V_{bb} = 12\text{V}$, $T_{j,start} = 150^\circ\text{C}^{4)}$, $I_L = 5.5\text{ A}$, $E_{AS} = 370\text{ mJ}$, $0\ \Omega$ one channel: $I_L = 8.5\text{ A}$, $E_{AS} = 790\text{ mJ}$, $0\ \Omega$ two parallel channels: see diagrams on page 10	Z_L	18 16	mH
Electrostatic discharge capability (ESD) (Human Body Model) IN: ST, IS: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 $R=1.5\text{k}\Omega$; $C=100\text{pF}$	V_{ESD}	1.0 4.0 8.0	kV
Input voltage (DC)	V_{IN}	$-10 \dots +16$	V
Current through input pin (DC)	I_{IN}	± 2.0	mA
Current through status pin (DC)	I_{ST}	± 5.0	
Current through current sense pin (DC) see internal circuit diagram page 9	I_{IS}	± 14	

Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	Max	
Thermal resistance junction - soldering point ^{4),5)} each channel:	R_{thjs}	--	--	12	K/W
junction - ambient ⁴⁾ one channel active:	R_{thja}	--	40	--	
all channels active:		--	33	--	

1) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a $150\ \Omega$ resistor for the GND connection is recommended).

2) R_l = internal resistance of the load dump test pulse generator

3) $V_{Load\ dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

4) Device on $50\text{mm} \times 50\text{mm} \times 1.5\text{mm}$ epoxy PCB FR4 with 6cm^2 (one layer, $70\ \mu\text{m}$ thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

5) Soldering point: upper side of solder edge of device pin 15. See page 15

Electrical Characteristics

Parameter and Conditions, each of the two channels at $T_j = -40...+150^{\circ}\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

Load Switching Capabilities and Characteristics

On-state resistance (V_{bb} to OUT); $I_L = 5\text{ A}$ each channel, $T_j = 25^{\circ}\text{C}$: $T_j = 150^{\circ}\text{C}$: two parallel channels, $T_j = 25^{\circ}\text{C}$:	R_{ON}	--	27 54 14	30 60 15	$\text{m}\Omega$
Output voltage drop limitation at small load currents, see page 14 $I_L = 0.5\text{ A}$ $T_j = -40...+150^{\circ}\text{C}$:	$V_{ON(NL)}$	--	50	--	mV
Nominal load current one channel active: two parallel channels active: Device on PCB ⁶⁾ , $T_a = 85^{\circ}\text{C}$, $T_j \leq 150^{\circ}\text{C}$	$I_{L(NOM)}$	4.9 7.8	5.5 8.5	--	A
Output current while GND disconnected or pulled up ⁷⁾ ; $V_{bb} = 30\text{ V}$, $V_{IN} = 0$, see diagram page 10	$I_{L(GNDhigh)}$	--	--	8	mA
Turn-on time ⁸⁾ IN  to 90% V_{OUT} :	t_{on}	25	70	150	μs
Turn-off time IN  to 10% V_{OUT} : $R_L = 12\ \Omega$	t_{off}	25	80	200	μs
Slew rate on ⁸⁾ 10 to 30% V_{OUT} , $R_L = 12\ \Omega$:	dV/dt_{on}	0.1	--	1	$\text{V}/\mu\text{s}$
Slew rate off ⁸⁾ 70 to 40% V_{OUT} , $R_L = 12\ \Omega$:	$-dV/dt_{off}$	0.1	--	1	$\text{V}/\mu\text{s}$

Operating Parameters

Operating voltage ⁹⁾	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown	$V_{bb(under)}$	3.2	--	5.0	V
Undervoltage restart $T_j = -40...+25^{\circ}\text{C}$: $T_j = +150^{\circ}\text{C}$:	$V_{bb(u\ rst)}$	--	4.5	5.5 6.0	V
Undervoltage restart of charge pump see diagram page 13 $T_j = -40...+25^{\circ}\text{C}$: $T_j = 150^{\circ}\text{C}$:	$V_{bb(ucp)}$	-- --	4.7 --	6.5 7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.5	--	V
Overvoltage shutdown	$V_{bb(over)}$	34	--	43	V
Overvoltage restart	$V_{bb(o\ rst)}$	33	--	--	V

⁶⁾ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70μm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

⁷⁾ not subject to production test, specified by design

⁸⁾ See timing diagram on page 11.

⁹⁾ At supply voltage increase up to $V_{bb} = 4.7\text{ V}$ typ without charge pump, $V_{OUT} \approx V_{bb} - 2\text{ V}$

Parameter and Conditions, each of the two channels at $T_j = -40...+150^{\circ}\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Overvoltage hysteresis	$\Delta V_{bb(\text{over})}$	--	1	--	V
Overvoltage protection ¹⁰⁾ $I_{bb}=40\text{ mA}$	$V_{bb(\text{AZ})}$	41 43	-- 47	-- 52	V
Standby current ¹¹⁾ $V_{IN} = 0$;	$I_{bb(\text{off})}$	--	8	30	μA
			24	50	
Leakage output current (included in $I_{bb(\text{off})}$) $V_{IN} = 0$	$I_{L(\text{off})}$	--	--	20	μA
Operating current ¹²⁾ , $V_{IN} = 5\text{V}$, $I_{GND} = I_{GND1} + I_{GND2}$, one channel on: two channels on:	I_{GND}	--	1.2	3	mA
			2.4	6	

Protection Functions¹³⁾

Current limit, (see timing diagrams, page 12) $T_j = -40^{\circ}\text{C}$: $T_j = 25^{\circ}\text{C}$: $T_j = +150^{\circ}\text{C}$:	$I_{L(\text{lim})}$	48 40 31	56	65	A
			50	58	
			37	45	
			--	--	
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 12)	$I_{L(\text{SCr})}$	--	24	--	A
			24	--	
Initial short circuit shutdown time (see timing diagrams on page 12) $T_{j,\text{start}} = 25^{\circ}\text{C}$:	$t_{\text{off}(\text{SC})}$	--	2.0	--	ms
Output clamp (inductive load switch off) ¹⁴⁾ at $V_{ON(\text{CL})} = V_{bb} - V_{OUT}$, $I_L = 40\text{ mA}$ $T_j = -40^{\circ}\text{C}$: $T_j = 25^{\circ}\text{C}...150^{\circ}\text{C}$:	$V_{ON(\text{CL})}$	41 43	-- 47	-- 52	V
		--	--	--	
Thermal overload trip temperature	T_{jt}	150	--	--	$^{\circ}\text{C}$
Thermal hysteresis	ΔT_{jt}	--	10	--	K

¹⁰⁾ Supply voltages higher than $V_{bb(\text{AZ})}$ require an external current limit for the GND and status pins (a $150\ \Omega$ resistor in the GND connection is recommended). See also $V_{ON(\text{CL})}$ in table of protection functions and circuit diagram page 9.

¹¹⁾ Measured with load; for the whole device; all channels off

¹²⁾ Add I_{ST} , if $I_{ST} > 0$

¹³⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

¹⁴⁾ If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(\text{CL})}$

Parameter and Conditions, each of the two channels at $T_j = -40...+150^{\circ}\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

Reverse Battery

Reverse battery voltage ¹⁵⁾	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ($V_{out} > V_{bb}$) $I_L = -4.0\text{ A}$, $T_j = +150^{\circ}\text{C}$	$-V_{ON}$	--	600	--	mV

Diagnostic Characteristics

Current sense ratio ¹⁶⁾ , static on-condition, $V_{IS} = 0...5\text{ V}$, $V_{bb(on)} = 6.5^{17)}...27\text{ V}$, $k_{ILIS} = I_L / I_{IS}$ $T_j = -40^{\circ}\text{C}$, $I_L = 5\text{ A}$: $T_j = -40^{\circ}\text{C}$, $I_L = 0.5\text{ A}$: $T_j = 25...+150^{\circ}\text{C}$, $I_L = 5\text{ A}$: $T_j = 25...+150^{\circ}\text{C}$, $I_L = 0.5\text{ A}$:	k_{ILIS}	4350 3100 4350 3800	4800 4800 4800 4800	5800 7800 5350 6300	
Current sense output voltage limitation $T_j = -40...+150^{\circ}\text{C}$ $I_{IS} = 0$, $I_L = 5\text{ A}$:	$V_{IS(lim)}$	5.4	6.1	6.9	V
Current sense leakage/offset current $T_j = -40...+150^{\circ}\text{C}$ $V_{IN}=0$, $V_{IS} = 0$, $I_L = 0$: $V_{IN}=5\text{ V}$, $V_{IS} = 0$, $I_L = 0$: $V_{IN}=5\text{ V}$, $V_{IS} = 0$, $V_{OUT} = 0$ (short circuit)	$I_{IS(LL)}$ $I_{IS(LH)}$ $I_{IS(SH)}^{18)}$	0 0 0	-- -- --	1 15 10	μA
Current sense settling time to $I_{IS\text{ static}} \pm 10\%$ after positive input slope ¹⁸⁾ , $I_L = 0 \rightarrow 5\text{ A}$	$t_{son(IS)}$	--	--	300	μs
Current sense settling time to 10% of $I_{IS\text{ static}}$ after negative input slope ¹⁸⁾ , $I_L = 5 \rightarrow 0\text{ A}$	$t_{soff(IS)}$	--	30	100	μs
Current sense rise time (60% to 90%) after change of load current ¹⁸⁾ $I_L = 2.5 \rightarrow 5\text{ A}$	$t_{slc(IS)}$	--	10	--	μs
Open load detection voltage ¹⁹⁾ (off-condition)	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (pin 17,18 to 2 resp. 13,14 to 6), $V_{OUT}=5\text{ V}$	R_O	5	15	40	$\text{k}\Omega$

¹⁵⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 9).

¹⁶⁾ This range for the current sense ratio refers to all devices. The accuracy of the k_{ILIS} can be raised at least by a factor of two by matching the value of k_{ILIS} for every single device.
In the case of current limitation the sense current I_{IS} is zero and the diagnostic feedback potential V_{ST} is High. See figure 2c, page 12.

¹⁷⁾ Valid if $V_{bb(u\text{ rst})}$ was exceeded before.

¹⁸⁾ not subject to production test, specified by design

¹⁹⁾ External pull up resistor required for open load detection in off state.

Parameter and Conditions, each of the two channels at $T_j = -40...+150^{\circ}\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

Input and Status Feedback²⁰⁾

Input resistance (see circuit page 9)	R_I	3.0	4.5	7.0	$\text{k}\Omega$
Input turn-on threshold voltage 	$V_{IN(T+)}$	--	--	3.5	V
Input turn-off threshold voltage 	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current $V_{IN} = 0.4\text{ V}$:	$I_{IN(off)}$	1	--	50	μA
On state input current $V_{IN} = 5\text{ V}$:	$I_{IN(on)}$	20	50	90	μA
Delay time for status with open load after Input neg. slope (see diagram page 13)	$t_{d(ST\ OL3)}$	--	400	--	μs
Status delay after positive input slope (not subject to production test, specified by design)	$t_{don(ST)}$	--	13	--	μs
Status delay after negative input slope (not subject to production test, specified by design)	$t_{doff(ST)}$	--	1	--	μs
Status output (open drain)					
Zener limit voltage $T_j = -40...+150^{\circ}\text{C}$, $I_{ST} = +1.6\text{ mA}$:	$V_{ST(high)}$	5.4	6.1	6.9	V
ST low voltage $T_j = -40...+25^{\circ}\text{C}$, $I_{ST} = +1.6\text{ mA}$:	$V_{ST(low)}$	--	--	0.4	
$T_j = +150^{\circ}\text{C}$, $I_{ST} = +1.6\text{ mA}$:		--	--	0.7	
Status leakage current, $V_{ST} = 5\text{ V}$, $T_j = 25...+150^{\circ}\text{C}$:	$I_{ST(high)}$	--	--	2	μA

²⁰⁾ If ground resistors R_{GND} are used, add the voltage drop across these resistors.

Truth Table

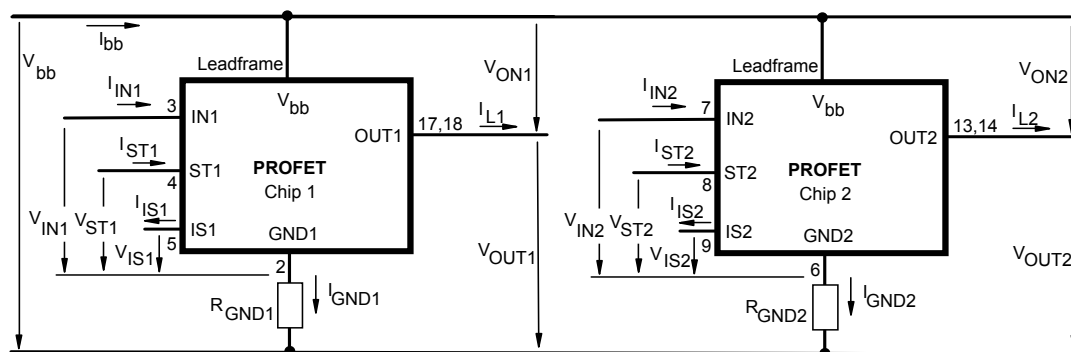
	Input 1	Output 1	Status 1	Current Sense 1
	Input 2	Output 2	Status 2	Current Sense 2
	level	level	level	I_{IS}
Normal operation	L	L	H	0
	H	H	L	nominal
Current-limitation	L	L	H	0
	H	H	H	0
Short circuit to GND	L	L	H	0
	H	L ²¹⁾	H	0
Over-temperature	L	L	H	0
	H	L	H	0
Short circuit to V_{bb}	L	H	L ²²⁾	0
	H	H	L	<nominal ²³⁾
Open load	L	L ²⁴⁾	H (L ²⁵⁾	0
	H	H	L	0
Undervoltage	L	L	H	0
	H	L	L	0
Overvoltage	L	L	H	0
	H	L	L	0
Negative output voltage clamp	L	L	H	0

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit

H = "High" Level Status signal after the time delay shown in the diagrams (see fig 5. page 13)

Parallel switching of channel 1 and 2 is possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor. The current sense outputs IS1 and IS2 have to be connected with a single pull-down resistor.

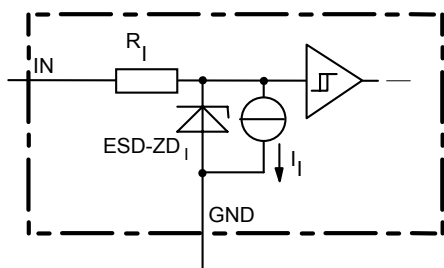
Terms



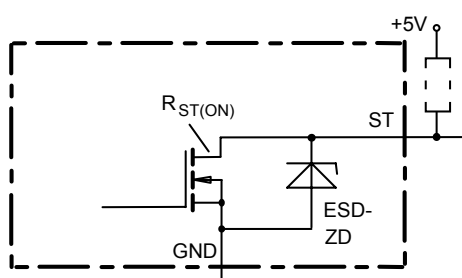
Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20

External R_{GND} optional; two resistors R_{GND1} , $R_{GND2} = 150 \Omega$ or a single resistor $R_{GND} = 75 \Omega$ for reverse battery protection up to the max. operating voltage.

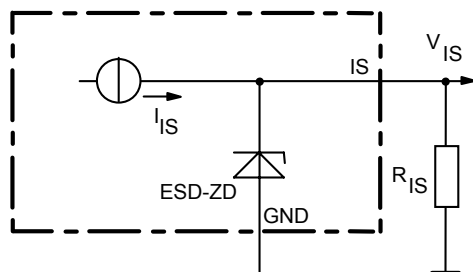
- 21) The voltage drop over the power transistor is $V_{bb} - V_{OUT} > 3V$ typ. Under this condition the sense current I_{IS} is zero
- 22) An external short of output to V_{bb} , in the off state, causes an internal current from output to ground. If R_{GND} is used, an offset voltage at the GND and ST pins will occur and the $V_{ST\ low}$ signal may be errorious.
- 23) Low ohmic short to V_{bb} may reduce the output current I_L and therefore also the sense current I_{IS} .
- 24) Power Transistor off, high impedance
- 25) with external resistor between V_{BB} and OUT

Input circuit (ESD protection), IN1 or IN2


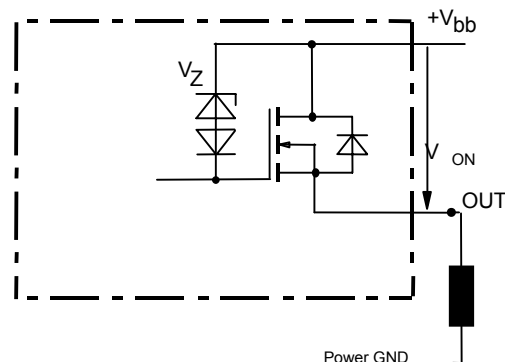
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Status output, ST1 or ST2


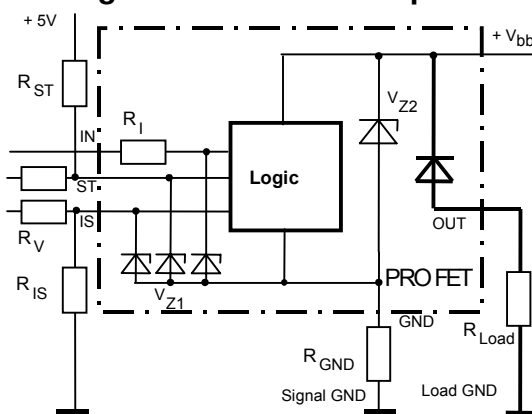
ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)} < 375 \Omega$ at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Current sense output


ESD-Zener diode: 6.1 V typ., max 14 mA; $R_{IS} = 1 \text{ k}\Omega$ nominal

Inductive and overvoltage output clamp, OUT1 or OUT2


V_{ON} clamped to $V_{ON(CL)} = 47 \text{ V typ.}$

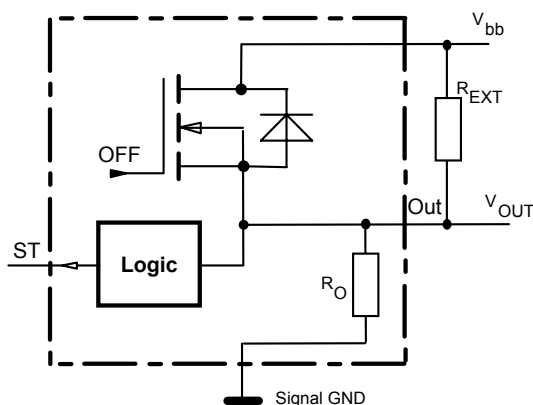
Overvoltage and reverse batt. protection


$V_{Z1} = 6.1 \text{ V typ.}$, $V_{Z2} = 47 \text{ V typ.}$, $R_{GND} = 150 \Omega$, $R_{ST} = 15 \text{ k}\Omega$, $R_I = 4.5 \text{ k}\Omega$ typ., $R_{IS} = 1 \text{ k}\Omega$, $R_V = 15 \text{ k}\Omega$. In case of reverse battery the current has to be limited by the load. Temperature protection is not active

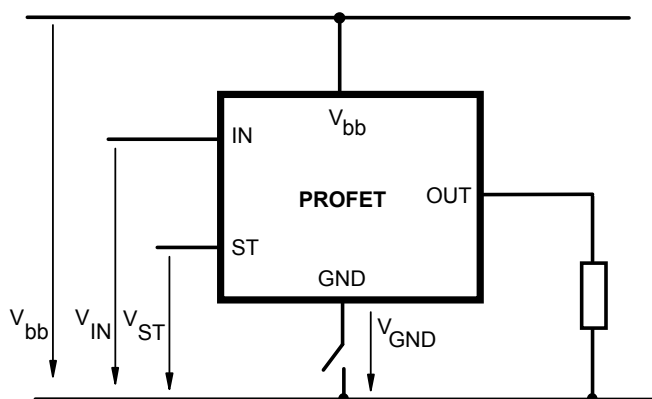
Open-load detection OUT1 or OUT2

OFF-state diagnostic condition:

$V_{OUT} > 3 \text{ V typ.}$; IN low

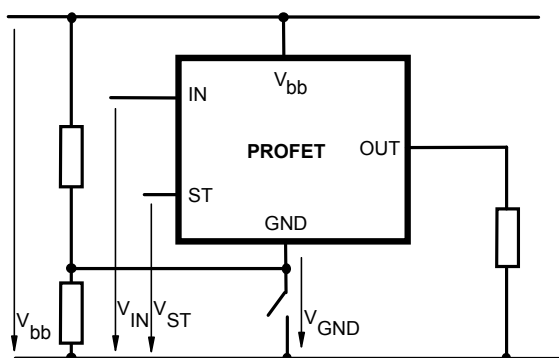


GND disconnect



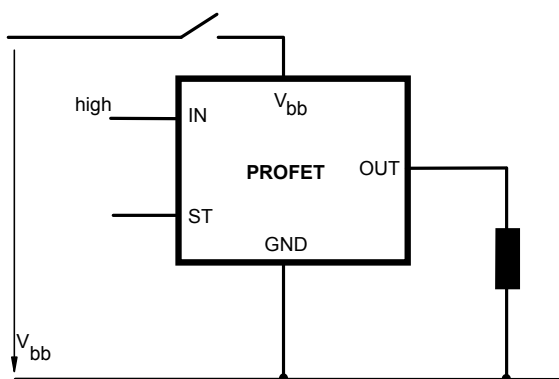
Any kind of load. In case of $I_N = \text{high}$ is $V_{OUT} \approx V_{IN} - V_{IN}(T+)$.
Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN}(T+)$ device stays off
Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

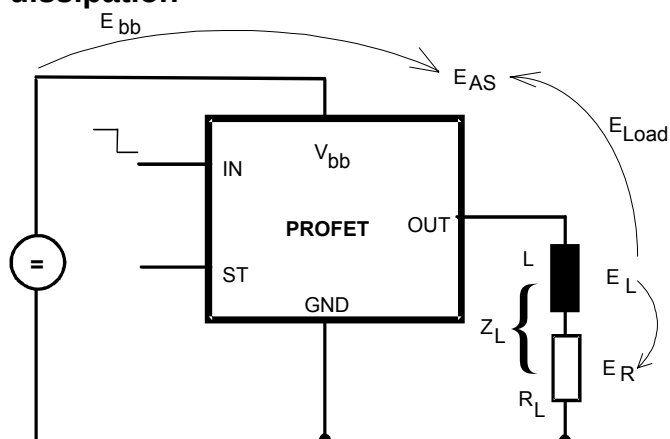
V_{bb} disconnect with energized inductive load



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 10) each switch is protected against loss of V_{bb} .

Consider at your PCB layout that in the case of V_{bb} disconnection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

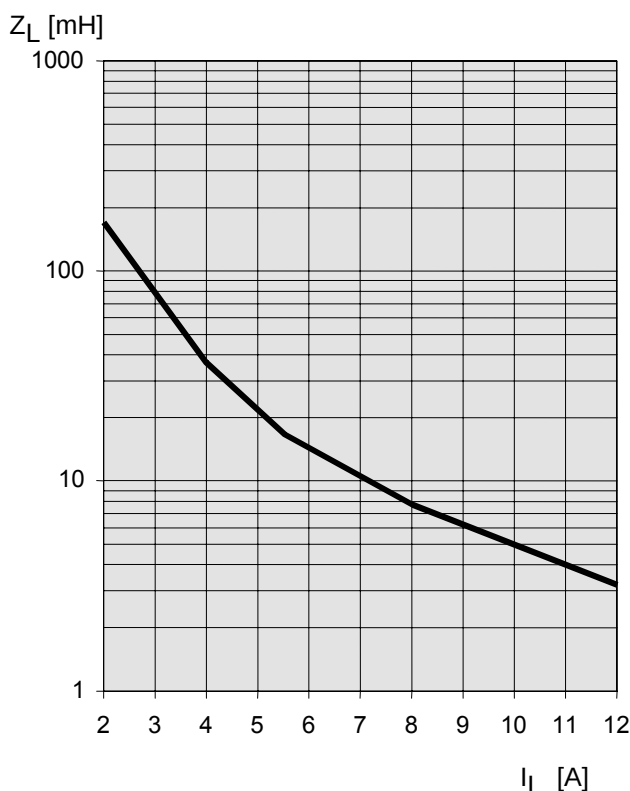
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for $R_L > 0 \Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

Maximum allowable load inductance for a single switch off (one channel)⁴⁾

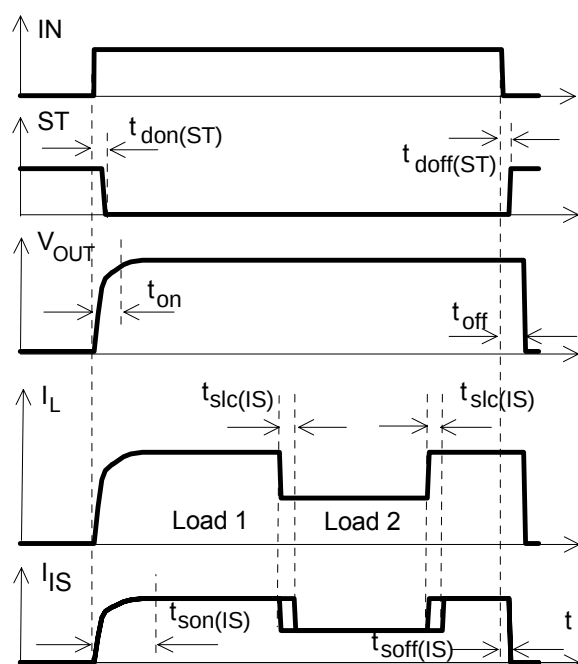
$$L = f(I_L); T_{j,start} = 150^\circ\text{C}, V_{bb} = 12\text{ V}, R_L = 0 \Omega$$



Timing diagrams

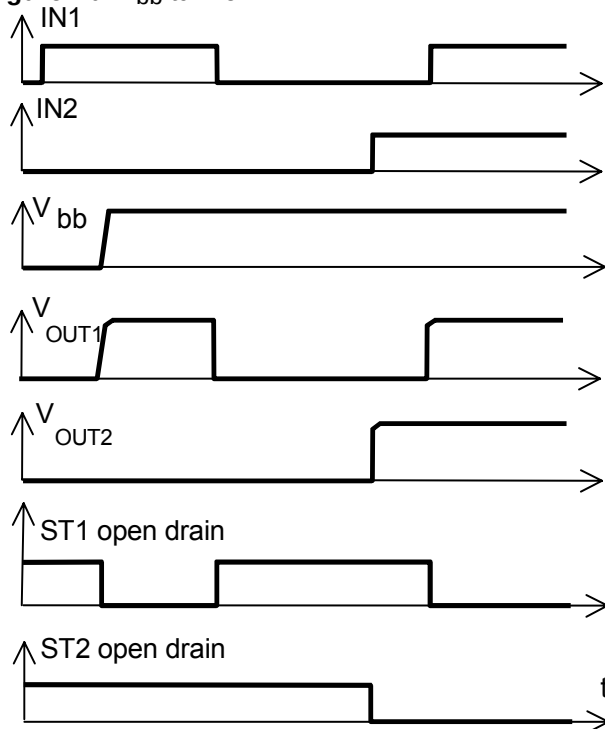
Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: Switching a resistive load, change of load current in on-condition:



The sense signal is not valid during settling time after turn or change of load current.

Figure 1b: V_{bb} turn on:



proper turn on under all conditions

Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

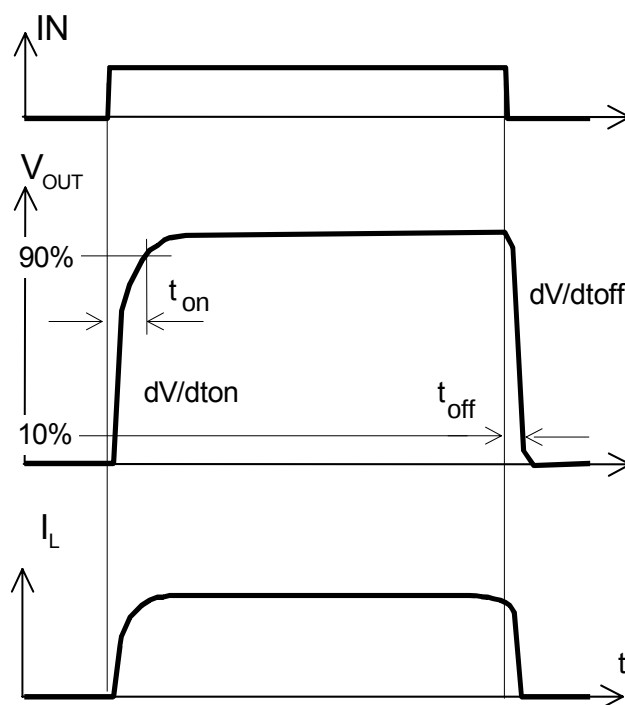


Figure 2b: Switching a lamp:

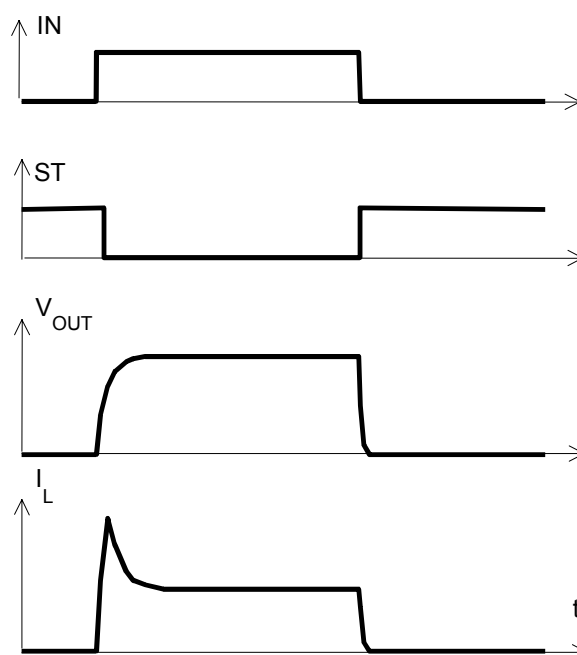
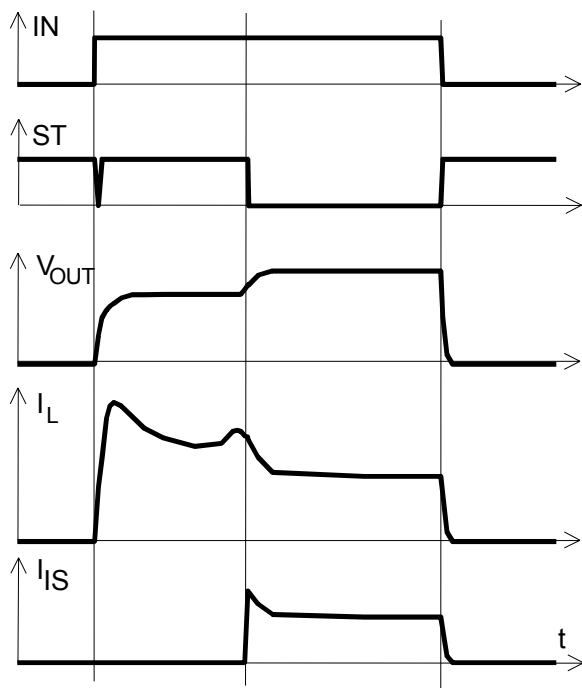
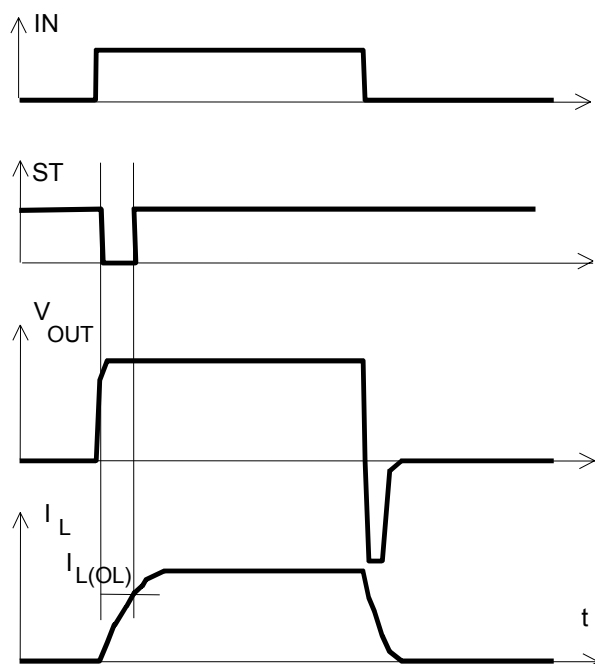
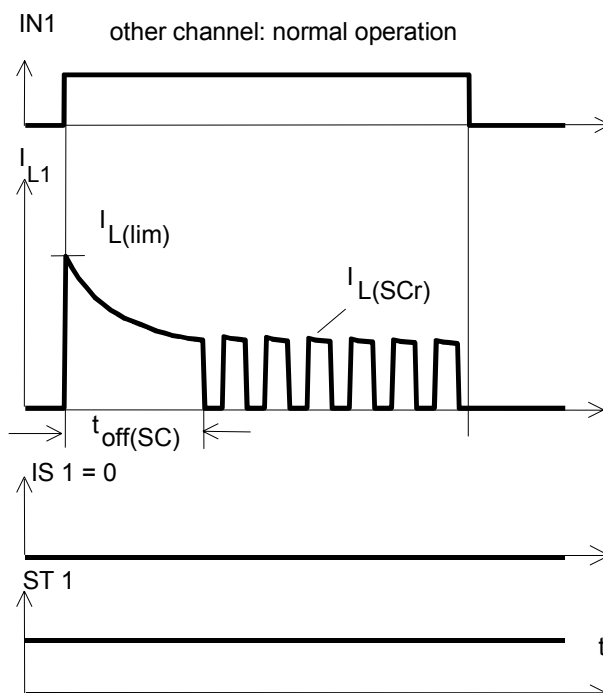
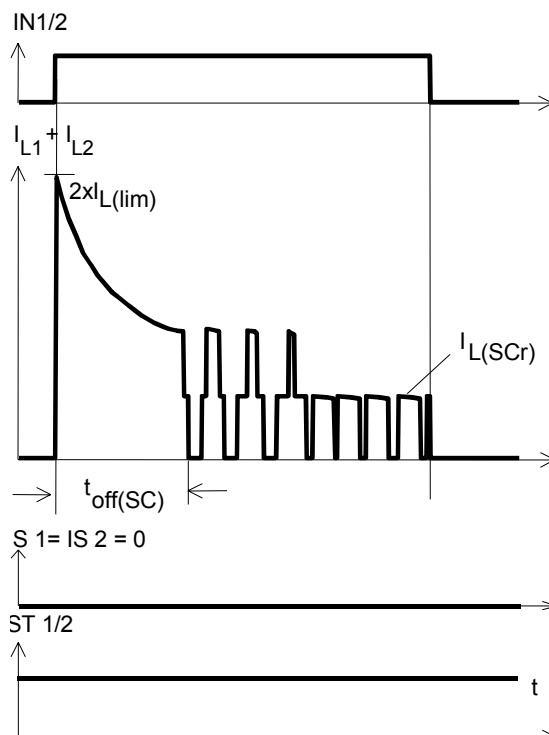


Figure 2c: Switching a lamp with current limit:

Figure 2d: Switching an inductive load


*) if the time constant of load is too large, open-load-status may occur

**Figure 3a: Turn on into short circuit:
shut down by overtemperature, restart by cooling**


Heating up of the chip may require several milliseconds, depending on external conditions

**Figure 3b: Turn on into short circuit:
shut down by overtemperature, restart by cooling
(two parallel switched channels 1 and 2)**


ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature:
Reset if $T_J < T_{jt}$

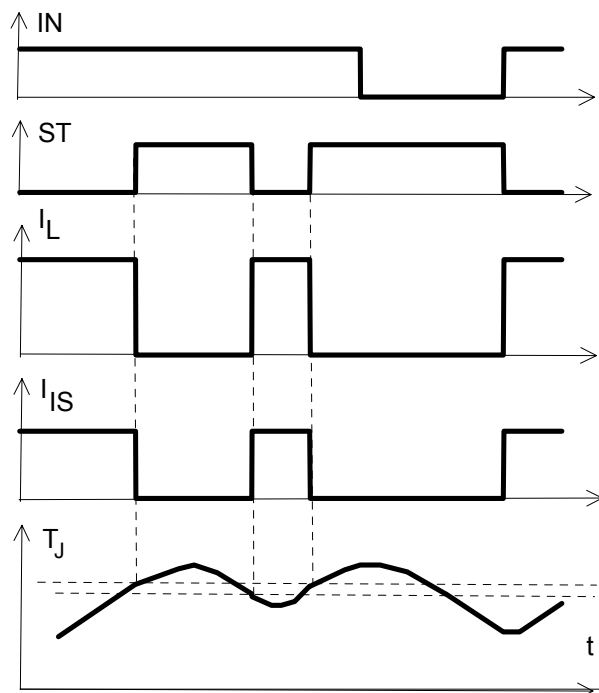


Figure 5a: Open load: detection (with R_{EXT}),
turn on/off to open load

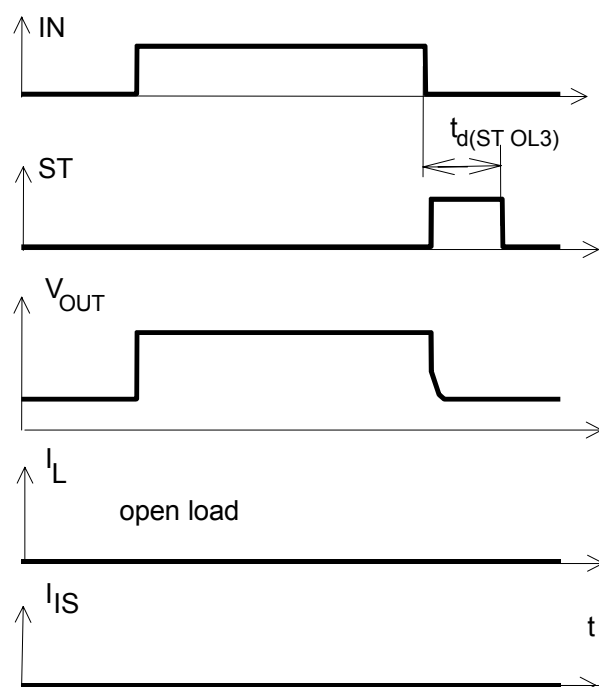


Figure 6a: Undervoltage:

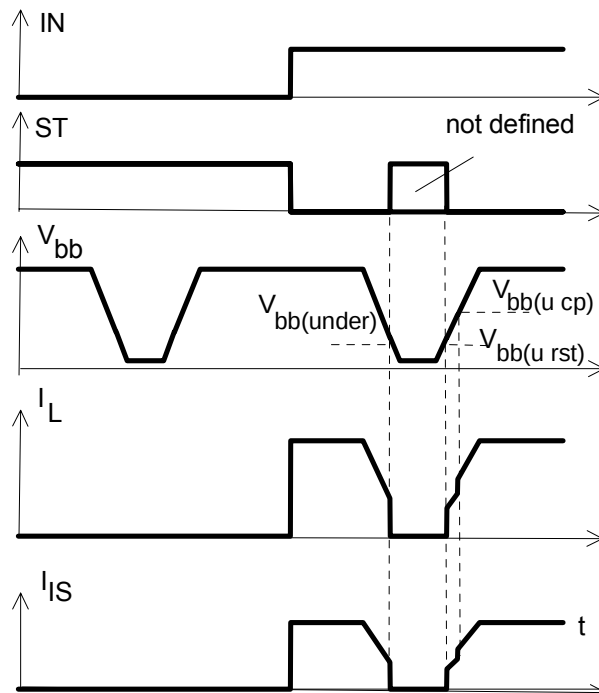
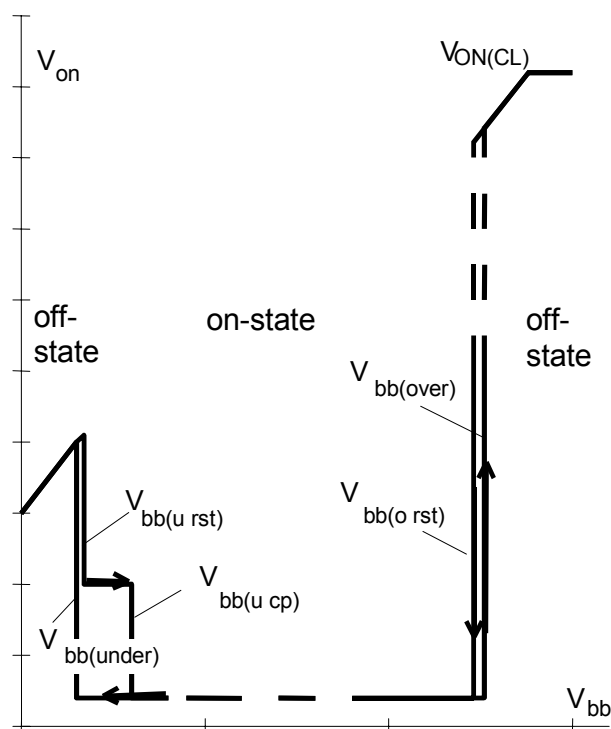
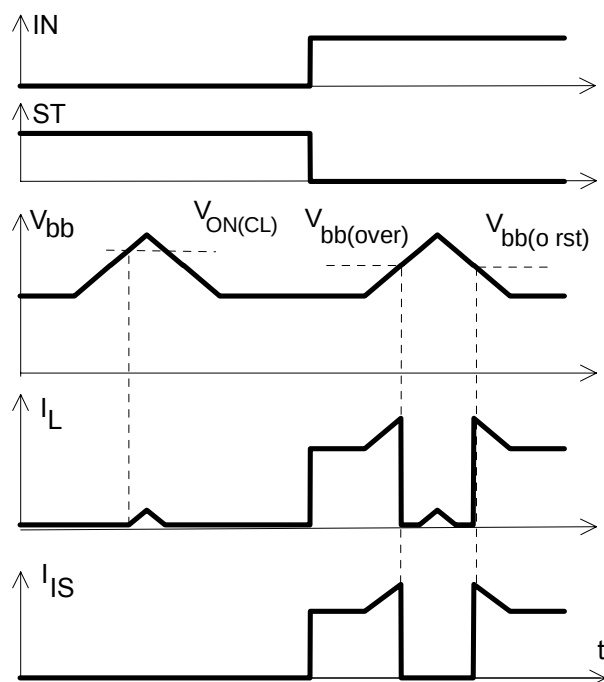
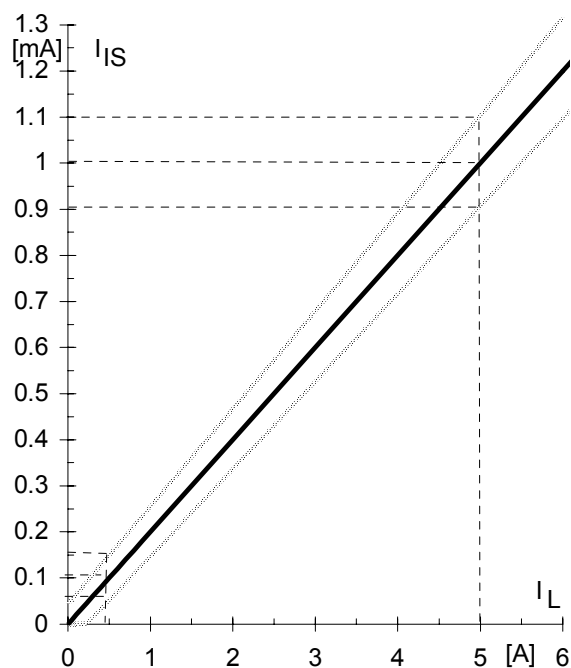


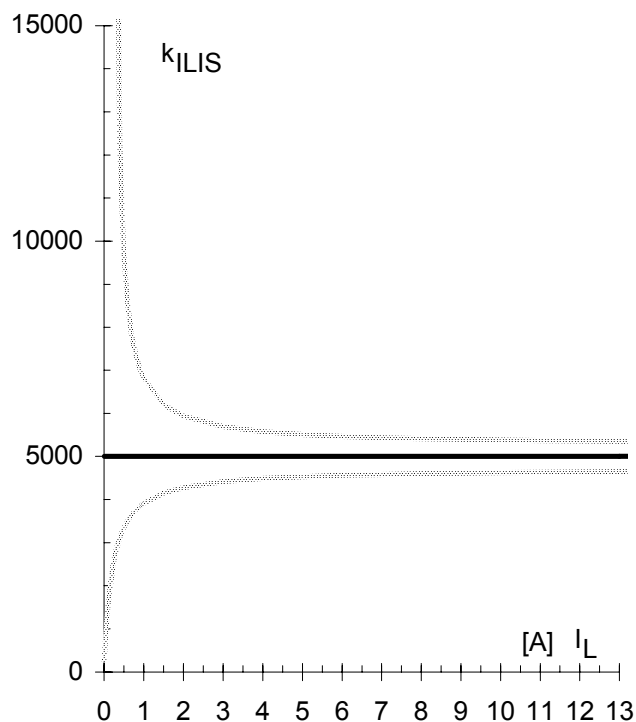
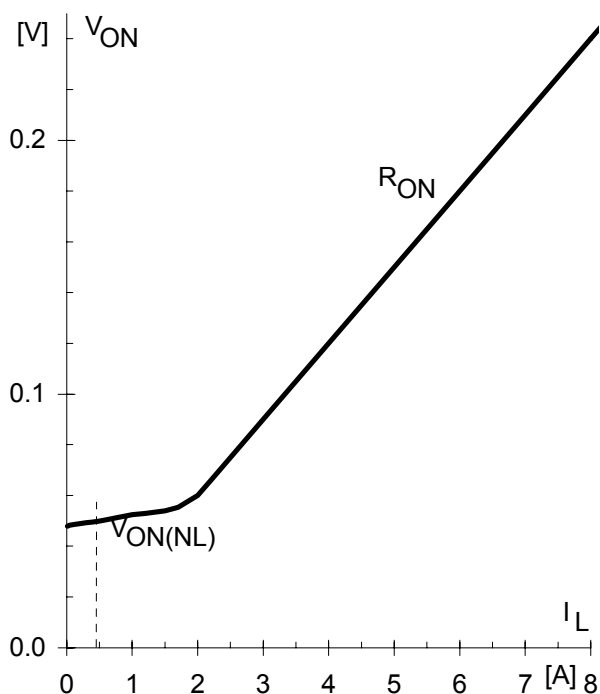
Figure 6b: Undervoltage restart of charge pump



charge pump starts at $V_{bb(ucp)} = 4.7 \text{ V typ.}$

Figure 7a: Overvoltage:

Figure 8a: Current sense versus load current²⁶:


²⁶ This range for the current sense ratio refers to all devices. The accuracy of the k_{ILIS} can be raised at least by a factor of two by matching the value of k_{ILIS} for every single device.

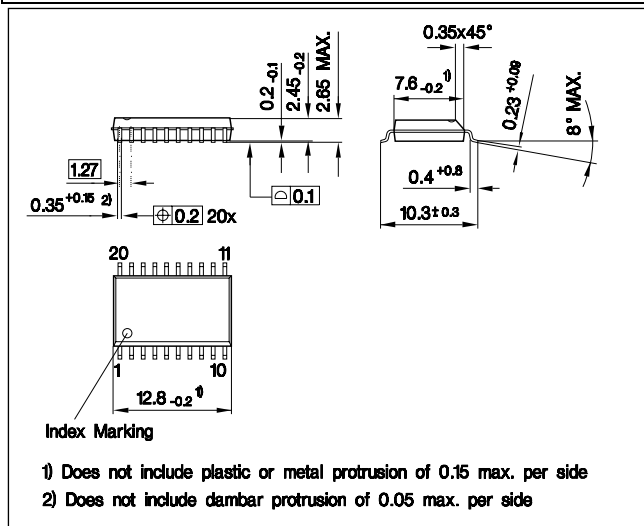
Figure 8b: Current sense ratio:

Figure 9a: Output voltage drop versus load current:


Package and Ordering Code

Standard: P-DSO-20-9

Sales Code	BTS 740 L2
Ordering Code	Q67060-S7012-A2

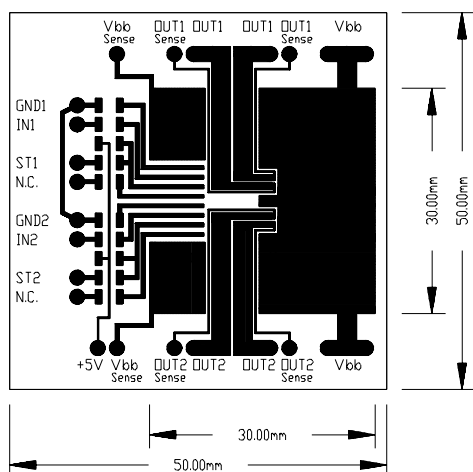
All dimensions in millimetres



Definition of soldering point with temperature T_S :
upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer
70µm, 6cm² active heatsink area) as a reference for
max. power dissipation P_{tot} , nominal load current
 $I_{L(NOM)}$ and thermal resistance R_{thja}



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