

# PLL frequency synthesizer for tuners

## BU2616F

BU2616F PLL frequency synthesizers work up through the FM band.

Featuring low power dissipation and highly sensitive built-in RF amps, they detect intermediate frequencies.

### ●Applications

Tuners (Mini components, radio cassette players, radio equipment, etc.)

### ●Features

- 1) Built-in high-speed prescaler can divide 130MHzVCO.
- 2) Low current dissipation (during operation: 6mA PLL OFF: 1mA)
- 3) In addition to the standard FM and AM, also offers the following 7 frequencies: 25kHz, 12.5kHz, 6.25kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
- 4) SD (station detector) input circuit.
- 5) Intermediate frequency detection circuit
- 6) Charge pump output control circuit
- 7) Four output ports (Nch open drain).
- 8) Serial data input (CE, CK, DA)

### ●Absolute maximum ratings (Ta = 25°C)

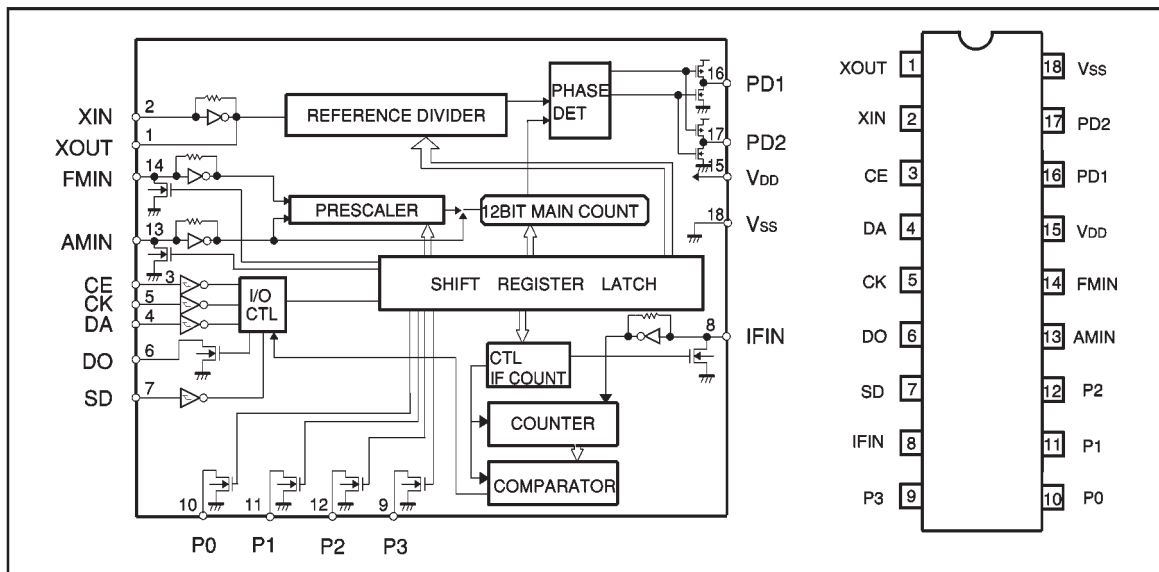
Parameter	Symbol	Limits	Unit	Conditions
Power supply voltage	V <sub>DD</sub>	-0.3~+7.0	V	V <sub>DD</sub>
Maximum input voltage 1	V <sub>IN1</sub>	-0.3~+7.0	V	CE, CK, DA, SD
Maximum input voltage 2	V <sub>IN2</sub>	-0.3~V <sub>DD</sub> +0.3	V	XIN, FMIN, AMIN, IFIN
Maximum output voltage 1	V <sub>OUT1</sub>	-0.3~+10.0	V	P <sub>0</sub> , P <sub>1</sub> , P <sub>2</sub> , P <sub>3</sub> , DO
Maximum output voltage 2	V <sub>OUT2</sub>	-0.3~V <sub>DD</sub> +0.3	V	PD <sub>1</sub> , PD <sub>2</sub> , XOUT
Maximum output current	I <sub>OUT</sub>	0~+3.0	mA	P <sub>0</sub> , P <sub>1</sub> , P <sub>2</sub> , P <sub>3</sub> , DO
Power dissipation	P <sub>d</sub>	450*	mW	
Operating temperature	T <sub>opr</sub>	-10~+75	°C	
Storage temperature	T <sub>stg</sub>	-55~+125	°C	

\* Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

### ●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	4.0~6.0	V

●Block diagram



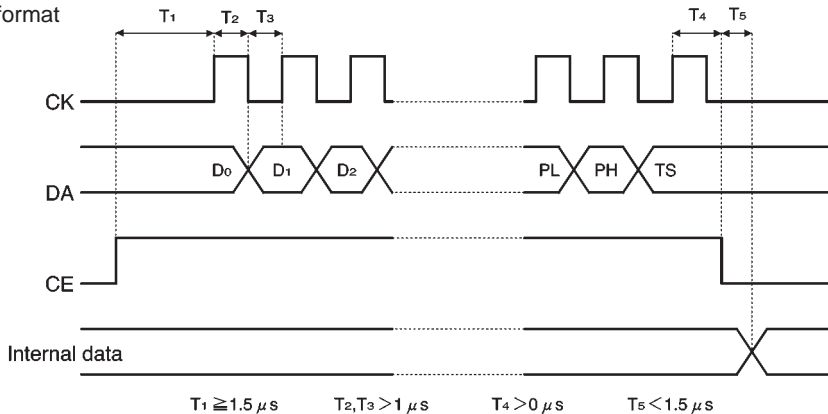
●Pin descriptions

Pin No.	Symbol	Pin name	Function	I/O
1	XOUT	Crystal oscillation	For generation of standard frequency and internal clock.	OUT
2	XIN		Connected to 7.2 MHz crystal resonator.	IN
3	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
4	DA	Serial data		
5	CK	Clock signal		
6	DO	Data out	Comes ON during IF frequency detection or SD detection.	Nch open drain
7	SD	SD input	SD signal is input. Observed by DO terminal.	IN
8	IFIN	IF input	Input is for IF frequency.	
9	P3	Output port	Controlled on the basis of input data.	Nch open drain
10	P0			
11	P1			
12	P2			
13	AMIN	AM input	Local input for AM	IN
14	FMIN	FM input	Local input for FM	IN
15	V <sub>DD</sub>	Power supply	Power supply, with 4.0V to 6.0V applied voltage.	—
16	PD1	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
17	PD2			
18	V <sub>SS</sub>	GROUND	—	—

●Electrical characteristics (unless otherwise noted, Ta = 25°C, VDD1 = VDD2 = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current	IDD1	—	6.0	10.0	mA	FMIN=130MHz, 100mVrms
Quiescent current	IDD2	—	1.0	2.0	mA	No input,, PLL=OFF
Input high level voltage	VIH	4.0	—	—	V	CE, CK, DA terminals
Input low level voltage	VIL	—	—	1.0	V	CE, CK, DA terminals
Input high level current 1	IiH1	—	—	1.0	μA	CE, CK, DA terminals VIN=VDD
Input high level current 2	IiH2	—	0.3	—	μA	XIN terminals VIN=VDD
Input high level current 3	IiH3	—	6.0	—	μA	FMIN, AMIN, IFIN terminals VIN=VDD
Input low level current 1	IiL1	-1.0	—	—	μA	CE, CK, DA terminals VIN=VSS
Input low level current 2	IiL2	—	-0.3	—	μA	XIN terminals VIN=VSS
Input low level current 3	IiL3	—	-6.0	—	μA	FMIN, AMIN, IFIN terminals VIN=VSS
Output low level voltage 1	VOL1	—	0.2	0.5	V	P0, P1, P2, P3, DO Io=1.0mA
Off level leakage current 1	IOFF1	—	—	1.0	μA	P0, P1, P2, P3, DO Vo=10V
Output low level voltage 2	VOL2	—	0.1	0.5	V	FMIN, AMIN, IFIN IoUT=0.1mA
Output high level voltage	VOH	VDD-1.0	VDD-0.3	—	V	PD1, PD2 IoUT=-1.0mA
Output low level voltage	VOL	—	0.2	1.0	V	PD1, PD2 IoUT=1.0mA
Off level leakage current 2	IOFF2	—	—	100	nA	PD1, PD2 VOUT=VDD
Off level leakage current 3	IOFF3	-100	—	—	nA	PD1, PD2 VOUT=VSS
Internal feedback resistor 1	RF1	—	10	—	MΩ	XIN
Internal feedback resistor 2	RF2	—	500	—	kΩ	FMIN, ANIN, IFIN
Input frequency 1	FIN1	—	7.2	—	MHz	XIN, sine wave, C coupling
Input frequency 2	FIN2	20	—	130	MHz	FMIN, sine wave, C coupling VIN=50mVrms
Input frequency 3	FIN3	0.4	—	30	MHz	AMIN 1, sine wave, C coupling VIN=70mVrms
Input frequency 4	FIN4	0.4	—	16	MHz	IFIN, sine wave, C coupling VIN=70mVrms
Maximum input amplitude	FINMAX	—	—	1.5	Vrms	XIN,FMIN,AMIN,IFIN,sine wave,C coupling
Minimum pulse width	TW	—	1.0	—	μs	CK, DA
Input rise time	TR	—	—	500	ns	CE, CK, DA
Input fall time	TF	—	—	500	ns	CE, CK, DA

●Input data format



D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
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← — Input done from D0.

P0	P1	P2	P3	R0	R1	R2	S	CT	L0	L1	GT	SW	PL	PH	TS
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● Input data format

Explanation of the data

(1) Division data: For D<sub>0</sub> through D<sub>15</sub> (When S = 0, use D<sub>4</sub> through D<sub>15</sub>.)

Example: S = 0, SW = 0

When divide ratio = 1000, the actual set value is 500 since it passes through 1/2 the circuit. This translates to 1F4 (H) in HEX notation, and to (MSB) 0000 0001 1111 0100 (LSB) in binary notation. This data is used from LSB to D<sub>0</sub> through D<sub>15</sub>.

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	0

LSB

Example: S = 1, SW = 1

When divide ratio = 1000, the actual set value is 1000 since it does not pass through 1/2 the circuit. This translates to 3E8 (H) in HEX notation, and to (MSB) 0000 0011 1110 1000 (LSB) in binary notation. This data is used from LSB to D<sub>0</sub> through D<sub>15</sub>.

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0

Example: S = 1, SW = 0

When divide ratio = 1000, D<sub>0</sub> through D<sub>3</sub> can be anything since it does not pass through the prescaler. This translates to 3E8 (H) in HEX notation, and to (MSB) 0001 1111 0100 (LSB) in binary notation. This data is used from LSB to D<sub>0</sub> through D<sub>15</sub>.

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
X	X	X	X	0	0	0	1	0	1	1	1	1	1	0	0

(2) Output port control data: P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>, P<sub>3</sub>

1: Nch open drain output ON

0: Nch open drain output OFF

(3) R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub>, standard frequency data

Data			Standard frequency
R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>	
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	6.25kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	* PLL OFF

\* FMIN = pulldown, AMIN = pulldown, PD = high impedance

(4) S: switch between FMIN and AMIN

0: FMIN

1: AMIN

(5) CT: Intermediate frequency measurement operation

1: Begins measurement.

0: Resets internal counter, IFIN goes to pulldown.

(6) L<sub>0</sub>, L<sub>1</sub>: Setting of IF frequency detection amplitude

S	L <sub>0</sub>	L <sub>1</sub>	Frequency detection amplitude
0	0	0	10.70MHz±20kHz
0	0	1	10.65MHz±20kHz
0	1	0	10.75MHz±20kHz
0	1	1	*
1	0	0	450kHz±2.0kHz
1	0	1	459kHz±2.0kHz
1	1	0	450kHz±0.5kHz
1	1	1	459kHz±0.5kHz

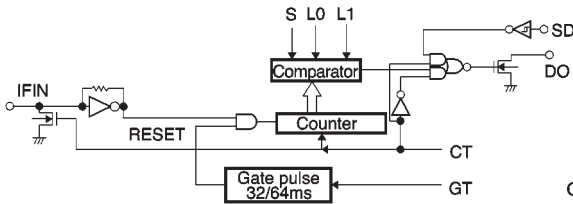
\*: Not used.

- (7) GT: Control of frequency measurement time  
0: 32ms  
1: 64ms
- (8) SW: If this bit is set to ON while AMIN is selected, swallow counter division is possible.

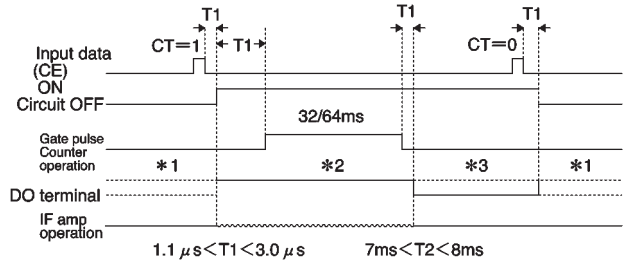
- (9) PL PH: Control of charge pump output  
PL = 0, PH = 0 PD1, PD2 go to PLL operation.  
PL = 1, PH = 0 PD1, PD2 go to LO level.  
PL = 0, PH = 1 PD1, PD2 go to HI level.  
PL = 1, PH = 1 PD1, PD2 go to LO level.
- (10) TS: Test data (0) is input

● Intermediate frequency detection circuit and the DO output.

(1) Structure

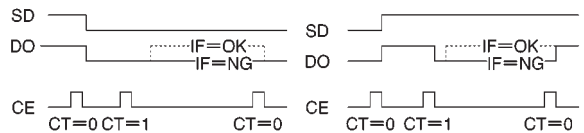
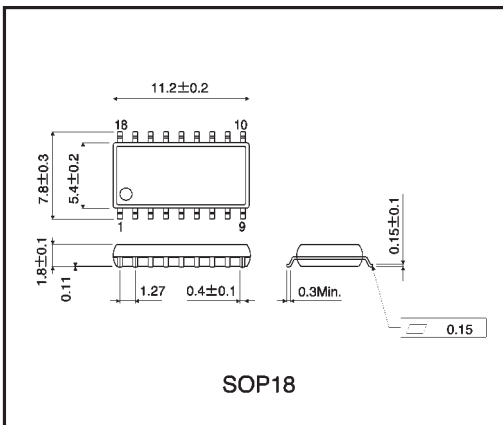


- (2) How the IF frequency detection circuit operates  
When control data CT is set to ON, the counter and the amp go into operation. When CT equals 0, the amp input pulldown counter is reset.



- (3) Explanation of the DO
- \*1 When the IF counter is OFF (CT = 0), SD input appears at the DO.
  - \*2 When the IF counter is set to ON (CT = 1), the control system keeps it at LO level until the measurement is finished.
  - \*3 After the measurement is finished, it goes to HI level if it is within the range of input frequency settings, and is kept at LO level if it is beyond the range of input frequency settings. When CT = 0, it returns to the conditions described under paragraph \*1.

● External dimensions (Units: mm)



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