National Semiconductor

March 2006

DS26LV32AQML
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that is comparable to TIA/EIA-422-B and ITU-T V.11 standards, but with a specified common mode voltage range of -0.5V to +5.5V due to the lower operating supply voltage of 3.0V to 3.6V. The TRI-STATE enables, EN and $\overline{EN}$, allow the device to be active High or active Low. The enables are common to all four receivers. The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200mV over the common mode range of -0.5V to +5.5V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Features

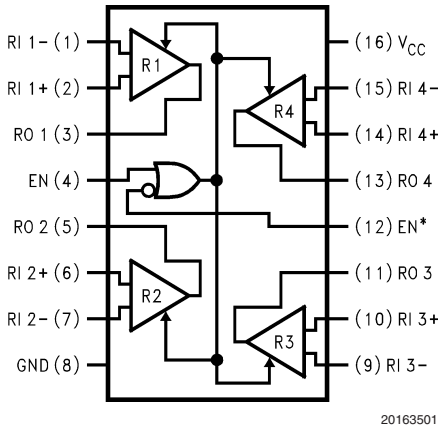
- Comparable to both TIA/EIA-422 and ITU-T V.11 standards
- Low Power CMOS design (30 mW typical)
- Interoperable with existing 5V RS-422 networks
- Receiver OPEN input failsafe feature
- Pin compatible with DS26C32AT

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS26LV32AW-QML	5962–9858501QFA	W16A	16LD Ceramic Flatpack

Connection Diagram

Ceramic Flatpack



Top View
See NS Package Number W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	7.0V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{Diff})	±14V
Enable Input Voltage (V_I)	-0.5V to V_{CC}+0.5V
Storage Temperature Range (T_{Stg})	-65˚C ≤ T_A ≤ +150˚C
Lead Temperature (T_L) Soldering, 4 seconds	260˚C
Maximum Power Dissipation +25˚C (Note 2)	1087mW
Thermal Resistance	
θ_{JA}	138˚C/W
θ_{JC}	13.5˚C/W

Recommended Operating Conditions

Supply Voltage (v_{CC})	3.0V to 3.6V
Operating Temperature Range (T_A)	–55˚C ≤ T_A ≤ +125˚C

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp ˚C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

DS26LV32AQML Electrical Characteristics

DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{Th}	Minimum Differential Input Voltage	V_{CC} = 3.0/3.6V, $V_O = V_{OH}$ or V_{OL}, -0.5V < V_{CM} < +5.5V		-200	+200	mV	1, 2, 3
R_I	Input Resistance	V_{CC} = 3.6V, -0.5V < V_{CM} < +5.5V, One input AC Gnd		5.0		KΩ	1, 2, 3
I_I	Input Current	V_{CC} = 3.6V, V_I = +5.5V Other Input = Gnd		0.0	+1.8	mA	1, 2, 3
		V_{CC} = 3.6V, V_I = -0.5V Other Input = Gnd		0.0	-1.8	mA	1, 2, 3
		V_{CC} = 0V, V_I = +5.5V Other Input = Gnd		0.0	+1.8	mA	1, 2, 3
		V_{CC} = 0V, V_I = -0.5V Other Input = Gnd		0.0	-1.8	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 3.0V, V_{Diff} = +1V, I_O = -6.0mA		2.4		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 3.0V, V_{Diff} = -1V, I_O = 6.0mA			0.5	V	1, 2, 3
V_{IH}	Minimum Enable High Level Voltage		(Note 3)	2.0		V	1, 2, 3
V_{IL}	Maximum Enable Low Level Voltage		(Note 3)		0.8	V	1, 2, 3
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{CC} = 3.6V, $V_O = V_{CC}$ or Gnd Enable = V_{IL}, $\overline{\text{Enable}} = V_{IH}$			±50	µA	1, 2, 3
I_{En}	Maximum Enable Input Current	V_{CC} = 3.6V, $V_I = V_{CC}$ or Gnd			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, No Load, En, $\overline{\text{En}} = V_{CC}$ or Gnd, -0.5V<V_{CM}<+5.5V			20	mA	1, 2, 3
I_{OS}	Output Short Circuit Current	V_{CC} = 3.0V/3.6V, V_O = 0V, V_{Diff} = +1V	(Note 4)	-10	-70	mA	1, 2, 3

DS26LV32AQML Electrical Characteristics (Continued)

AC Parameters

The following conditions apply, unless otherwise specified.

AC: V_{CC} = 3.0/3.6V, C_L = 50pF

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PLH}	Input to Output Propagation Delay	V_{CM} = 1.5V	(Note 5)	6.0	45	nS	9, 10, 11
t_{PHL}	Input to Output Propagation Delay	V_{CM} = 1.5V	(Note 5)	6.0	45	nS	9, 10, 11
t_{SK1}	Skew tpHLD-tpLHD (same channel)				6.0	nS	9, 10, 11
t_{SK2}	Pin to Pin Skew (Same device)				6.0	nS	9, 10, 11
t_{PLZ}	Output Disable Time	2KΩ to V_{CC}	(Note 6)		50	nS	9, 10, 11
t_{PZL}	Output Enable Time	2KΩ to V_{CC}	(Note 6)		50	nS	9, 10, 11
t_{PHZ}	Output Disable Time	2KΩ to Gnd	(Note 6)		50	nS	9, 10, 11
t_{PZH}	Output Enable Time	2KΩ to Gnd	(Note 6)		50	nS	9, 10, 11

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: Derate CERPAK 7.3mW/˚C above +25˚C.

Note 3: Parameter tested Go-No-Go only.

Note 4: Short one output at a time to Gnd.

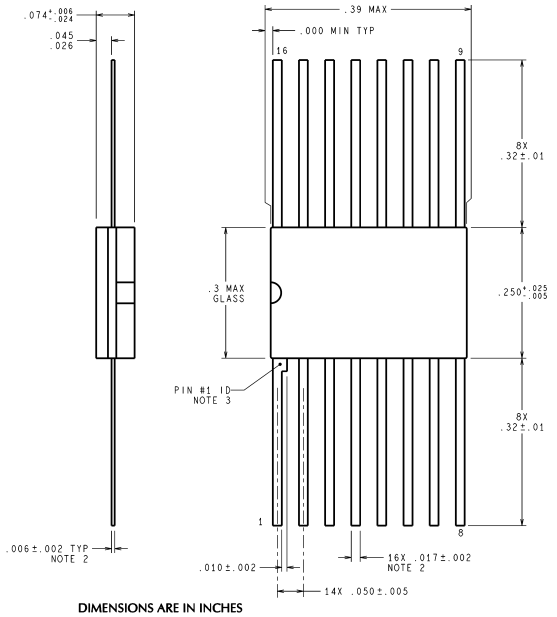
Note 5: Generator waveform is specified as follows: f = 1MHz, Duty Cycle = 50%, Z_O = 50Ω, $t_R = t_F \leq$ 6nS. Receiver inputs = 1V to 2V with measure points equal to 1.5V on the inputs to 1/2 V_{CC} on the outputs.

Note 6: Generator waveform is specified as follows: f = 1MHz, Duty Cycle = 50%, Z_O = 50Ω, $t_R = t_F \leq$ 6nS. En/$\overline{\text{En}}$ inputs = 0V to 3V with measure points equal to 1.5V on the inputs, to 1/2 V_{CC} on the outputs for Z_L and Z_H, and (V_{OL} + 0.3V) for L_Z, and (V_{OH}.- 0.3V) for H_Z.

Revision History Section

Released	Revision	Section	Originator	Changes
03/01/06	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into one Corp. data sheet format. MNDS26LV32A-X Rev 0A0 will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted



Cerpack Package (W)
NS Package Number W16A

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