

DS90C031QML

LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, thus dropping the device to a low idle power state of 11 mW typical.

In addition, the DS90C031 provides power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present. The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- High impedance LVDS outputs with power-off
- ± 350 mV differential signaling
- Low power dissipation
- Low differential skew
- Low propagation delay
- Pin compatible with DS26C31
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with proposed TIA LVDS standard

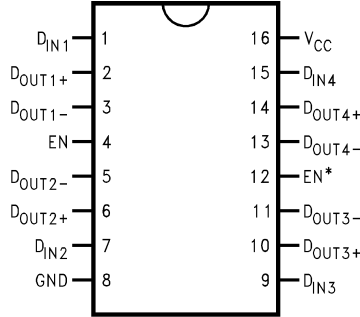
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
DS90C031E-QML	5962-9583301Q2A	E20A	20LD Leadless Chip Carrier
DS90C031W-QML	5962-9583301QFA	W16A	16LD Ceramic Flatpack
DS90C031WG-QML	5962-9583301QZA	WG16A	16LD Ceramic SOIC
DS90C031W-QMLV	5962-9583301VFA	W16A	16LD Ceramic Flatpack
DS90C031WG-QMLV	5962-9583301VZA	WG16A	16LD Ceramic SOIC
DS90C031WRQMLV	5962R9583301VFA 100k rd(Si)	W16A	16LD Ceramic Flatpack
DS90C031WGRQMLV	5962R9583301VZA 100k rd(Si)	WG16A	16LD Ceramic SOIC

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Connection Diagrams

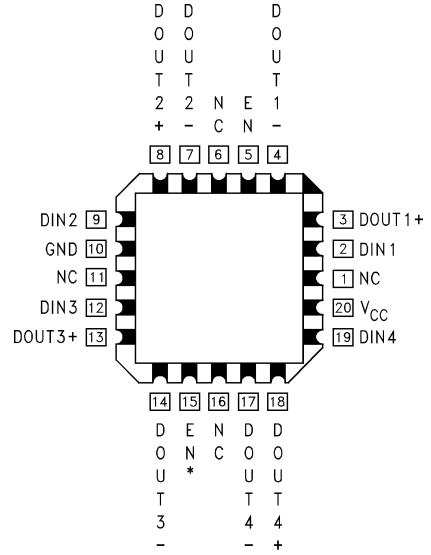
Dual-In-Line



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See NS Package Number W16A & WG16A

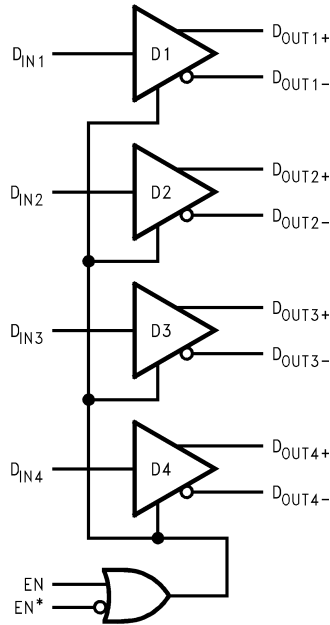
LCC Package



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See NS Package Number E20A

Functional Diagram



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Truth Table

Enables		Input	Outputs	
EN	EN*	D _I	D _{O+}	D _{O-}
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.3V to +6V
Input Voltage (D_i)	-0.3V to ($V_{CC} + 0.3V$)
Enable Input Voltage (EN, EN*)	-0.3V to ($V_{CC} + 0.3V$)
Output Voltage (D_{O+} , D_{O-})	-0.3V to ($V_{CC} + 0.3V$)
Storage Temperature Range	$-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation @ +25°C (Note 4)	
20 Pin LCC Package	1,900 mW
16 Pin Flatpack	1,450 mW
16 Pin Ceramic SOIC	1,450 mW
Thermal Resistance	
θ_{JA}	
20 Pin LCC Package	78 °C/W
16 Pin Flatpack	145 °C/W
16 Pin Ceramic SOIC	145 °C/W
θ_{JC}	
20 Pin LCC Package	18 °C/W
16 Pin Flatpack	14 °C/W
16 Pin Ceramic SOIC	14 °C/W
ESD Rating (Note 3)	3.5KV

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{CC})	+4.5V	+5.0V	+5.5V
Operating Free Air Temperature (T_A)	-55°C	+25°C	+125°C

Radiation Features

DS90C031WRQMLV	100 krad (Si)
DS90C031WGRQMLV	100 krad (Si)

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

DC Parameters (Note 9)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{OD1}	Differential Output Voltage	$R_L = 100\Omega$		250	450	mV	1, 2, 3
DV_{OD1}	Change in Magnitude of V_{OD1} for complementary output States	$R_L = 100\Omega$			35	mV	1, 2, 3
V_{OS}	Offset Voltage	$R_L = 100\Omega$		1.125	1.375	V	1, 2, 3
DV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	$R_L = 100\Omega$			25	mV	1, 2, 3
V_{OH}	Output Voltage High	$R_L = 100\Omega$			1.6	V	1, 2, 3
V_{OL}	Output Voltage Low	$R_L = 100\Omega$		0.9		V	1, 2, 3
V_{IH}	Input Voltage High		(Note 5)	2.0	V_{CC}	V	1, 2, 3
V_{IL}	Input Voltage Low		(Note 5)	Gnd	0.8	V	1, 2, 3
I_I	Input Current	$V_I = V_{CC}, \text{Gnd}, 2.5, \text{ or } 0.4\text{V}$			± 10	μA	1, 2, 3
V_{CI}	Input Clamp Voltage	$I_{CI} = -18\text{mA}$			-1.5	V	1, 2, 3
I_{OS}	Output Short Circuit Current	$V_O = 0\text{V}$			-5.0	mA	1, 2, 3
I_{Off}	Power-off Leakage	$V_O = 0\text{V or } 2.4\text{V},$ $V_{CC} = 0\text{V or Open}$			± 10	μA	1, 2, 3
I_{OZ}	Output TRI-STATE Current	$EN = 0.8\text{V and } EN^* = 2.0\text{V}$ $V_O = 0\text{V or } V_{CC}$			± 10	μA	1, 2, 3
I_{CC}	Drivers Enabled Supply Current	$D_I = \text{Hi or Low}$			25	mA	1, 2, 3
I_{CCZ}	Drivers Disabled Supply Current	$D_I = \text{Hi or Low}, EN = \text{Gnd},$ $EN^* = V_{CC}$			10	mA	1, 2, 3

AC Parameters

The following conditions apply, unless otherwise specified.

AC: $V_{CC} = 4.5\text{V} / 5.0\text{V} / 5.5\text{V}, R_L = 100\Omega$ (between outputs), $C_L = 20\text{pF}$ (each output to Gnd)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
t_{PHLD}	Differential Propagation Delay High to Low			0.5	5.0	ns	9, 10, 11
t_{PLHD}	Differential Propagation Delay Low to High			0.5	5.0	ns	9, 10, 11
t_{SKD}	Differential Skew $ t_{PHLD} - t_{PLHD} $				3.0	ns	9, 10, 11
t_{SK1}	Channel to Channel Skew		(Note 6)		3.0	ns	9, 10, 11
t_{SK2}	Chip to Chip Skew		(Note 7)		4.5	ns	9, 10, 11
t_{PHZ}	Disable Time High to Z		(Note 8)		20	ns	9, 10, 11
t_{PLZ}	Disable Time Low To Z		(Note 8)		20	ns	9, 10, 11
t_{PZH}	Enable Time Z to High		(Note 8)		20	ns	9, 10, 11
t_{PZL}	Enable Time Z to Low		(Note 8)		20	ns	9, 10, 11

AC/DC Parameters - Post Radiation Limits (Note 9)

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Drivers Enabled Supply Current	$D_I = \text{Hi or Low}, EN = \text{Gnd},$ $EN^* = V_{CC}$			30	mA	1
I_{CCZ}	Drivers Disabled Supply Current	$D_I = \text{Hi or Low}, EN = \text{Gnd},$ $EN^* = V_{CC}$			30	mA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5 k Ω in series with 100 pF.

Note 4: Derate LCC @ 12.8mW/°C above +25°C. Derate Ceramic flatpack @ 6.9mW/°C above +25°C.

Note 5: Tested during V_{OH} / V_{OL} tests.

Note 6: Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

Note 7: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 8: Parameter guaranteed, not tested 100%

Note 9: Pre and Post irradiation limits are identical to those listed under AC & DC electrical characteristics except as listed in the "Post Radiation Limits" table. Radiation end point limits for the noted parameters are guaranteed only for the conditions, as specified.

Parameter Measurement Information

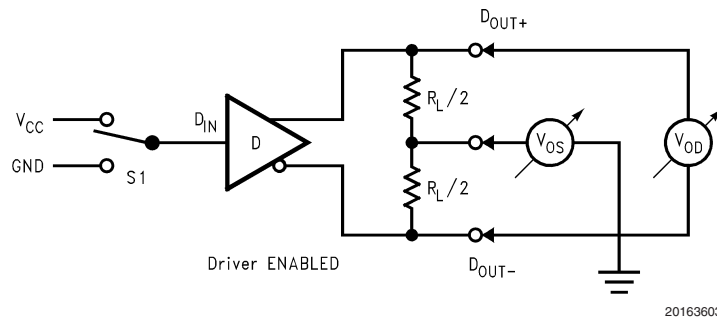


FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

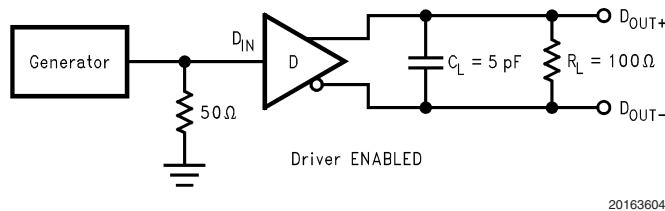


FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

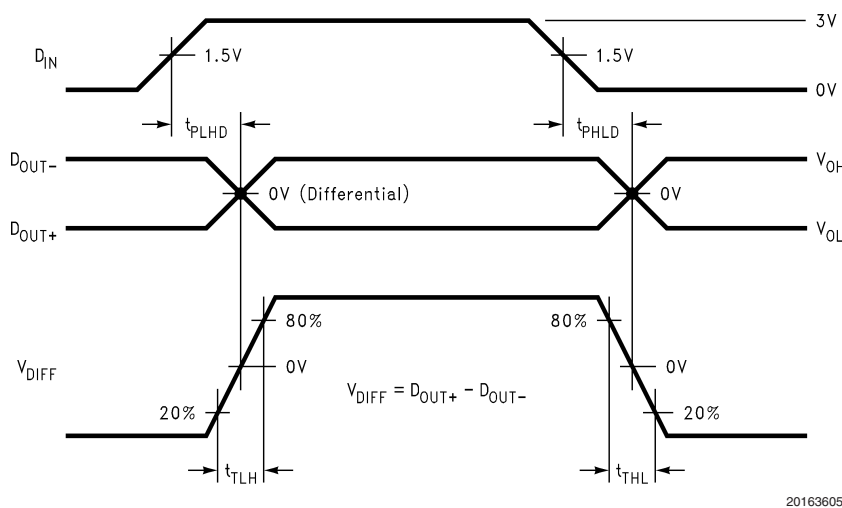
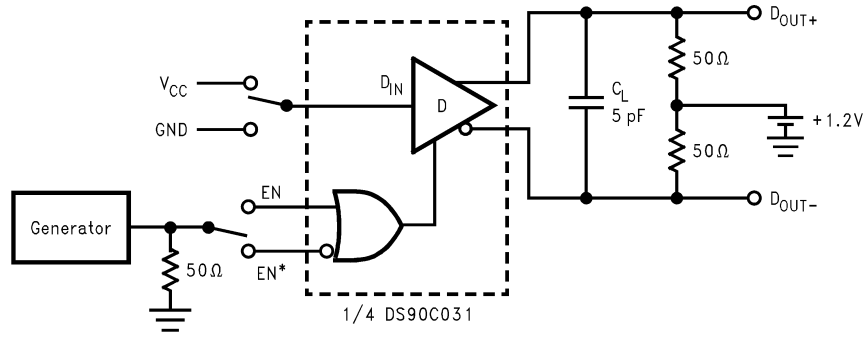


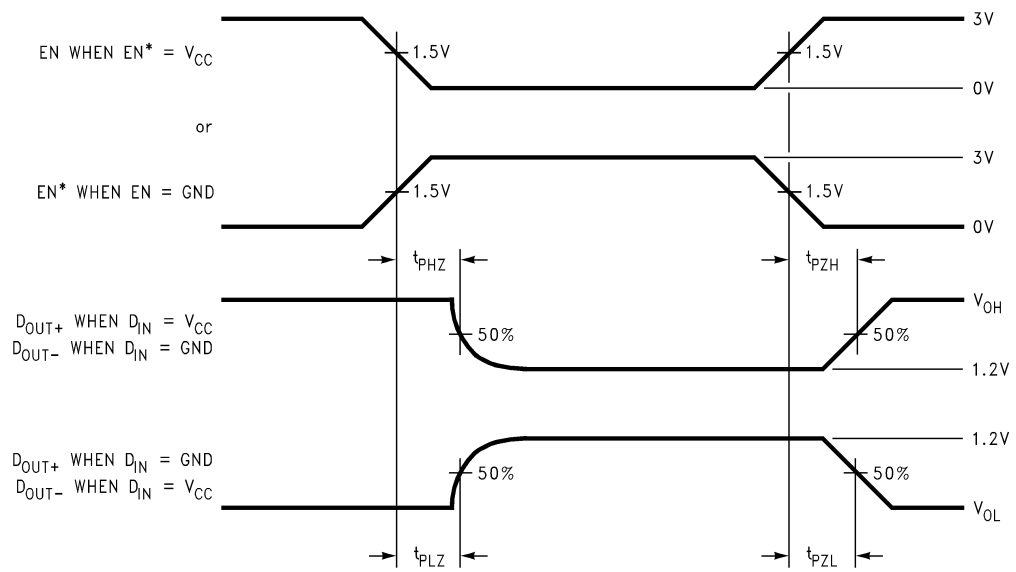
FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)



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FIGURE 4. Driver TRI-STATE Delay Test Circuit

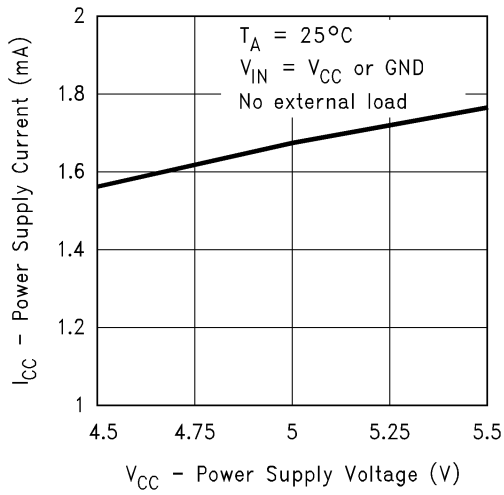


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FIGURE 5. Driver TRI-STATE Delay Waveform

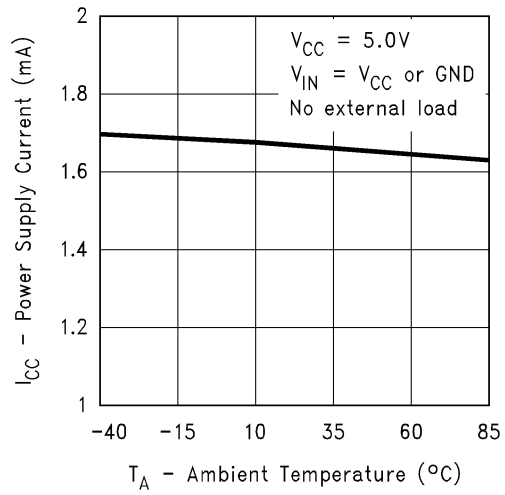
Typical Performance Characteristics

Power Supply Current vs Power Supply Voltage



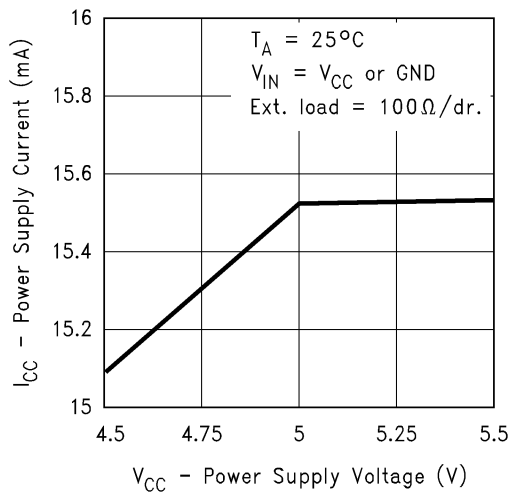
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Power Supply Current vs Temperature



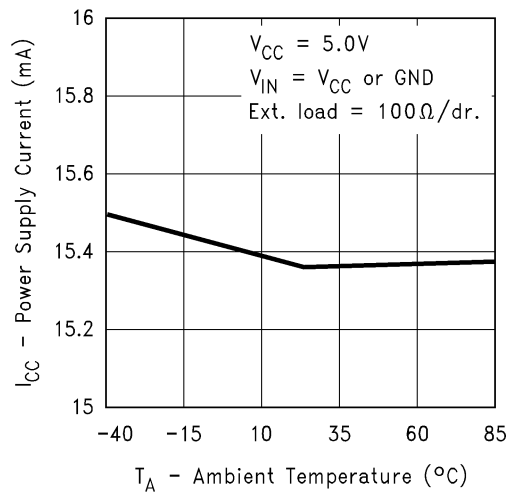
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Power Supply Current vs Power Supply Voltage



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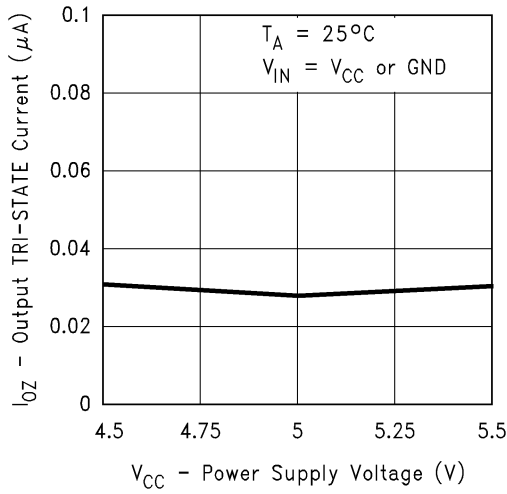
Power Supply Current vs Temperature



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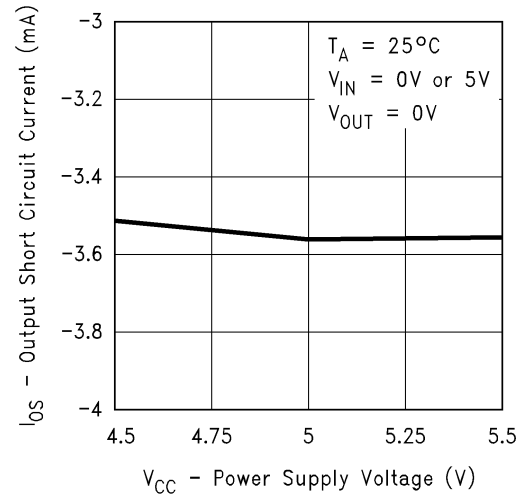
Typical Performance Characteristics (Continued)

Output TRI-STATE Current vs Power Supply Voltage



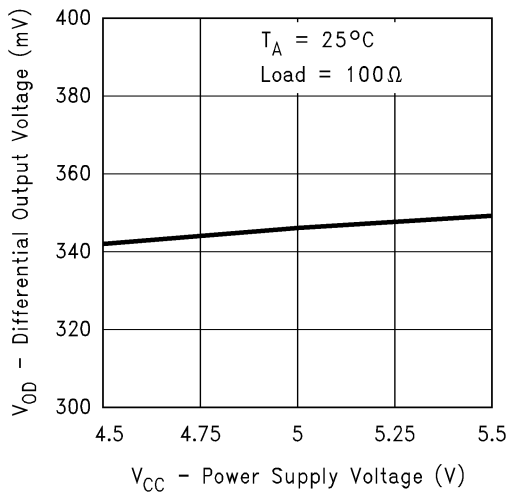
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Output Short Circuit Current vs Power Supply Voltage



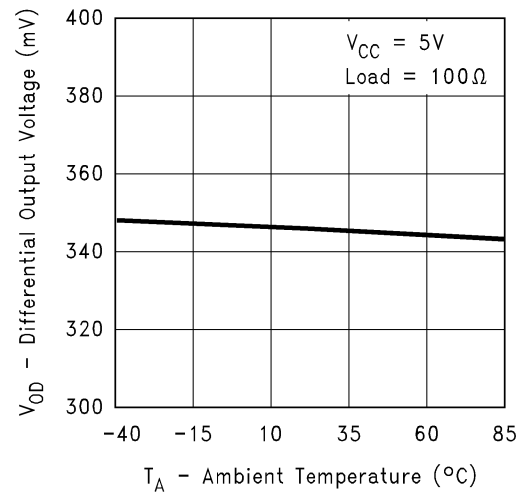
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Differential Output Voltage vs Power Supply Voltage



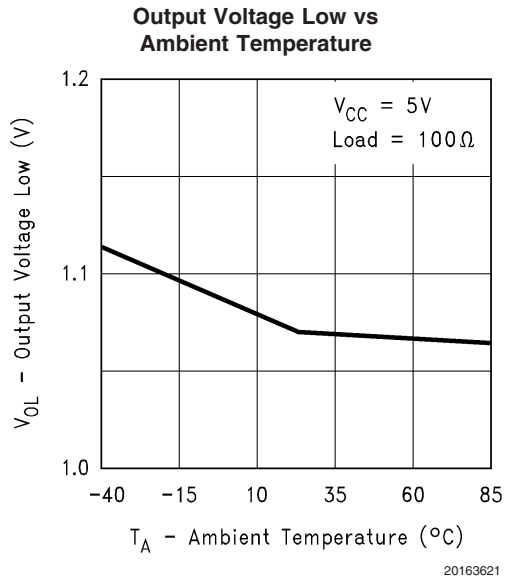
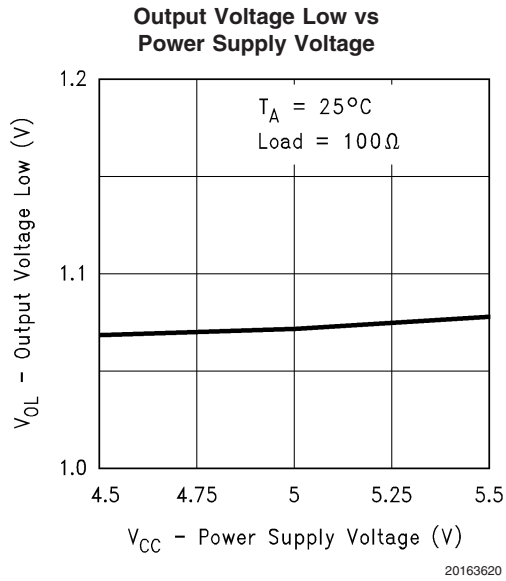
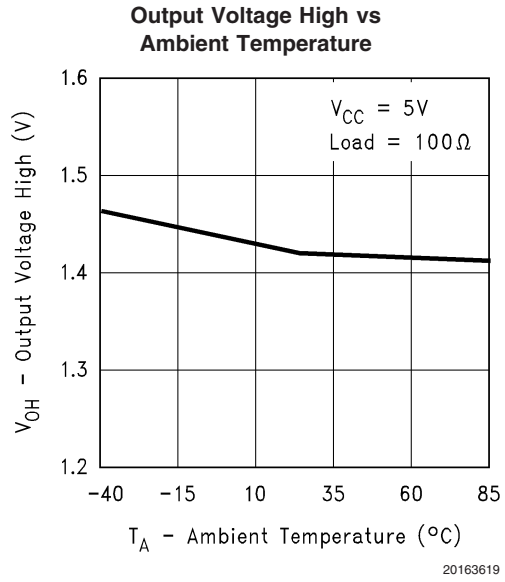
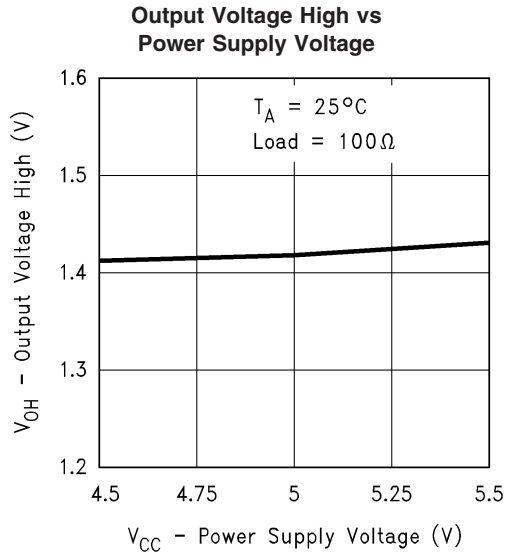
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Differential Output Voltage vs Ambient Temperature

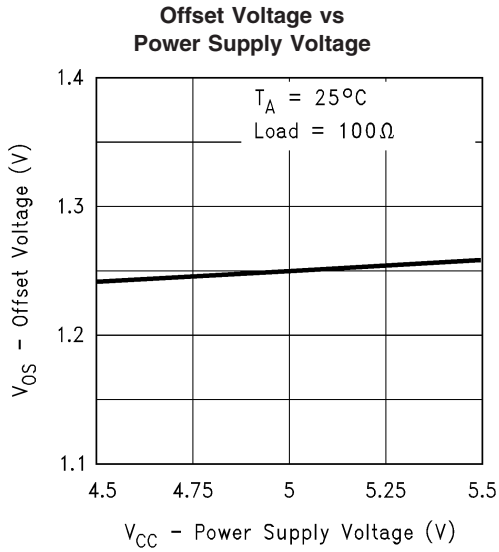


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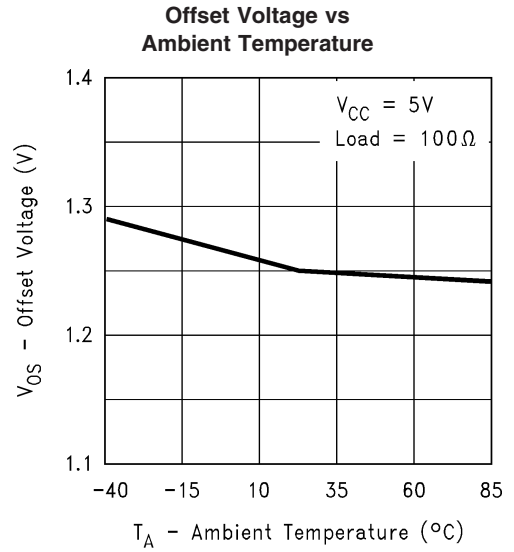
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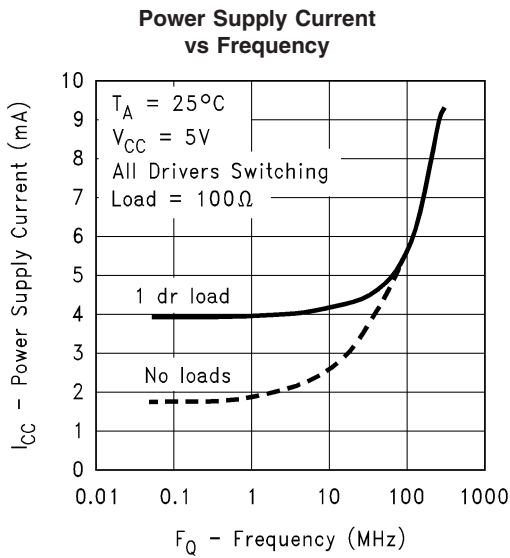
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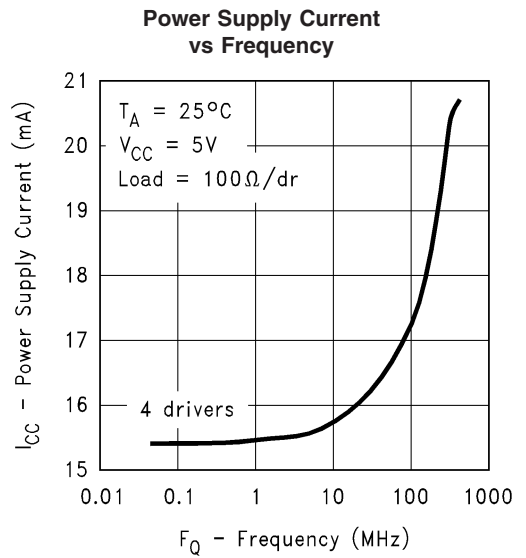
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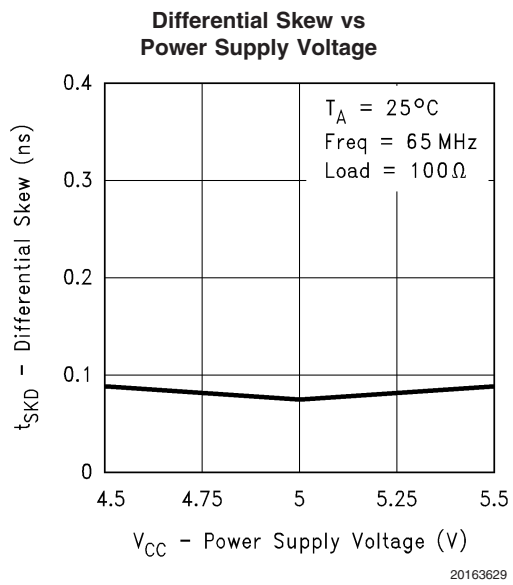
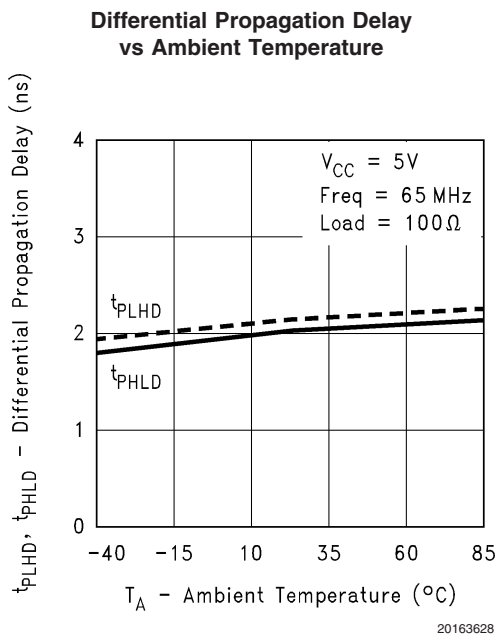
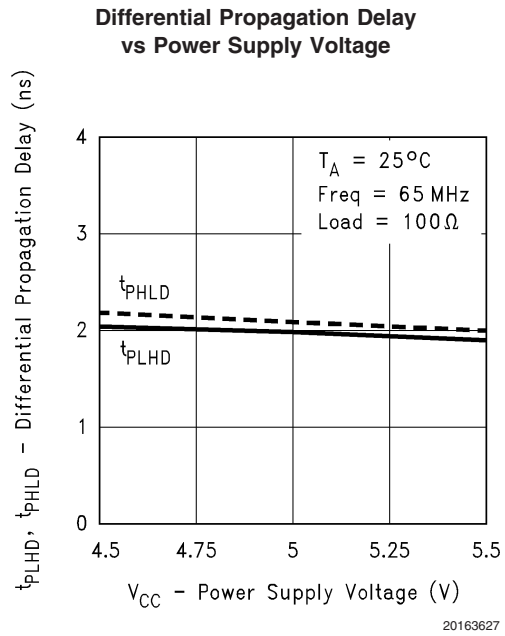
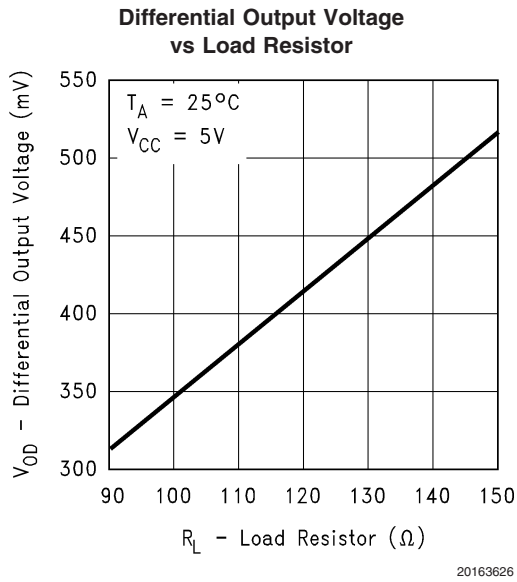


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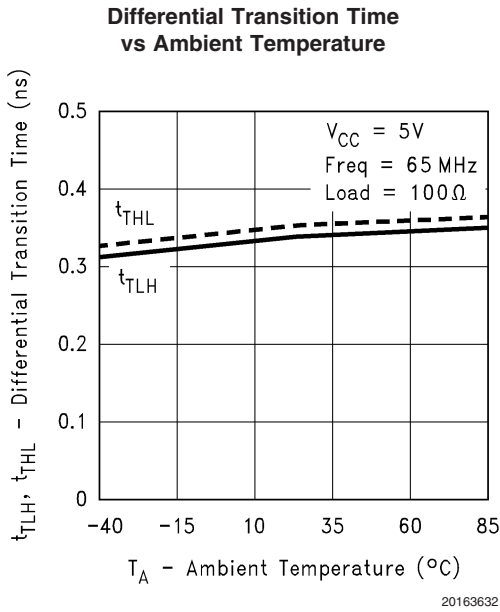
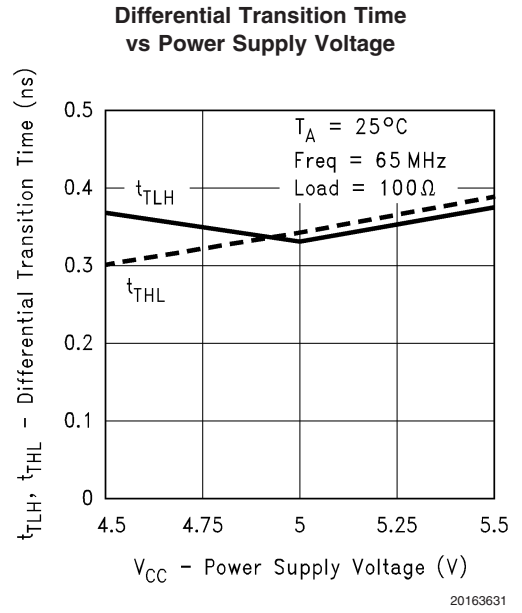
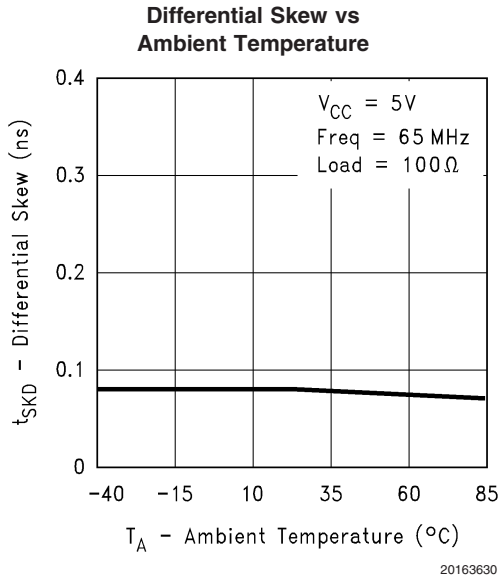


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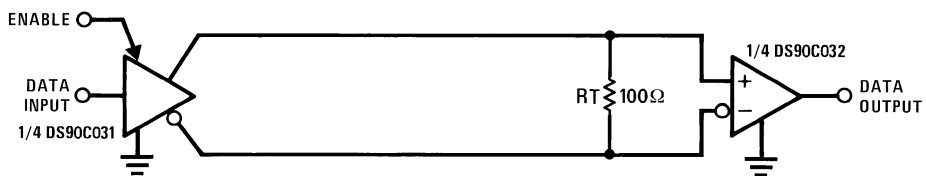
Typical Performance Characteristics (Continued)



Typical Performance Characteristics (Continued)



Typical Application



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FIGURE 6. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 6*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C03 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 6*. AC or unterminated

configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV – 100 mV = 240 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 7*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90C031 is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.

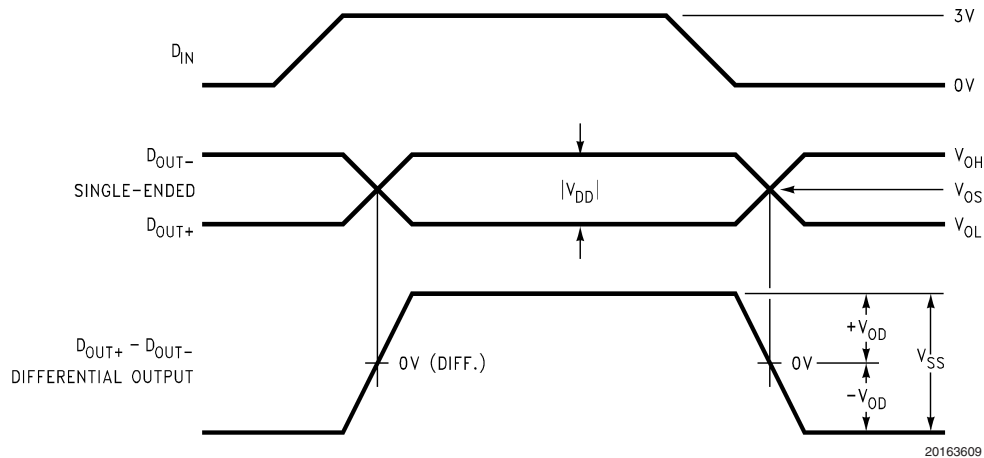


FIGURE 7. Driver Output Levels

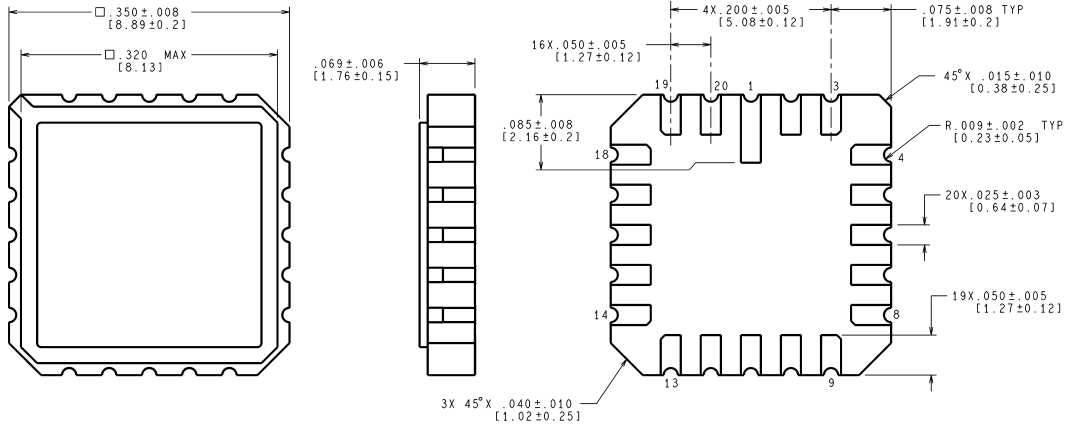
Pin Descriptions

Pin No. (SOIC)	Name	Description
1, 7, 9, 15	D_I	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	D_{O+}	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	D_{O-}	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	Gnd	Ground pin

Revision History

Released	Revision	Section	Originator	Changes
03/01/06	A	New Release, Corporate format	L. Lytle	1 MDS data sheet converted into Corp. data sheet format. MNDS90C031-X-RH Rev 2A1 will be archived.

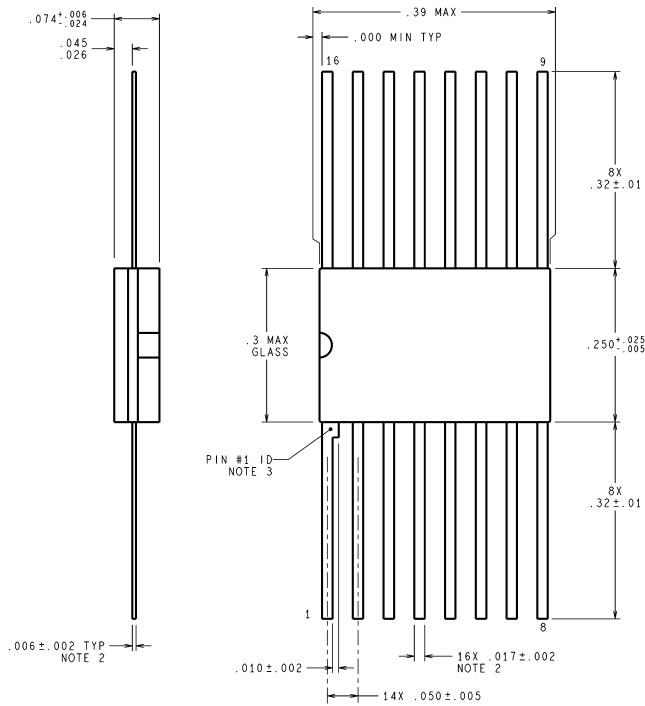
Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

E20A (Rev F)

**20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A**

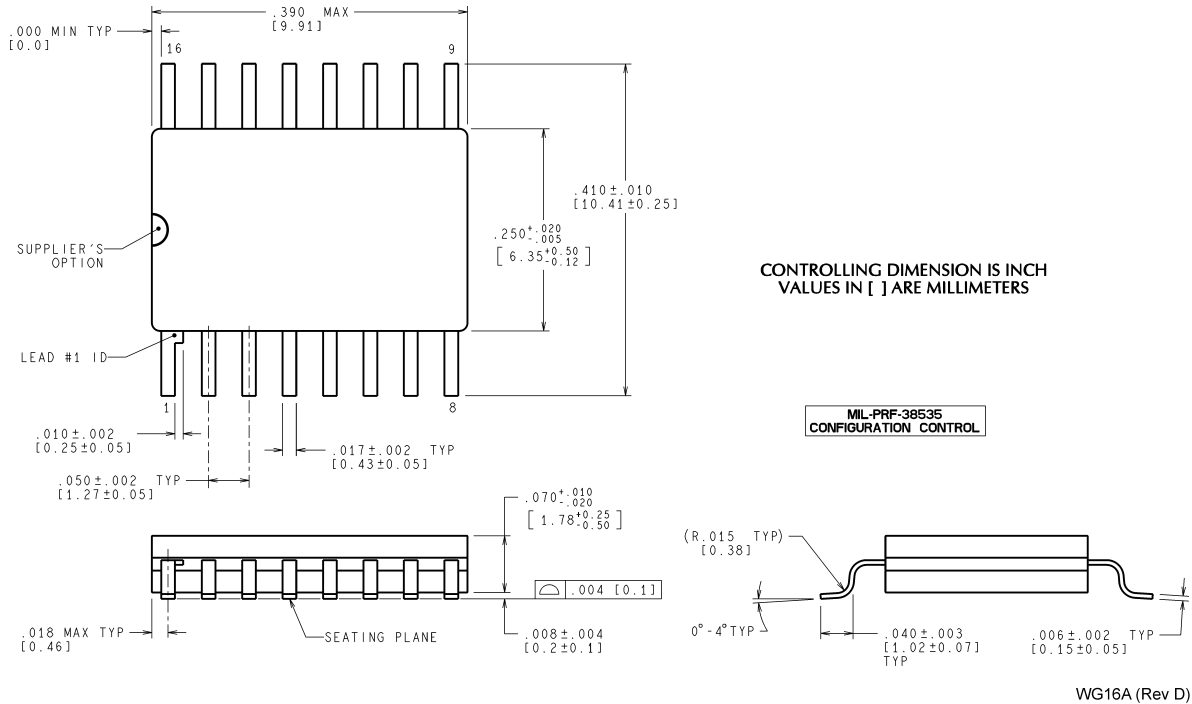


DIMENSIONS ARE IN INCHES

W16A (Rev T)

**16-Lead Ceramic Flatpack
See NS Package Number W16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic SOIC
See NS Package Number WG16A

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