National Semiconductor

January 2006

DS90CR481 / DS90CR482
48-Bit LVDS Channel Link SER/DES – 65 - 112 MHz

General Description

The DS90CR481 transmitter converts 48 bits of CMOS/TTL data into eight LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a ninth LVDS link. Every cycle of the transmit clock 48 bits of input data are sampled and transmitted. The DS90CR482 receiver converts the LVDS data streams back into 48 bits of LVCMOS/TTL data. At a transmit clock frequency of 112MHz, 48 bits of TTL data are transmitted at a rate of 672Mbps per LVDS data channel. Using a 112MHz clock, the data throughput is 5.38Gbit/s (672Mbytes/s). At a transmit clock frequency of 112MHz, 48 bits of TTL data are transmitted at a rate of 672Mbps per LVDS data channel. Using a 66MHz clock, the data throughput is 3.168Gbit/s (396Mbytes/s).

The multiplexing of data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 48-bit wide data and one clock, up to 98 conductors are required. With this Channel Link chipset as few as 19 conductors (8 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 48 CMOS/TTL inputs can support a variety of signal combinations. For example, 6 8-bit words or 5 9-bit (byte + parity) and 3 controls.

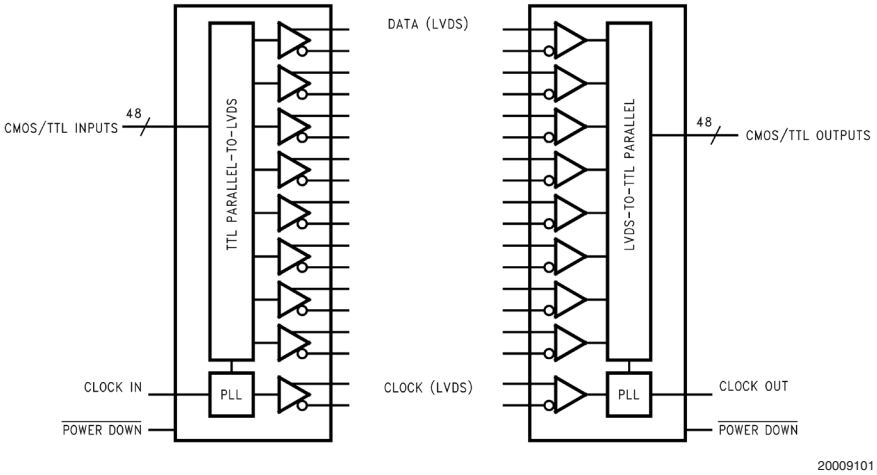
The DS90CR481/DS90CR482 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to +/–1 LVDS data bit time (up to 80 MHz Clock Rate). These three enhancements allow cables 5+ meters in length to be driven.

The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

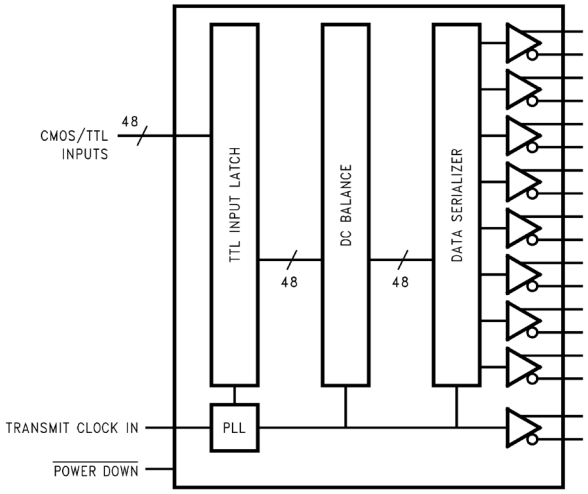
- 3.168 Gbits/sec bandwidth with 66 MHz Clock
- 5.376 Gbits/sec bandwidth with 112 MHz Clock
- 65 - 112 MHz input clock support
- LVDS SER/DES reduces cable and connector size
- Pre-emphasis reduces cable loading effects
- Optional DC balance encoding reduces ISI distortion
- Cable Deskew of +/–1 LVDS data bit time (up to 80 MHz Clock Rate)
- 5V Tolerant TxIN and control input pins
- Flow through pinout for easy PCB design
- +3.3V supply voltage
- Transmitter rejects cycle-to-cycle jitter
- Conforms to ANSI/TIA/EIA-644-1995 LVDS Standard

Generalized Block Diagrams (DS90CR481 and DS90CR482)



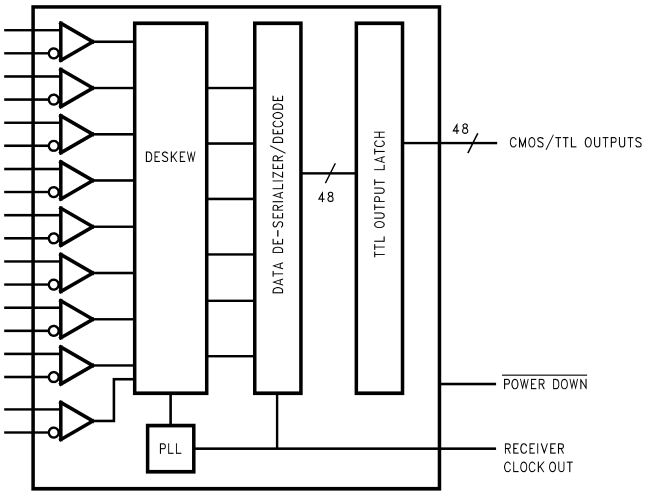
© 2006 National Semiconductor Corporation

Generalized Transmitter Block Diagram – DS90CR481



20009102

Generalized Receiver Block Diagram – DS90CR482



20009103

Ordering Information

Order Number	Function	Package
DS90CR481VJD	Transmitter (Serializer)	VJD100A
DS90CR482VS	Receiver (Deserializer)	VJD100A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +4V
CMOS/TTL Input Voltage	−0.3V to +5.5V
LVCMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to +3.6V
LVDS Driver Output Voltage	−0.3V to +3.6V
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	
100L TQFP	+260˚C
Maximum Package Power Dissipation Capacity @ 25˚C	
100 TQFP Package:	
DS90CR481VJD	2.3W
DS90CR482VS	2.3W
Package Derating:	
DS90CR481VJD	18.1mW/˚C above +25˚C
DS90CR482VS	18.1mW/˚C above +25˚C
ESD Rating:	
DS90CR481	
(HBM, 1.5kΩ, 100pF)	> 6 kV
(EIAJ, 0Ω, 200pF)	> 300 V
DS90CR482	
(HBM, 1.5kΩ, 100pF)	> 2 kV
(EIAJ, 0Ω, 200pF)	> 200 V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Supply Noise Voltage			100	mV_{p-p}
Input Clock (TX)	65		112	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	2.9		V
		I_{OH} = −2mA	2.7	2.85		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+15	μA
		V_{IN} = GND	−15	0		μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−120	mA
LVDS DRIVER DC SPECIFICATIONS						
$\|V_{OD}\|$	Differential Output Voltage	R_L = 100Ω	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	μA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	μA
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, BAL = High, Worst Case Pattern (*Figures 1, 2*)	f = 66MHz		106	160	mA
			f = 112MHz		155	210	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{PD}$ = Low Driver Outputs in TRI-STATE during power down Mode			5	50	μA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, BAL = High, Worst Case Pattern (*Figures 1, 3*)	f = 66MHz		200	210	mA
			f = 112MHz		250	280	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{PD}$ = Low Receiver Outputs stay low during power down mode.			20	100	μA

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time (*Figure 4*)	1.0	2.0	3.0	ns
TCIP	TxCLK IN Period (*Figure 5*)	8.93		15.38	ns
TCIH	TxCLK in High Time (*Figure 5*)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (*Figure 5*)	0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time	1.5		6.0	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time, (*Figure 2*), PRE = 0.75V (disabled)			0.14	0.7	ns
	LVDS Low-to-High Transition Time, (*Figure 2*), PRE = Vcc (max)			0.11	0.6	ns
LHLT	LVDS High-to-Low Transition Time, (*Figure 2*), PRE = 0.75V (disabled)			0.16	0.8	ns
	LVDS High-to-Low Transition Time, (*Figure 2*), PRE = Vcc (max)			0.11	0.7	ns
TBIT	Transmitter Bit Width	f = 66 MHz, 112MHz		1/7 TCIP		ns
TPPOS	Transmitter Pulse Positions - Normalized	f = 65 to 112 MHz	– 200	0	+200	ps
TJCC	Tranmitter Jitter - Cycle-to-Cycle			100		ps
TCCS	TxOUT Channel to Channel Skew			40		ps
TSTC	TxIN Setup to TxCLK IN, (*Figure 5*)		2.5			ns
THTC	TxIN Hold to TxCLK IN, (*Figure 5*)		0			ns
TPDL	Transmitter Propagation Delay - Latency, (*Figure 7*)		1.5(TCIP)+3.72	1.5(TCIP)+4.4	1.5(TCIP)+6.24	ns
TPLLS	Transmitter Phase Lock Loop Set, (*Figure 9*)				10	ms
TPDD	Transmitter Powerdown Delay, (*Figure 11*)				100	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time, Rx data out, (*Figure 3*)				2.0	ns
	CMOS/TTL Low-to-High Transition Time, Rx clock out, (*Figure 3*)				1.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time, Rx data out, (*Figure 3*)				2.0	ns
	CMOS/TTL High-to-Low Transition Time, Rx clock out, (*Figure 3*)				1.0	ns
RCOP	RxCLK OUT Period, (*Figure 6*)		8.928	T	15.38	ns
RCOH	RxCLK OUT High Time, (*Figure 6*), (Note 4)	f = 112 MHz	3.5			ns
		f = 66 MHz	6.0			ns
RCOL	RxCLK OUT Low Time, (*Figure 6*), (Note 4)	f = 112 MHz	3.5			ns
		f = 66 MHz	6.0			ns
RSRC	RxOUT Setup to RxCLK OUT,(*Figure 6*)	f = 112 MHz	2.4			ns
		f = 66 MHz	3.6			ns
RHRC	RxOUT Hold to RxCLK OUT, (*Figure 6*), (Note 4)	f = 112 MHz	3.4			ns
		f = 66 MHz	6.0			ns
RPDL	Receiver Propagation Delay - Latency, (*Figure 8*)		3(TCIP)+4.0	3(TCIP)+4.8	3(TCIP)+6.5	ns
RPLLS	Receiver Phase Lock Loop Set, (*Figure 10*)				10	ms
RPDD	Receiver Powerdown Delay, (*Figure 12*)				1	µs

Chipset RSKM Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(Notes 4, 7). See Applications Information section for more details on this parameter and how to apply it.

Symbol	Parameter		Min	Typ	Max	Units
RSKM	Receiver Skew Margin without Deskew in non-DC Balance Mode, (*Figure 13*), (Note 5)	f = 112 MHz	170			ps
		f = 100 MHz	170	240		ps
		f = 85MHz	300	350		ps
		f = 66MHz	300	350		ps
RSKM	Receiver Skew Margin without Deskew in DC Balance Mode, (*Figure 13*), (Note 5)	f = 112 MHz	170			ps
		f = 100 MHz	170	200		ps
		f = 85 MHz	250	300		ps
		f = 66 MHz	250	300		ps
RSKMD	Receiver Skew Margin with Deskew in DC Balance, (*Figure 14*), (Note 6)	f = 33 to 80 MHz	0.25TBIT			ps
RDR	Receiver Deskew Range	f = 80 MHz	± 1			TBIT
RDSS	Receiver Deskew Step Size	f = 80 MHz		0.3 TBIT		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25˚C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{TH}, V_{TL}, V_{OD} and ΔV_{OD}).

Note 4: The Minimum and Maximum Limits are based on statistical analysis of the device performance over voltage and temperature ranges. This parameter is functionally tested on Automatic Test Equipment (ATE). ATE is limited to 85MHz. A sample of characterization parts have been bench tested to verify functional performance.

Note 5: Receiver Skew Margin (RSKM) is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window, RSPOS). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable) and clock jitter (TJCC).

RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle,TJCC) + ISI (if any). See Applications Information section for more details.

Note 6: Receiver Skew Margin with Deskew (RSKMD) is defined as the valid data sampling region at the receiver inputs. The DESKEW function will constrain the receiver's sampling strobes to the middle half of the LVDS bit and removes (adjusts for) fixed interconnect skew. This margin (RSKMD) allows for inter-symbol interference (dependent on type/length of cable), Transmitter Pulse Position (TPPOS) variance, and LVDS clock jitter (TJCC).

RSKMD ≥ ISI + TPPOS(variance) + source clock jitter (cycle to cycle, TJCC). See Applications Information section for more details.

Note 7: Typical values for RSKM and RSKMD are applicable for fixed V_{CC} and T_A of the Transmitter and Receiver (both are assumed to be at the same V_{CC} and T_A points).

AC Timing Diagrams

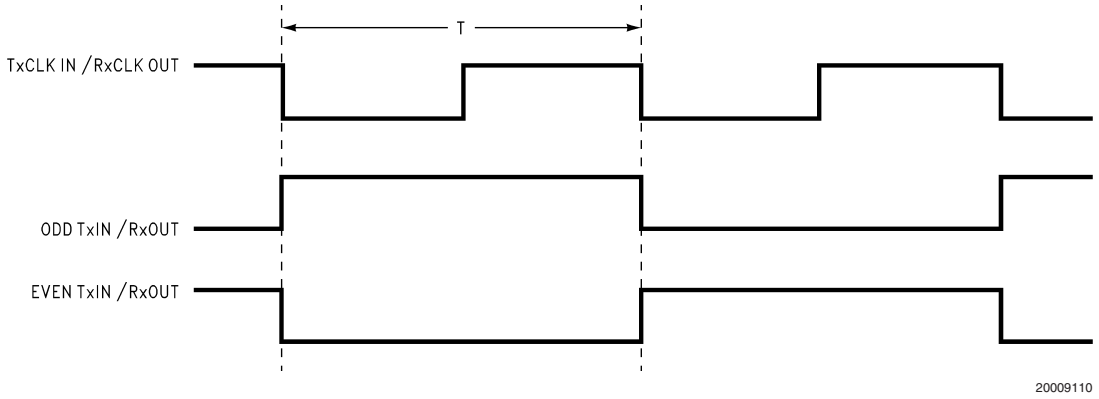


FIGURE 1. "Worst Case" Test Pattern

Note 8: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

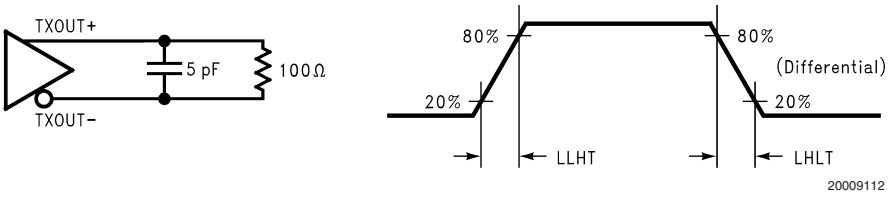


FIGURE 2. DS90CR481 (Transmitter) LVDS Output Load and Transition Times

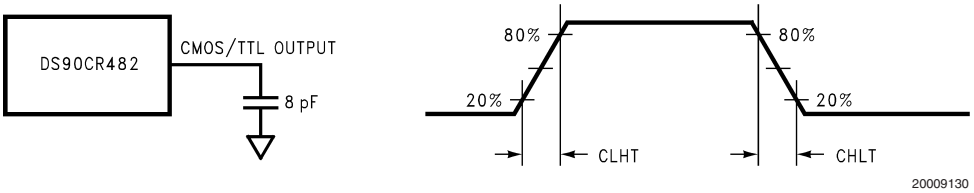


FIGURE 3. DS90CR482 (Receiver) CMOS/TTL Output Load and Transition Times

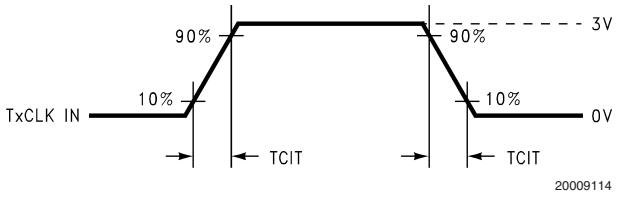


FIGURE 4. DS90CR481 (Transmitter) Input Clock Transition Time

AC Timing Diagrams (Continued)

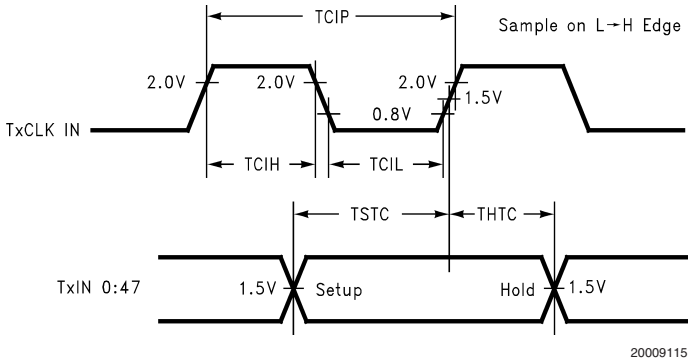


FIGURE 5. DS90CR481 (Transmitter) Setup/Hold and High/Low Times

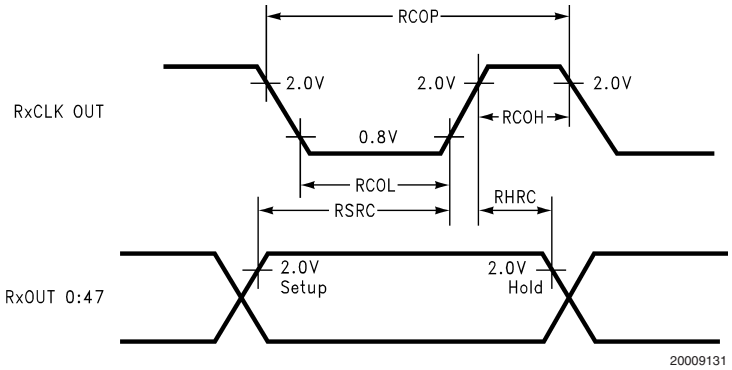


FIGURE 6. DS90CR482 (Receiver) Setup/Hold and High/Low Times

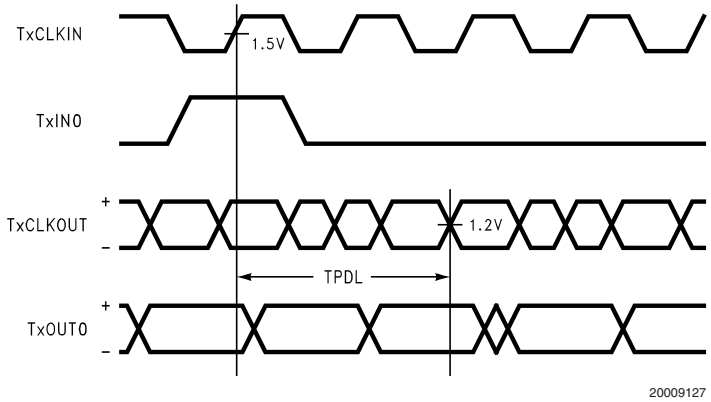


FIGURE 7. DS90CR481 (Transmitter) Propagation Delay - Latency

AC Timing Diagrams (Continued)

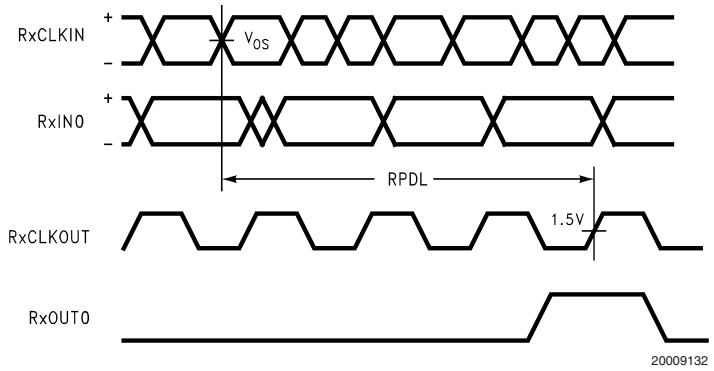


FIGURE 8. DS90CR482 (Receiver) Propagation Delay - Latency

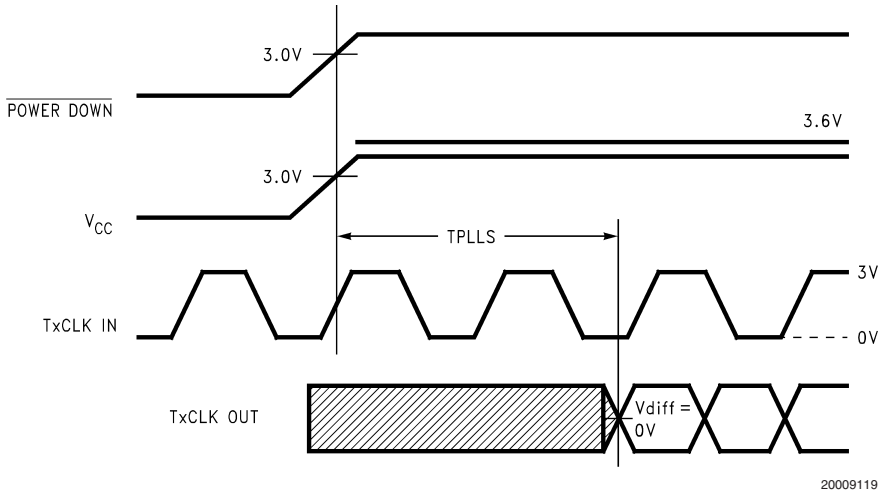


FIGURE 9. DS90CR481 (Transmitter) Phase Lock Loop Set Time

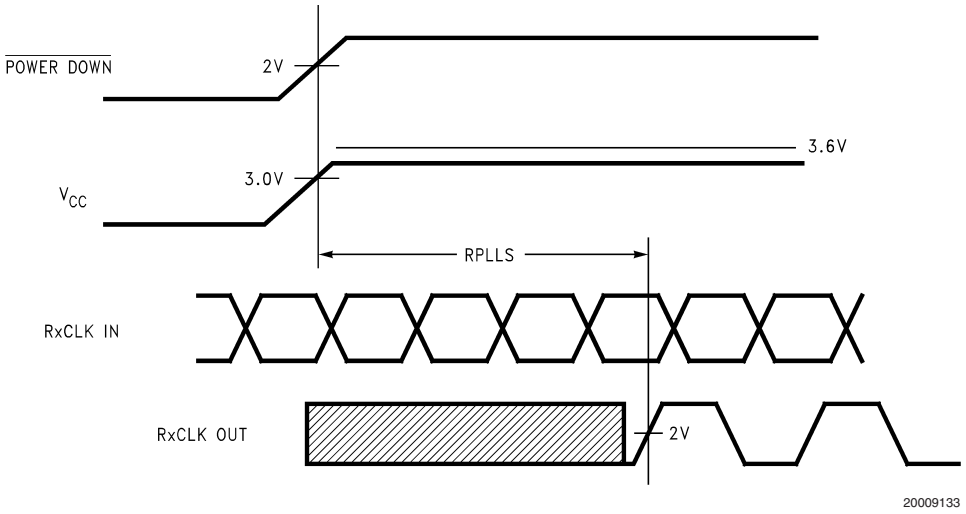


FIGURE 10. DS90CR482 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

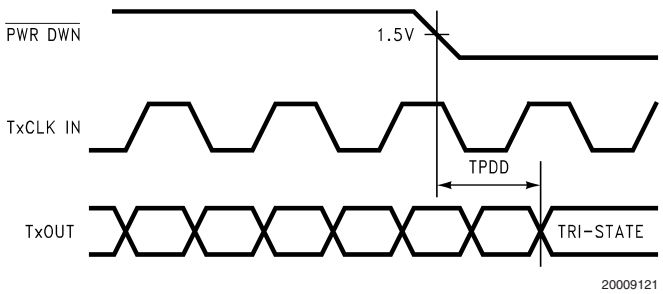


FIGURE 11. DS90CR481 (Transmitter) Power Down Delay

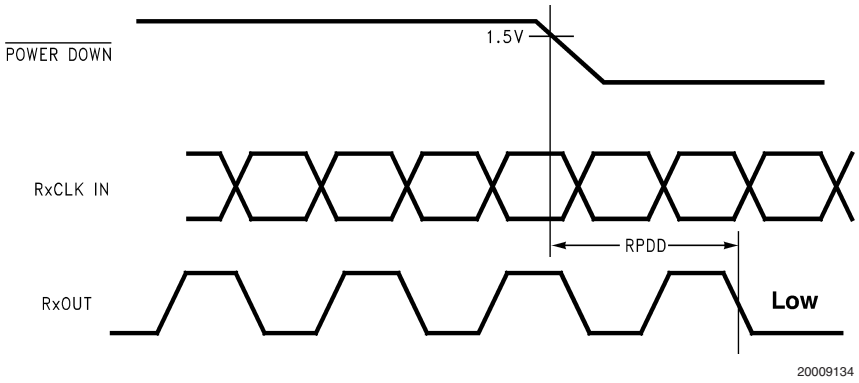
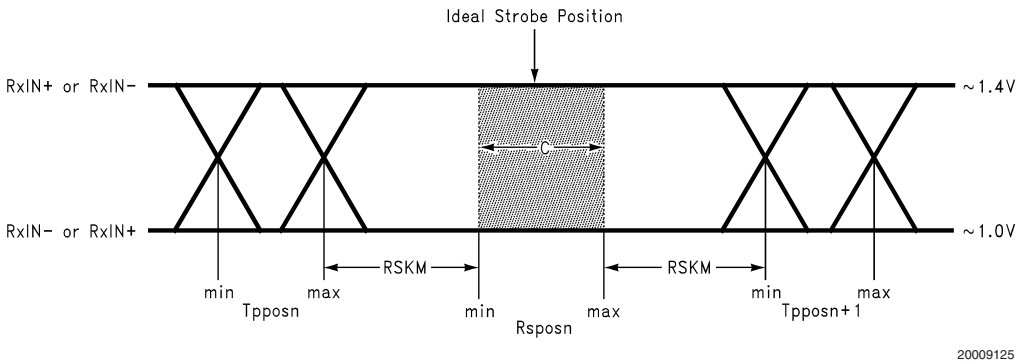


FIGURE 12. DS90CR482 (Receiver) Power Down Delay

AC Timing Diagrams (Continued)



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

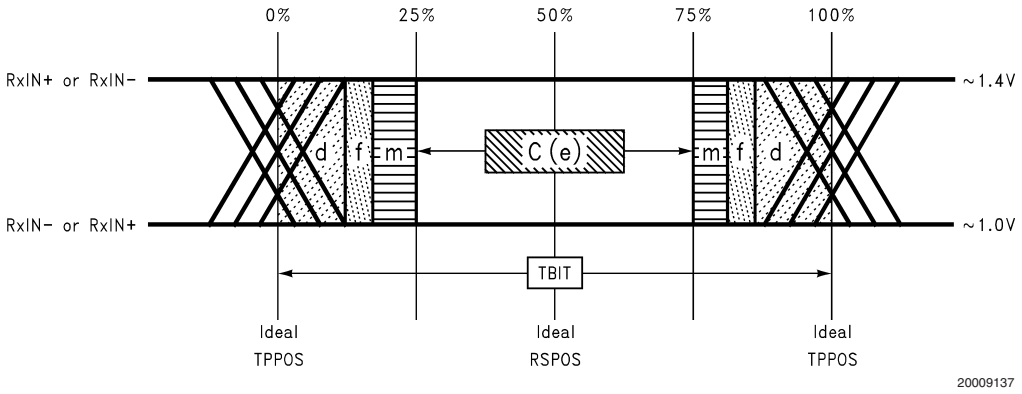
Tppos — Transmitter output pulse position (min and max)

RSKM ≥ Cable Skew (type, length) + LVDS Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)

- Cable Skew — typically 10 ps–40 ps per foot, media dependent
- Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate).
- ISI is dependent on interconnect length; may be zero

See Applications Information section for more details.

FIGURE 13. Receiver Skew Margin (RSKM) for Chipset without DESKEW



C — Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

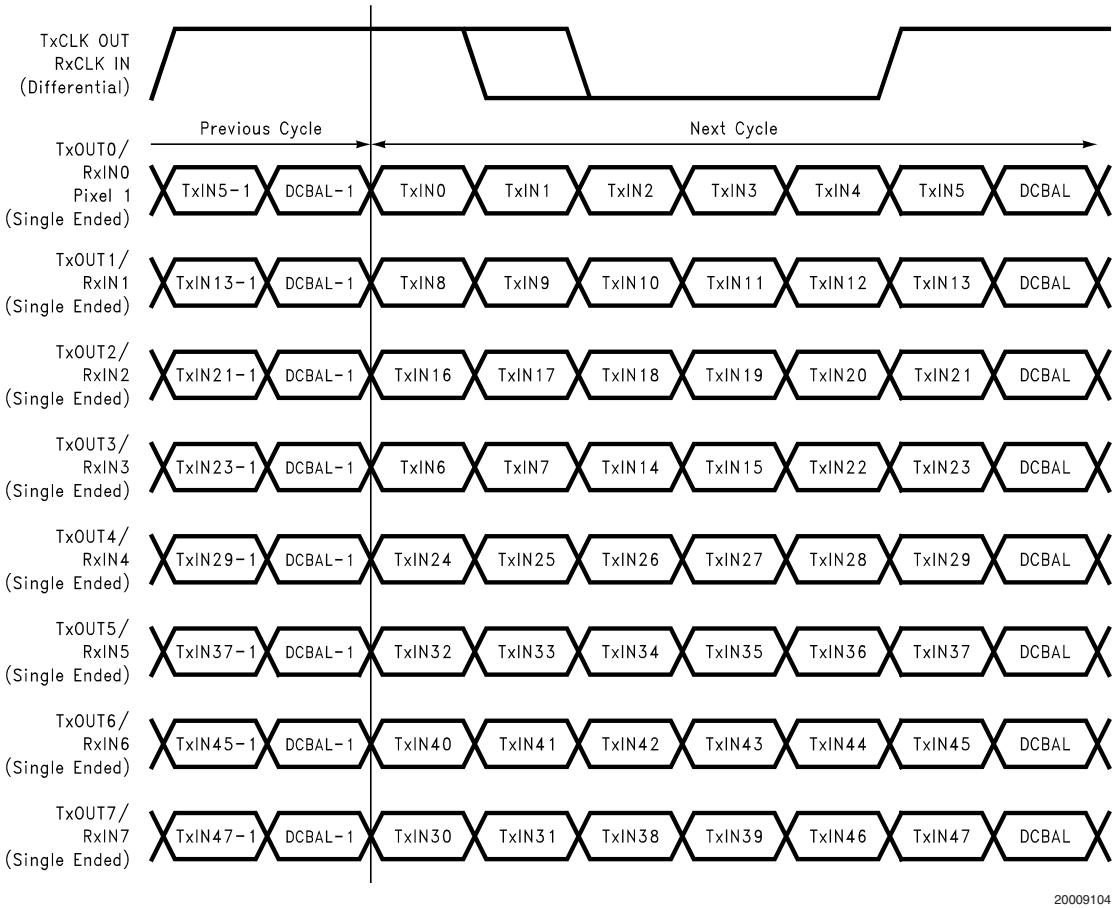
RSKMD ≥ TPPOSvariance (d) + TJCC (output jitter)(f) + ISI (m)

- d= Tppos — Transmitter output pulse position (min and max)
- f= Cycle-to-cycle LVDS Output jitter (TJCC) is less than 100 ps (worse case estimate)
- m= extra margin - assigned to ISI in long cable applications

See Applications Informations section for more details.

FIGURE 14. Receiver Skew Margin (RSKMD) for Chipset with DESKEW

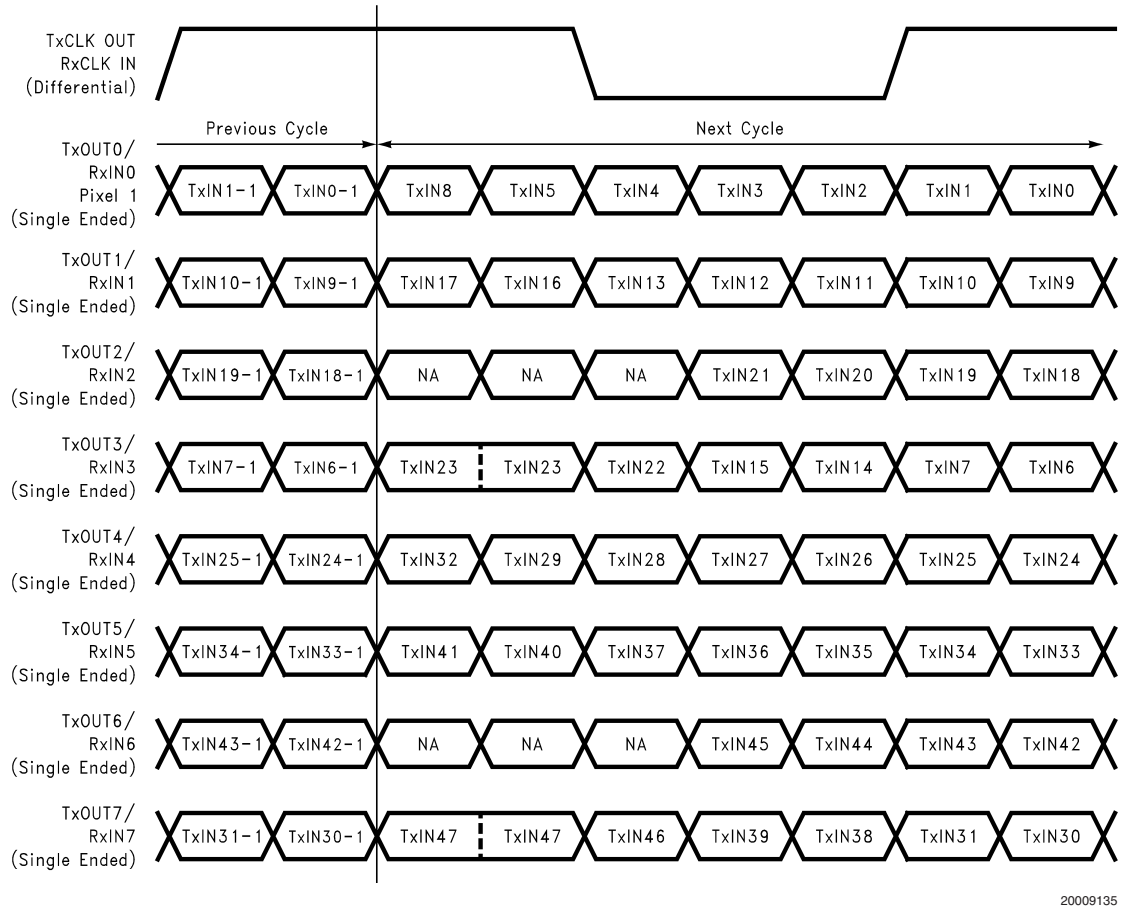
LVDS Interface



Optional features supported: Pre-emphasis and DESKEW

FIGURE 15. 48 Parallel TTL Data Bits Mapped to LVDS Bits with DC Balance Enabled

LVDS Interface (Continued)



Optional feature supported: Pre-emphasis

FIGURE 16. 48 Parallel TTL Data Bits Mapped to LVDS Bits with DC Balance Disabled

Applications Information

The DS90CR481/DS90CR482 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pull up resistor to Vcc; please refer to *Table 1* to set the level needed. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to ±1 LVDS data bit time (up to 80 MHz clock rates). For details on deskew, refer to "Deskew" section below. These three enhancements allow cables 5+ meters in length to be driven depending upon media and clock rate.

The DS90CR481/482 chipset may also be used in a non-DC Balance mode. In this mode pre-emphasis is supported. In this mode, the chipset is also compatible with 21 and 28-bit Channel Link Receivers. See *Figure 16* for the LVDS mapping.

NEW FEATURES DESCRIPTION

1. Pre-emphasis

Adds extra current during LVDS logic transition to reduce the cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to Vcc) at the "PRE" pin. A higher input voltage on the "PRE" pin increases the magnitude of dynamic current during data transition. The "PRE" pin requires one pull-up resistor (Rpre) to Vcc in order to set the DC level. There is an internal resistor network, which cause a voltage drop. Please refer to the tables below to set the voltage level.

The waveshape at the Receiver input should not exhibit over or undershoot with the proper amount of pre-emphasis set. Too much pre-emphasis generates excess noise and increases power dissipation. Cables less than 2 meters in length typically do not require pre-emphasis.

TABLE 1. Pre-emphasis DC voltage level with (Rpre)

Rpre	Resulting PRE Voltage	Effect
1MΩ or NC	0.75V	Standard LVDS
50kΩ	1.0V	
9kΩ	1.5V	50% pre-emphasis
3kΩ	2.0V	
1kΩ	2.6V	
100Ω	Vcc	100% pre-emphasis

TABLE 2. Pre-emphasis needed per cable length

Frequency	PRE Voltage	Typical cable length
112MHz	1.0V	2 meters
112MHz	1.5V	5 meters
80MHz	1.0V	2 meters
80MHz	1.2V	5+ meters
66MHz	1.5V	7 meters

Note 9: This is based on testing with standard shield twisted pair cable. The amount of pre-emphasis will vary depending on the type of cable, length and operating frequency.

2. DC Balance

In addition to data information an additional bit is transmitted on every LVDS data signal line during each cycle as shown in *Figure 15*. This bit is the DC balance bit (DCBAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word shall be calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and −6. The running word disparity shall be calculated as a continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity shall saturate at +7 and −6.

The value of the DC balance bit (DCBAL) shall be 0 when the data is sent unmodified and 1 when the data is sent inverted. To determine whether to send data unmodified or inverted, the running word disparity and the current data disparity are used. If the running word disparity is positive and the current data disparity is positive, the data shall be sent inverted. If the running word disparity is positive and the current data disparity is zero or negative, the data shall be sent unmodified. If the running word disparity is negative and the current data disparity is positive, the data shall be sent unmodified. If the running word disparity is negative and the

Applications Information (Continued)

current data disparity is zero or negative, the data shall be sent inverted. If the running word disparity is zero, the data shall be sent inverted.

DC Balance mode is set when the BAL pin on the transmitter is tied HIGH - see pin descriptions. DC Balancing is useful on long cable applications which are typically greater than 5 meters in length.

3. Deskew

Deskew is supported in the DC Balance mode only (BAL = high on DS90CR481). The "DESKEW" pin on the receiver when set high will deskew a minimum of ±1 LVDS data bit time skew from the ideal strobe location between signals arriving on independent differential pairs (pair-to-pair skew). It is required that the "DS_OPT" pin on the Transmitter must be applied low for a minimum of four clock cycles to complete the deskew operation. It is also required that this must be performed at least once at any time after the PLLs have locked to the input clock frequency. If power is lost, or if the cable has been switched, this procedure must be repeated or else the receiver may not sample the incoming LVDS data correctly. When the receiver is in the deskew mode, all receiver outputs are set to a LOW state, but the receiver clock output is still active and switching. Setting the "DESKEW" pin to low will disable the deskew operation and allow the receiver to operation on a fixed data sampling strobe. In this case, the "DS_OPT" pin on the transmitter must then be set high.

The DS_OPT pin at the input of the transmitter (DS90CR481) is used to initiate the deskew calibration pattern. It must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. For this reason, the LVDS clock signal with DS_OPT applied high (active data sampling) shall be 1111000 or 1110000 pattern. During the deskew operation with DS_OPT applied low, the LVDS clock signal shall be 1111100 or 1100000 pattern. The transmitter will also output a series of 1111000 or 1110000 onto the LVDS data lines (TxOUT 0-7) during deskew so that the receiver can automatically calibrated the data sampling strobes at the receiver inputs. Each data channel is deskewed independently and is tuned with a step size of 1/3 of a bit time over a range of +/−1 TBIT from the ideal strobe location. The Deskew feature operates up to clock rates of 80 MHz only. If the Receiver is enabled in the deskew mode, then it must be trained before data transfer.

CLOCK JITTER

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. Cycle-to-cycle jitter has been measured over frequency to be less than 100 ps with input step function jitter applied. This should be subtracted from the RSKM/RSKMD budget as shown and described in *Figure 13* and *Figure 14*. This rejection capability significantly reduces the impact of jitter at the TXinput clock pin, and improves the accuracy of data sampling in the receiver. Transmitter output jitter is effected by PLLVCC noise and input clock jitter - minimize supply noise and use a low jitter clock source to limit output jitter. The falling edge of the input clock to the transmitter is the critical edge and is used by the PLL circuit.

RSKM - RECEIVER SKEW MARGIN

RSKM is a chipset parameter and is explained in AN-1059 in detail. It is the difference between the transmitter's pulse position and the receiver's strobe window. RSKM must be greater than the summation of: Interconnect skew, LVDS Source Clock Jitter (TJCC), and ISI (if any). See *Figure 13*. Interconnect skew includes PCB traces differences, connector skew and cable skew for a cable application. PCB trace and connector skew can be compensated for in the design of the system. Cable skew is media type and length dependant.

RSKMD - RECEIVER SKEW MARGIN WITH DESKEW

RSKMD is a chipset parameter and is applicable when the DESKEW feature of the DS90CR482 is employed. It is the difference between the receiver's strobe window and the ideal pulse locations. The DESKEW feature adjusts for skew between each data channel and the clock channel. This feature is supported up to 80MHz clock rate. RSKMD must be greater than the summation of: Transmitter's Pulse Position variance, LVDS Source Clock Jitter (TJCC), and ISI (if any). See *Figure 14*. With DESKEW, RSKMD will be a minimum of 25% of TBIT. Deskew compensates for interconnect skew which includes PCB traces differences, connector skew and cable skew (for a cable application). PCB trace and connector skew can be compensated for in the design of the system. Note, cable skew is media type and length dependant. Cable length may be limited by the RSKMD parameter prior to the interconnect skew reaching 1 TBIT in length due to ISI effects.

POWER DOWN

Both transmitter and receiver provide a power down feature. When asserted current draw through the supply pins is minimized and the PLLs are shut down. The transmitter outputs are in TRI-STATE when in power down mode. The receiver outputs are forced to a active LOW state when in the power down mode. (See Pin Description Tables). The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

CONFIGURATIONS

The transmitter is designed to be connected typically to a single receiver load. This is known as a point-to-point configuration. It is also possible to drive multiple receiver loads if certain restrictions are made. Only the final receiver at the end of the interconnect should provide termination across the pair. In this case, the driver still sees the intended DC load of 100 Ohms. Receivers connected to the cable between the transmitter and the final receiver must not load down the signal. To meet this system requirement, stub lengths from the line to the receiver inputs must be kept very short.

CABLE TERMINATION

A termination resistor is required for proper operation to be obtained. The termination resistor should be equal to the differential impedance of the media being driven. This should be in the range of 90 to 132 Ohms. 100 Ohms is a typical value common used with standard 100 Ohm twisted pair cables. This resistor is required for control of reflections and also to complete the current loop. It should be placed as close to the receiver inputs to minimize the stub length from the resistor to the receiver input pins.

Applications Information (Continued)

HOW TO CONFIGURE FOR BACKPLANE APPLICATIONS

In a backplane application with differential line impedance of 100Ω the differential line pair-to-pair skew can controlled by trace layout. The transmitter-DS90CR481 "DS_OPT" pin may be set high. In a backplane application with short PCB distance traces, pre-emphasis from the transmitter is typically not required. The "PRE" pin should be left open (do not tie to ground). A resistor pad provision for a pull up resistor to Vcc can be implemented in case pre-emphasis is needed to counteract heavy capacitive loading effects.

HOW TO CONFIGURE FOR CABLE INTERCONNECT APPLICATIONS

In applications that require the long cable drive capability. The DS90CR481/DS90CR482 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with the use of DC balanced data transmission, pre-emphasis. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pull up resistor to Vcc; please refer to *Table 1* to set the level needed. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference) for long cable applications. With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. These enhancements allow cables 5+ meters in length to be driven. Depending upon clock rate and the media being driven, the cable Deskew feature may also be employed - see discussion on DESKEW, RSKM and RSKMD above.

SUPPLY BYPASS RECOMMENDATIONS

Bypass capacitors must be used on the power supply pins. Different pins supply different portions of the circuit, therefore capacitors should be nearby all power supply pins except as noted in the pin description table. Use high frequency ceramic (surface mount recommended) 0.1µF capacitors close to each supply pin. If space allows, a 0.01µF capacitor should be used in parallel, with the smallest value closest to the device pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple (large) via should be used to connect the decoupling capacitors to the power plane. A 4.7 to 10 µF bulk cap is recommended near the PLLVCC pins and also the LVDSVCC (pin #40) on the Transmitter. Connections between the caps and the pin should use wide traces.

INPUT SIGNAL QUALITY REQUIREMENTS - TRANSMITTER

The input signal quality must comply to the datasheet requirements, please refer to the "Recommended Transmitter Input Characteristics" table for specifications. In addition undershoots in excess of the ABS MAX specifications are not recommended. If the line between the host device and the transmitter is long and acts as a transmission line, then termination should be employed. If the transmitter is being driven from a device with programmable drive strengths, data inputs are recommended to be set to a weak setting to prevent transmission line effects. The clock signal is typically set higher to provide a clean edge that is also low jitter.

UNUSED LVDS OUTPUTS

Unused LVDS output channels should be terminated with 100 Ohm at the transmitter's output pin.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - — S = space between the pair
  - — 2S = space between pairs
  - — 3S = space to TTL signal
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Minimize skew between pairs
- Terminate as close to the RXinputs as possible

RECEIVER OUTPUT DRIVE STRENGTH

The DS90CR482 output specify a 8pF load, V_{OH} and V_{OL} are tested at ± 2mA, which is intended for only 1 or maybe 2 loads. If high fan-out is required or long transmission line driving capability, buffering the receiver output is recommended. Receiver outputs do not support / provide a TRI-STATE function.

DS90CR483/484

The DS90CR481/2 chipset is electrically similar to the DS90CR483/4. The DS90CR481/2 differ only in the control circuit of the internal PLL and are specified for 65 to 112 MHz operation. The devices will directly inter-operate within the scope of the respective datasheets.

FOR MORE INFORMATION

Channel Link Applications Notes currently available:

- AN-1041 Introduction to Channel Link
- AN-1059 RSKM Calculations
- AN-1108 PCB and Interconnect Guidelines
- AN-905 Differential Impedance
- National's LVDS Owner's Manual

DS90CR481 Pin Descriptions—Channel Link Transmitter

Pin Name	I/O	Description
TxIN	I	TTL level input. (Note 10).
TxOUTP	O	Positive LVDS differential data output.
TxOUTM	O	Negative LVDS differential data output.
TxCLKIN	I	TTL level clock input. The rising edge acts as data strobe.
TxCLKP	O	Positive LVDS differential clock output.
TxCLKM	O	Negative LVDS differential clock output.
$\overline{PD}$	I	TTL level input. Assertion (low input) tri-states the outputs, ensuring low current at power down. (Note 10).
PLLSEL	I	PLL range select. This pin must be tied to V_{CC}. NC or tied to Ground is reserved for future use. (Note 10)
PRE	I	Pre-emphasis “level” select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines Pre-emphasis level (See Applications Information Section). For normal LVDS drive level (No Pre-emphasis) leave this pin open (do not tie to ground).
DS_OPT	I	Cable Deskew performed when TTL level input is low. No TxIN data is sampled during Deskew. To perform Deskew function, input must be held low for a minimum of 4 clock cycles. The Deskew operation is normally conducted after the TX and RX PLLs have locked. It should also be conducted after a system reset, or a reconfiguration event. It must be peformed at least once when "DESKEW" is enabled. (Note 10)
BAL	I	TTL level input. This pin was previously labeled as V_{CC}, which enabled the DC Balance function. But when tied low or left open, the DC Balance function is disabled. Please refer to (*Figures 15, 16*) for LVDS data bit mapping respectively. (Note 10), (Note 12)
V_{CC}	I	Power supply pins for TTL inputs and digital circuitry. Bypass not required on Pins 20 and 21.
GND	I	Ground pins for TTL inputs and digital circuitry.
$PLLV_{CC}$	I	Power supply pin for PLL circuitry.
PLLGND	I	Ground pins for PLL circuitry.
$LVDSV_{CC}$	I	Power supply pin for LVDS outputs.
LVDSGND	I	Ground pins for LVDS outputs.
NC		No Connect. Make NO Connection to these pins - leave open.

Note 10: Inputs default to “low” when left open due to internal pull-down resistor.

DS90CR482 Pin Descriptions—Channel Link Receiver

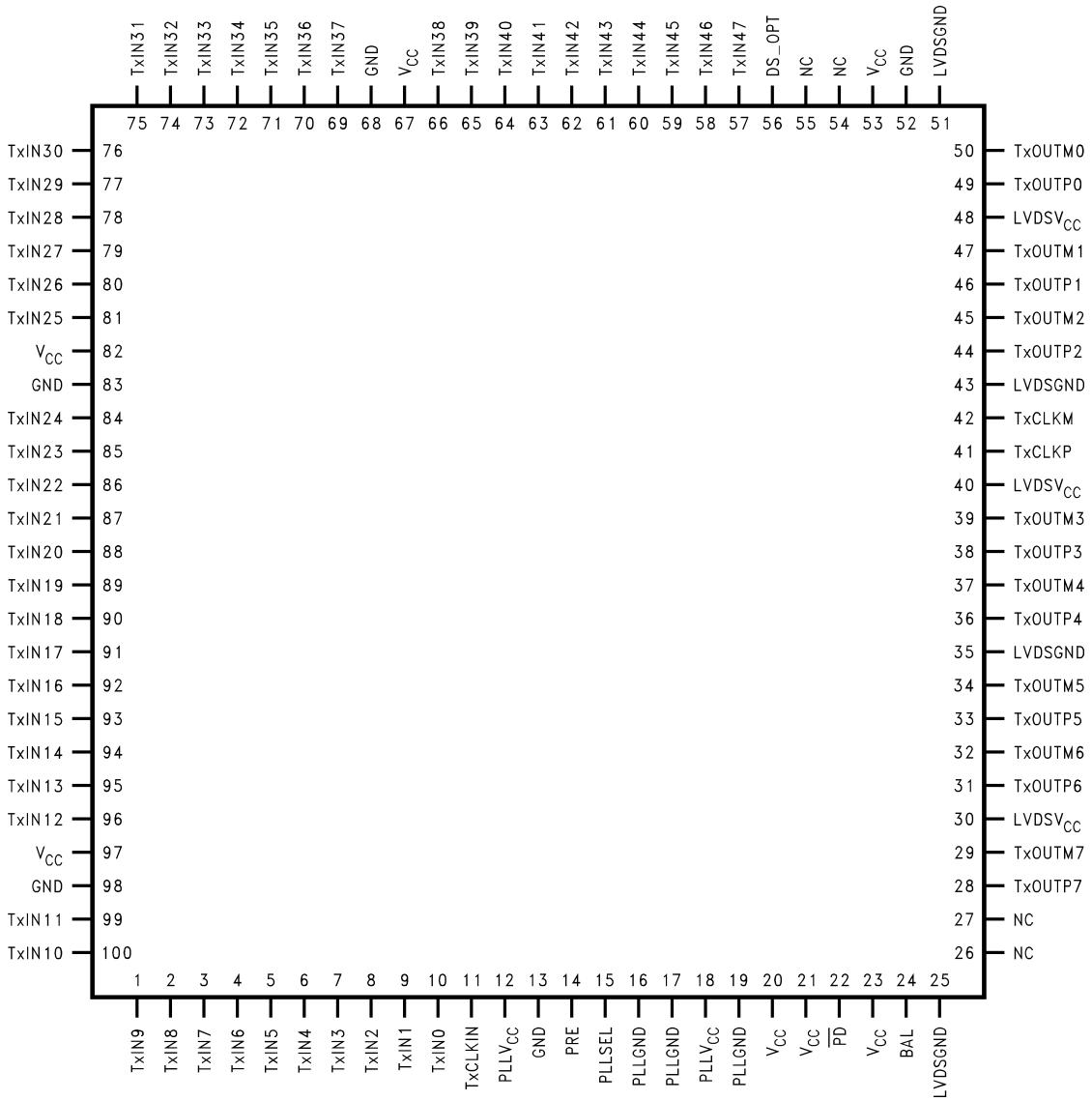
Pin Name	I/O	Description
RxINP	I	Positive LVDS differential data inputs.
RxINM	I	Negative LVDS differential data inputs.
RxOUT	O	TTL level data outputs. In PowerDown ($\overline{PD}$ = Low) mode, receiver outputs are forced to a Low state.
RxCLKP	I	Positive LVDS differential clock input.
RxCLKM	I	Negative LVDS differential clock input.
RxCLKOUT	O	TTL level clock output. The rising edge acts as data strobe.
PLLSEL	I	PLL range select. This pin must be tied to V_{CC}. NC or tied to Ground is reserved for future use. (Note 10)
DESKEW	I	Deskew / Oversampling “on/off” select. When using the Deskew / Oversample feature this pin must be tied to V_{CC}. Tieing this pin to ground disables this feature. (Note 10) Deskew is only supported in the DC Balance mode.
$\overline{PD}$	I	TTL level input. When asserted (low input) the receiver outputs are Low. (Note 10)
V_{CC}	I	Power supply pins for TTL outputs and digital circuitry. Bypass not required on Pins 6 and 77.
GND	I	Ground pins for TTL outputs and digital circuitry.
$PLLV_{CC}$	I	Power supply for PLL circuitry.
PLLGND	I	Ground pin for PLL circuitry.
$LVDSV_{CC}$	I	Power supply pin for LVDS inputs.
LVDSGND	I	Ground pins for LVDS inputs.
NC		No Connect. Make NO Connection to these pins - leave open.

Note 11: These receivers have input fail-safe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under test conditions receiver inputs will be in a HIGH state. If the cable interconnect (media) are disconnected which results in floating/terminated inputs, the outputs will remain in the last valid state.

Note 12: The DS90CR482 is design to automatically detect the DC Balance or non-DC Balance transmitted data from the DS90CR481 and deserialize the LVDS data according to the define bit mapping.

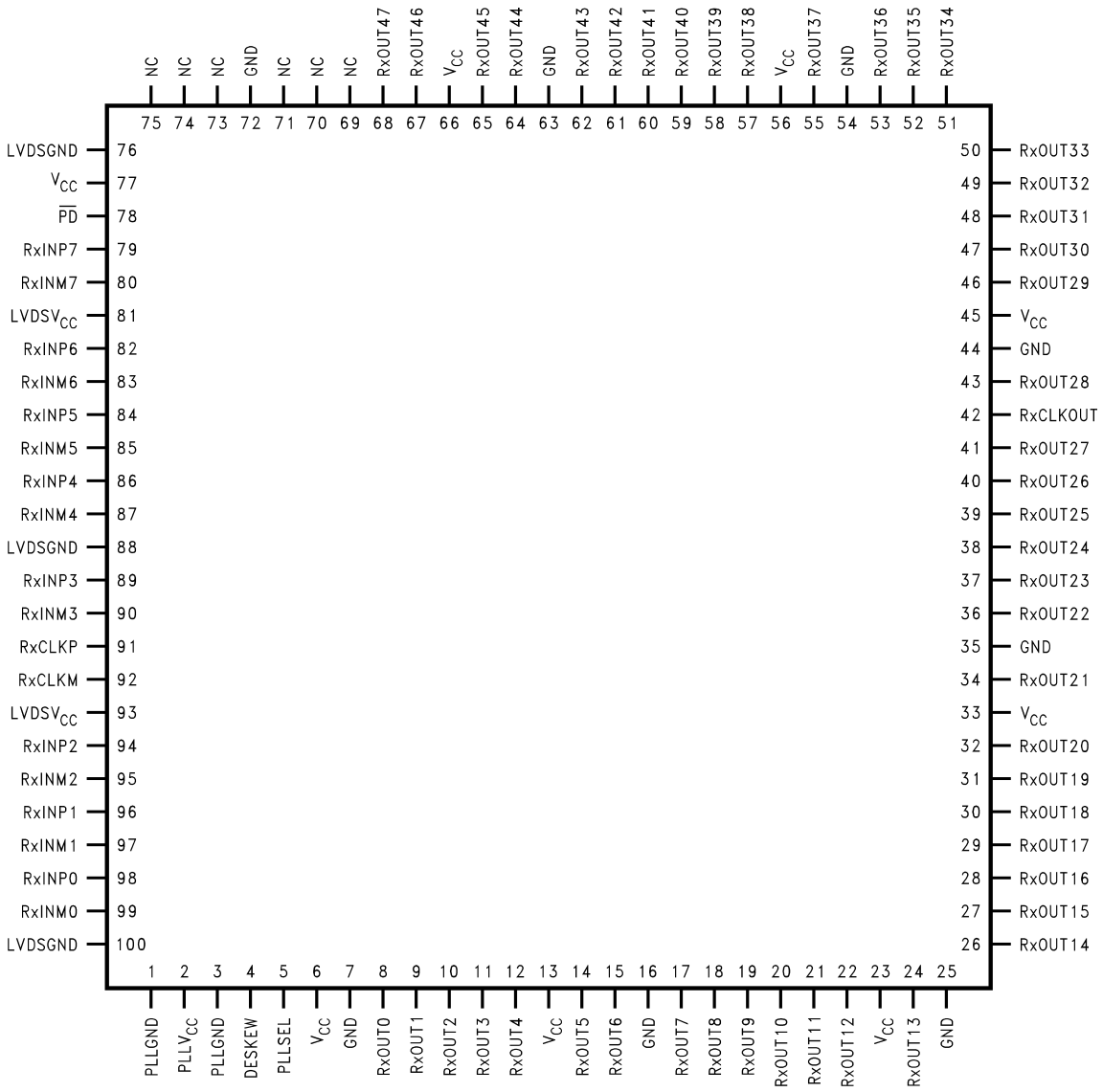
DS90DR481 — Connection Diagram

Transmitter - DS90CR481 - TQFP - Top View



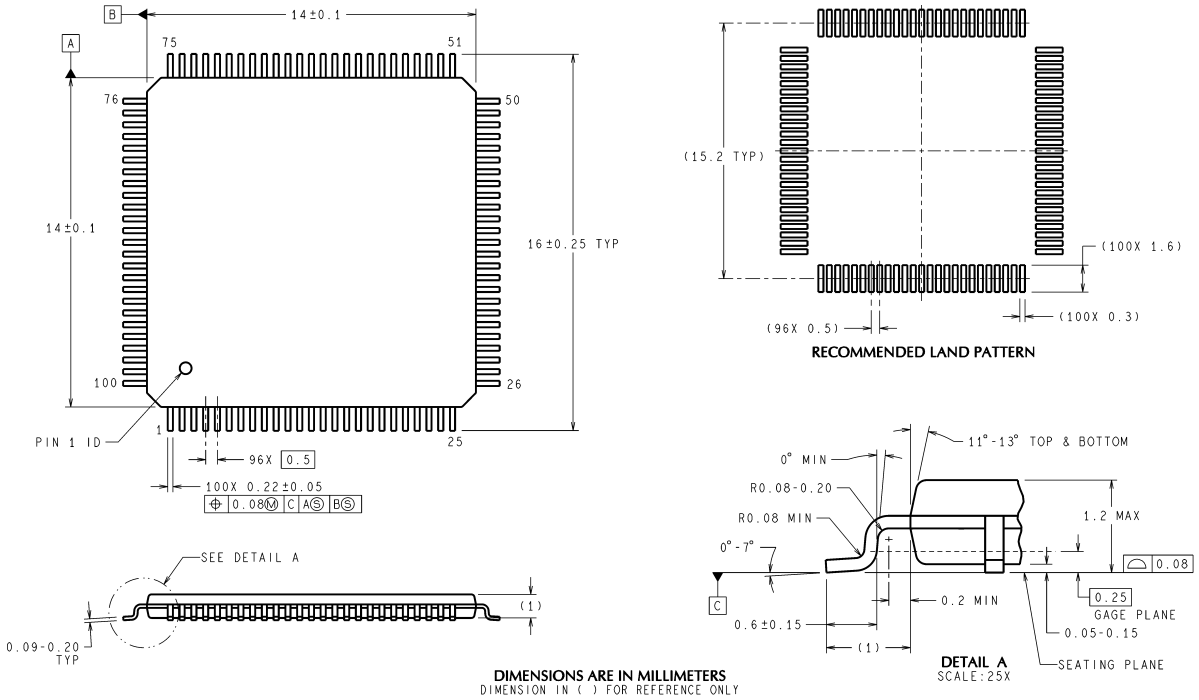
DS90CR482 – Connection Diagram

Receiver - DS90CR482 - TQFP - Top View



20009107

Physical Dimensions inches (millimeters) unless otherwise noted



Dimensions show in millimeters only
Order Number DS90CR481VJD or DS90CR482VS
NS Package Number VJD100A

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560