National Semiconductor

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LM3218
650 mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

General Description

The LM3218 is a DC-DC converter with inductor which is optimized for powering RF power amplifiers (PAs) from a single Lithium-Ion cell. It steps down an input voltage in the range from 2.7V to 5.5V to an adjustable output voltage of 0.8V to 3.6V. Output voltage is set by using a V_{CON} analog input to control power levels and efficiency of the RF PA.

The LM3218 offers superior electrical performance for mobile phones and similar RF PA applications with a reduced footprint (3mm x 2.5mm x 1.2mm). Fixed-frequency PWM operation minimizes RF interference. A shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ.).

The LM3218 is available in an integrated inductor 8–pin LTCC package. A high switching frequency (2 MHz typ.) allows use of tiny surface-mount components. Only two small external surface-mount components, two ceramic capacitors, are required. The overall board space is reduced up to 25% from the typical discrete inductor solution.

Features

- Includes 2.6 µH Inductor in very small form factor (3mm x 2.5mm x 1.2mm)
- 2 MHz (typ.) PWM Switching Frequency
- Operates from a single Li-Ion cell (2.7V to 5.5V)
- Adjustable Output Voltage (0.8V to 3.6V)
- Fast Output Voltage Transient (0.8V to 3.4V in 25 µs typ.)
- 650 mA Maximum load capability
- High Efficiency (95% typ. at 3.9 V_{IN}, 3.4 V_{OUT} at 400 mA)
- 8-pin LTCC Package
- Current Overload Protection
- Thermal Overload Protection

Applications

- Cellular Phones
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices

Typical Application

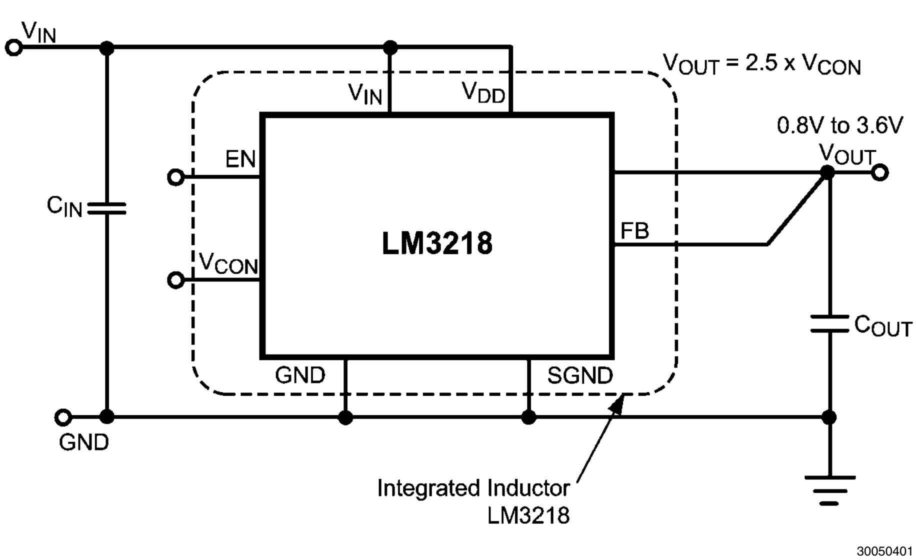
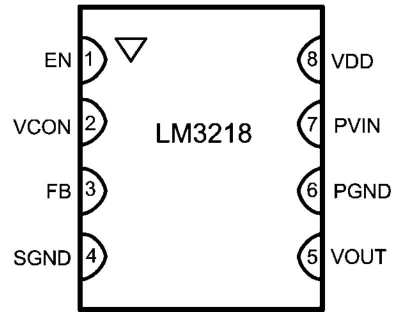


FIGURE 1. LM3218 Typical Application

Connection Diagram



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NS Package Number SE08A

Order Information

Order Number	Package Marking (Note)	Supplied As
LM3218SE	XVS SA	250 units, Tape-and-Reel
LM3218SEX	XVS SA	3000 units, Tape-and-Reel

Note: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the date code. "V" is a NSC internal code for die traceability. Both will vary in production. "S" designates device type as switcher and "SA" identifies the device (part number).

Pin Descriptions

Pin #	Name	Description
1	EN	Enable Input. Set this digital input high for normal operation. For shutdown, set low.
2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
3	FB	Feedback Analog Input. Connect to the V_{OUT} pin.
4	SGND	Analog and Control Ground.
5	V_{OUT}	Output Voltage, connects to one terminal of 2.6 µH inductor. Connect output filter capacitor C2 to get DC voltage out.
6	PGND	Power Ground
7	PV_{IN}	Power Supply Voltage Input to the internal Buck PFET switch.
8	V_{DD}	Analog Supply Input.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{DD}, PV_{IN} to SGND	−0.2V to +6.0V
PGND to SGND	−0.2V to +0.2V
EN, FB, V_{CON}	(SGND −0.2V) to (V_{DD} +0.2V) w/6.0V max
V_{OUT}	(PGND −0.2V) to (PV_{IN} +0.2V) w/6.0V max
PV_{IN} to V_{DD}	−0.2V to +0.2V
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	+260°C
ESD Rating (Notes 4, 13)	
Human Body Model:	2000V
Machine Model:	200V

Operating Ratings (Notes 1, 2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0 mA to 650 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (Note 5)	−30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), TLP08 Package (Note 6)	120°C/W

Electrical Characteristics

(Notes 2, 7, 8) Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +85°C$). Unless otherwise noted, all specifications apply to the LM3218 with: $PV_{IN} = V_{DD} = EN = 3.6V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB, MIN}$	Feedback voltage at minimum setting	V_{CON} = 0.32V V_{IN} = 3.6V(Note 8)	**0.75**	0.80	**0.85**	V
$V_{FB, MAX}$	Feedback voltage at maximum setting	V_{CON} = 1.44V, V_{IN} = 4.2V(Note 8)	**3.526**	3.600	**3.696**	V
I_{SHDN}	Shutdown supply current	EN = V_{OUT} = V_{CON} = 0V, (Note 9)		0.01	**2**	µA
I_Q	DC bias current into V_{DD}	V_{CON} = 0V, FB = 0V, No Switching (Note 10)		0.6	**0.7**	mA
$R_{DROPOUT}$	Pin_{Vout} - Pin_{Vin} resistance	I_{OUT} = 200mA, V_{CON} = 0.5V		300	**400**	mΩ
I_{LIM} (L_PFET)	Large PFET (L) Switch peak current limit	V_{CON} = 0.5V (Note 11)		1100		mA
I_{LIM} (S_PFET)	Small PFET (S) Switch peak current limit	V_{CON} = 0.32V (Note 11)		800		mA
F_{OSC}	Internal oscillator frequency			2.0		MHz
$V_{IH,ENABLE}$	Logic high input threshold		**1.2**			V
$V_{IL,ENABLE}$	Logic low input threshold				**0.5**	V
$I_{PIN,ENABLE}$	Pin pull down current	EN = 3.6V		5	**10**	µA
$V_{CON,ON}$	V_{CON} Threshold for turning on switches			0.15		V
I_{CON}	V_{CON} pin leakage current	V_{CON} = 1.0V			**±1**	µA
Gain	V_{CON} to V_{OUT} Gain	$0.32V \le V_{CON} \le 1.44V$		2.5		V/V

System Characteristics

The following spec table entries are guaranteed by design providing the component values in the typical application circuit are used (L = LTCC Inductor, 2.6 µH; DCR = 150 mΩ; C_{IN} = 10 µF, 6.3V, 0603, TDK C1608X5R0J106K; C_{OUT} = 4.7 µF, 6.3V, 0603, C1608X5R0J475M). **These parameters are not guaranteed by production testing.** Min and Max values are specified over the ambient temperature range T_A = –30°C to 85°C. Typical values are specified at PV_{IN} = V_{DD} = EN = 3.6V and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{RESPONSE}$ (Rise Time)	Time for V_{OUT} to rise from 0.8V to 3.4V (to reach 3.35V)	V_{IN} = 4.2V R_{LOAD} = 5.5Ω		25	40	µs
$T_{RESPONSE}$ (Fall Time)	Time for V_{OUT} to fall from 3.4V to 0.8V	V_{IN} = 4.2V R_{LOAD} = 15Ω		35	45	µs
C_{CON}	V_{CON} input capacitance	V_{CON} = 1V, V_{IN}=2.7V to 5.5V Test frequency = 100 KHz		5	10	pF
C_{EN}	EN input capacitance	EN = 2V, V_{IN}= 2.7V to 5.5V Test frequency = 100 KHz		5	10	pF
V_{CON} (S>L)	$R_{DSON(P)}$ management threshold	Threshold for PFET $R_{DSON(P)}$ to change from 960 mΩ to 140 mΩ	**0.39**	0.42	**0.45**	V
V_{CON} (L>S)	$R_{DSON(P)}$ management threshold	Threshold for PFET $R_{DSON(P)}$ to change from 140 mΩ to 960 mΩ	**0.37**	0.40	**0.43**	V
$I_{OUT,\ MAX}$	Maximum Output Current	V_{IN} = 2.7V to 5.5V V_{CON} = 0.45V to 1.44V	650			mA
		V_{IN} = 2.7V to 5.5V V_{CON} = 0.32V to 0.45V	400			mA
Linearity	Linearity in control range 0.32V to 1.44V	V_{IN} = 3.9V (Note 14) Monotonic in nature	–3		+3	%
			–50		+50	mV
T_{ON}	Turn on time (time for output to reach 97% of final value after Enable low-to-high transition)	EN = Low to High V_{IN} = 4.2V, V_{OUT} = 3.4V, I_{OUT} ≤ 1mA		40	60	µs
η	Efficiency	V_{IN} = 3.6V, V_{OUT} = 0.8V I_{OUT} = 90mA		81		%
		V_{IN} = 3.6V, V_{OUT} = 1.5V I_{OUT} = 150mA		89		%
		V_{IN} = 3.9V, V_{OUT} = 3.4V I_{OUT} = 400 mA		95		%
V_O_ripple	Ripple voltage at no pulse skip condition	V_{IN} = 2.7V to 4.5V, V_{OUT} = 0.8V to 3.4V, Differential voltage = V_{IN} - V_{OUT} > 1V, I_{OUT} = 0 mA to 400 mA (Note 12)		10		mVp-p
	Ripple voltage at pulse skip condition	V_{IN} = 5.5V to dropout, V_{OUT} = 3.4V, I_{OUT} = 650 mA (Note 12)		60		mVp-p
Line_tr	Line transient response	V_{IN} = 3.6V to 4.2V, T_R = T_F = 10 µs, V_{OUT} = 0.8V, I_{OUT} = 100 mA		50		mVpk
Load_tr	Load transient response	V_{IN} = 3.1/3.6/4.5V, V_{OUT} = 0.8V, I_{OUT} = 50 mA to 150 mA		50		mVpk
Max Duty cycle	Maximum duty cycle		100			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins. The LM3218 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.7V.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).

Note 4: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin.

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 6: Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. A 4–layer, 4" x 4", 2/1/1/2 oz. Cu board as per JEDEC standards is used for the measurements.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm. Due to the pulsed nature of the testing $T_A = T_J$ for the electrical characteristics table.

Note 8: The parameters in the electrical characteristics table are tested under open loop conditions at $PV_{IN} = V_{DD}$ = 3.6V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

Note 9: Shutdown current includes leakage current of PFET.

Note 10: I_Q specified here is when the part is not switching. For operating quiescent current at no load, refer to datasheet curves.

Note 11: Current limit is built-in, fixed, and not adjustable. Electrical Characteristic table reflects open loop data (FB = 0V and current drawn from SW pin ramped up until cycle by cycle limit is activated). Refer to System Characteristics table for maximum output current.

Note 12: Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board and using the suggested inductor and capacitors.

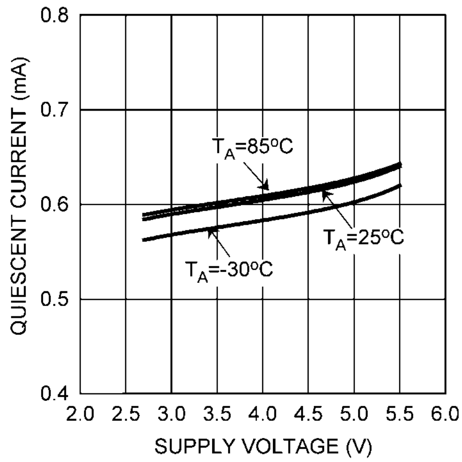
Note 13: National Semiconductor recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling procedures can result in damage.

Note 14: Linearity limits are ±3% or ±50 mV whichever is larger.

Typical Performance Characteristics

(Circuit in *Figure 3*, $PV_{IN} = V_{DD}$ = EN = 3.6V and T_A = 25°C unless otherwise specified.).

Quiescent Current vs Supply Voltage (V_{CON} = 0V, FB = 0V, No Switching)



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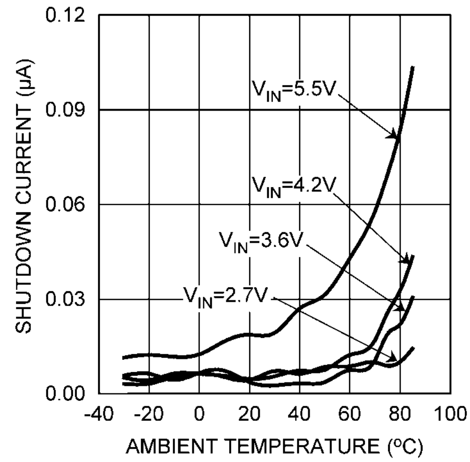
Shutdown Current vs Temperature (V_{CON} = 0V, EN = 0V)



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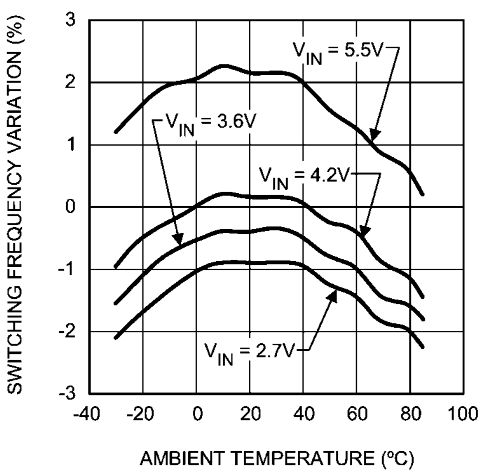
Switching Frequency vs Temperature (V_{OUT} = 1.3V, I_{OUT} = 200 mA)



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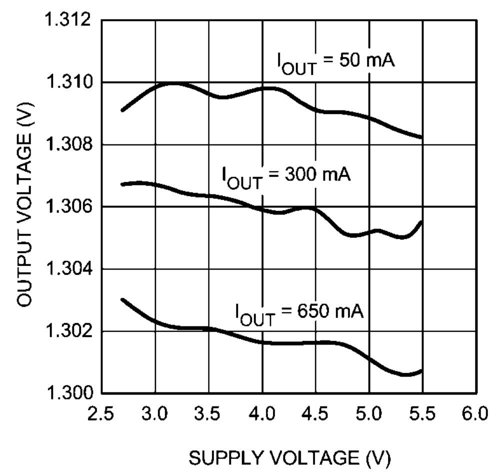
Output Voltage vs Supply Voltage (V_{OUT} = 1.3V)



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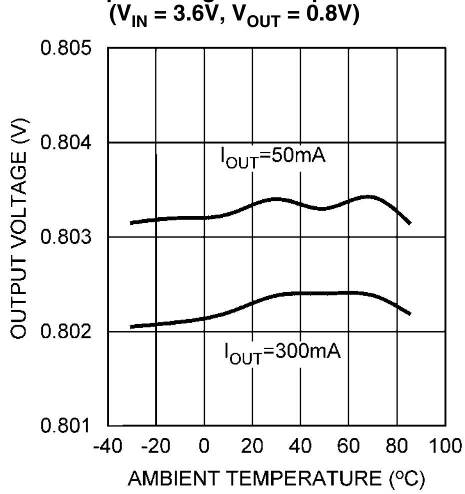
Output Voltage vs Temperature (V_{IN} = 3.6V, V_{OUT} = 0.8V)



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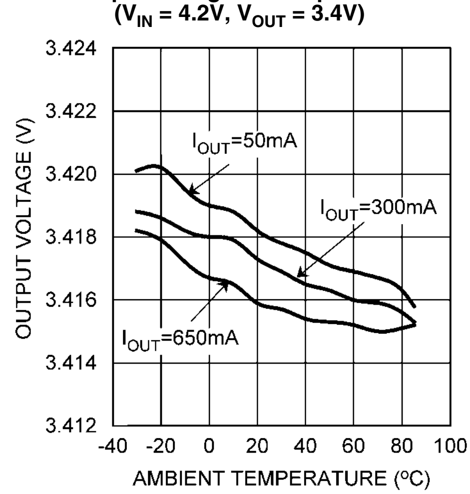
Output Voltage vs Temperature (V_{IN} = 4.2V, V_{OUT} = 3.4V)



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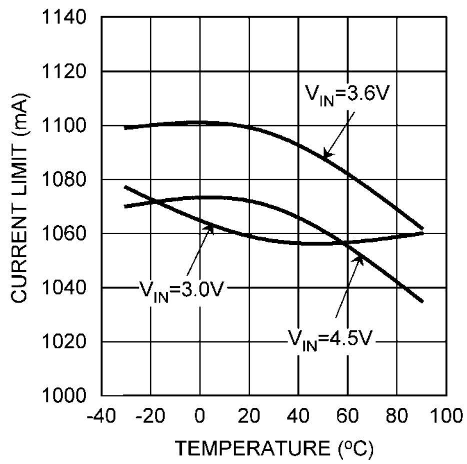
Current Limit vs Temperature (Large PFET)



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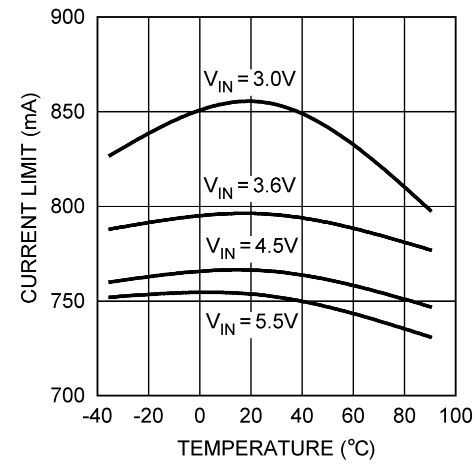
Current Limit vs Temperature (Small PFET)



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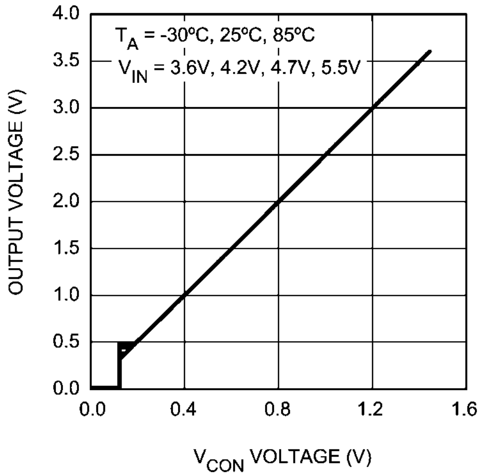
V_{CON} Voltage vs Output Voltage (R_{LOAD} = 10Ω)



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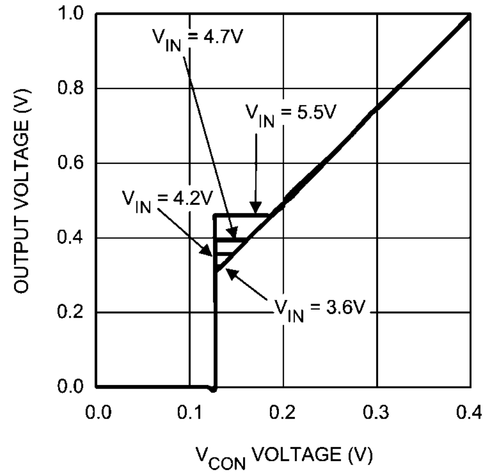
V_{CON} Voltage vs Output Voltage (R_{LOAD} = 10Ω)



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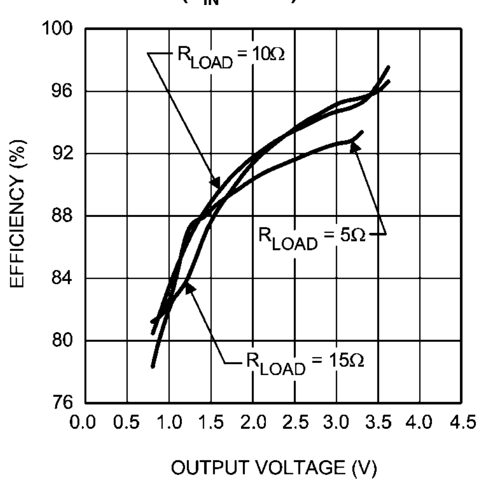
Efficiency vs Output Voltage (V_{IN} = 3.9V)



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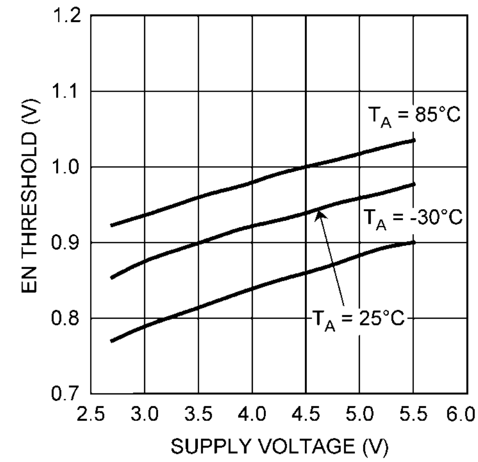
EN High Threshold vs Supply Voltage



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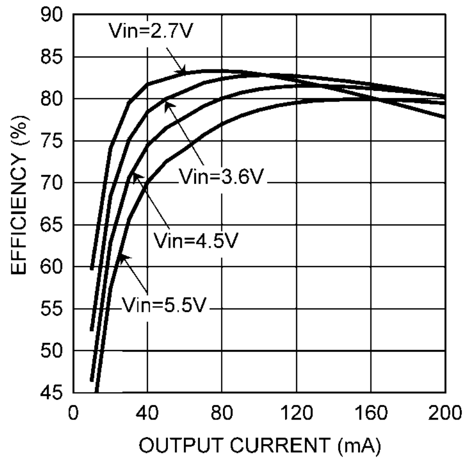
Efficiency vs Output Current (V_{OUT} = 0.8V)



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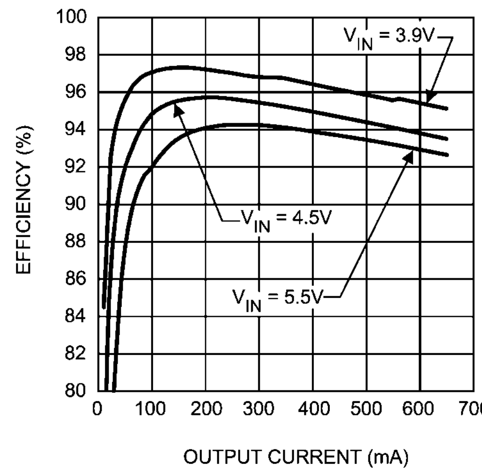
Efficiency vs Output Current (V_{OUT} = 3.6V)



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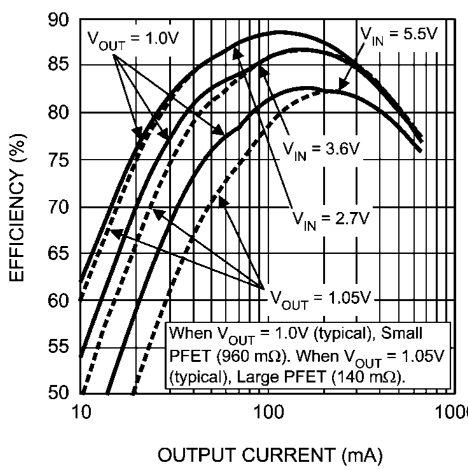
Efficiency vs Output Current (R_{DSON} Management)



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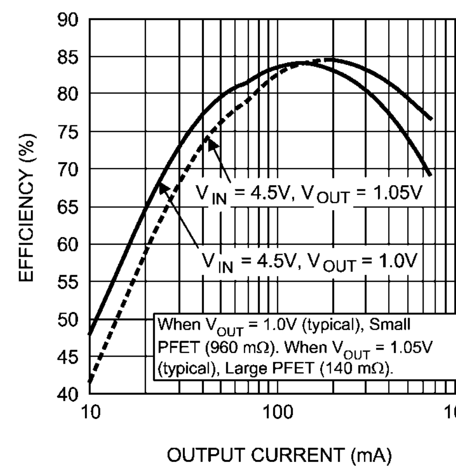
Dark curves are efficiency profiles of either large PFET or small PFET whichever is higher.

Efficiency vs Output Current (R_{DSON} Management, V_{IN}=4.5V)



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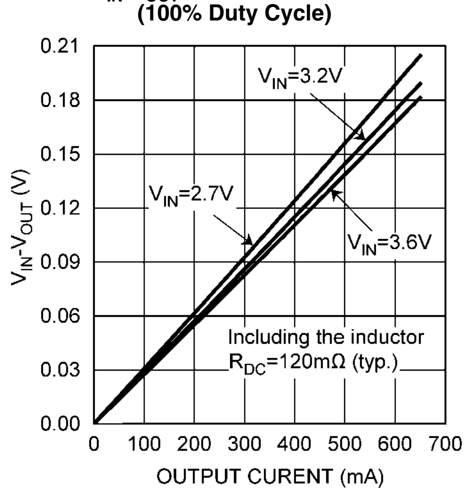
V_{IN}-V_{OUT} vs Output Current (100% Duty Cycle)



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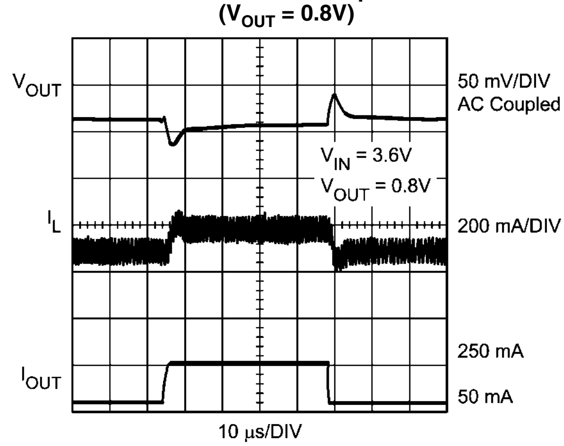
Load Transient Response (V_{OUT} = 0.8V)



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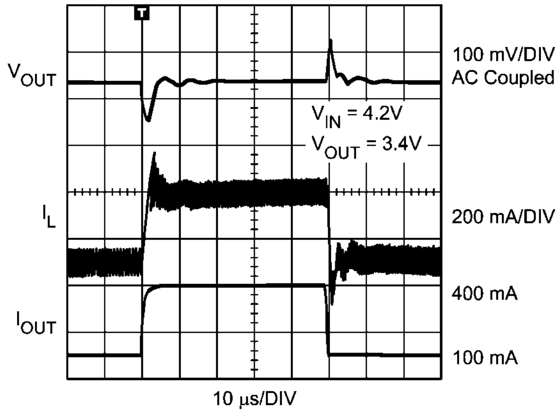
Load Transient Response
(V_{IN} = 4.2V, V_{OUT} = 3.4V)



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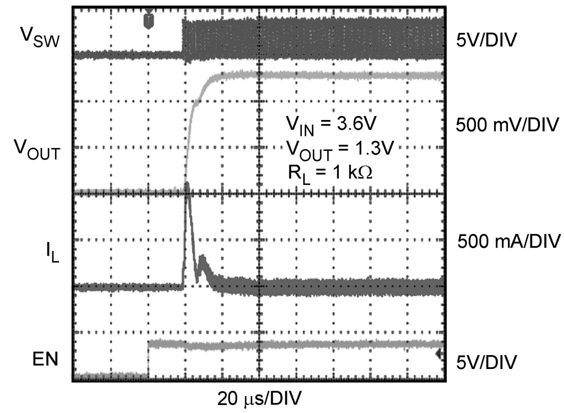
Startup
(V_{IN} = 3.6V, V_{OUT} = 1.3V, R_{LOAD} = 1 kΩ)



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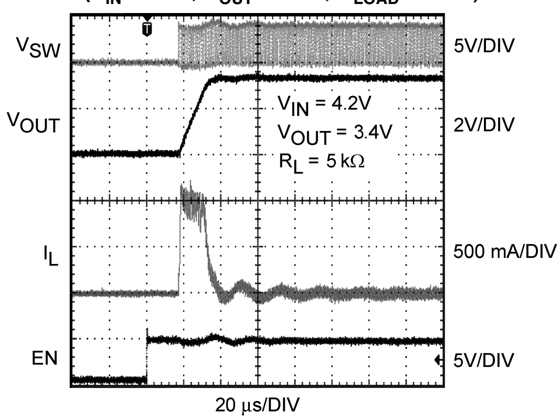
Startup
(V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 5 kΩ)



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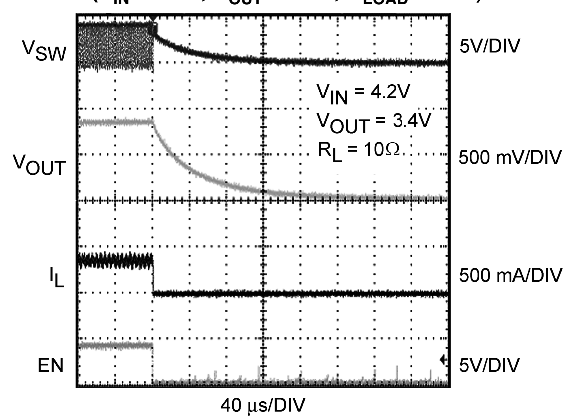
Shutdown Response
(V_{IN} = 4.2V, V_{OUT} = 3.4V, R_{LOAD} = 10Ω)



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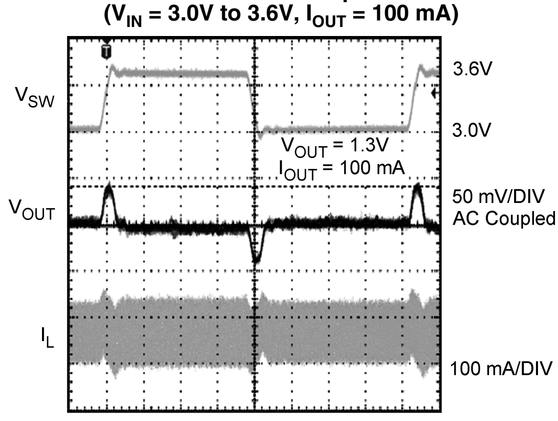
Line Transient Reponse
(V_{IN} = 3.0V to 3.6V, I_{OUT} = 100 mA)



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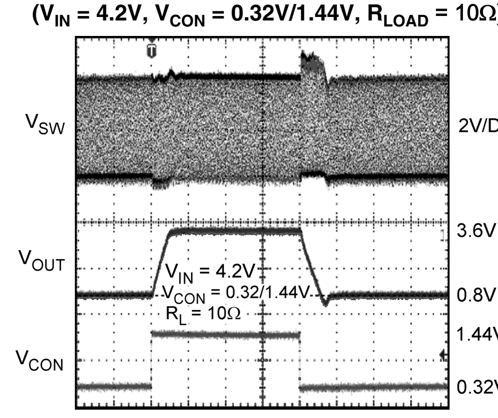
V_{CON} Transient Response
(V_{IN} = 4.2V, V_{CON} = 0.32V/1.44V, R_{LOAD} = 10Ω)



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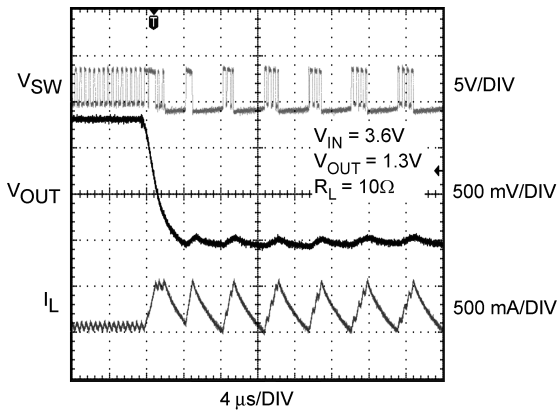
Timed Current Limit Response (V_{IN} = 3.6V)



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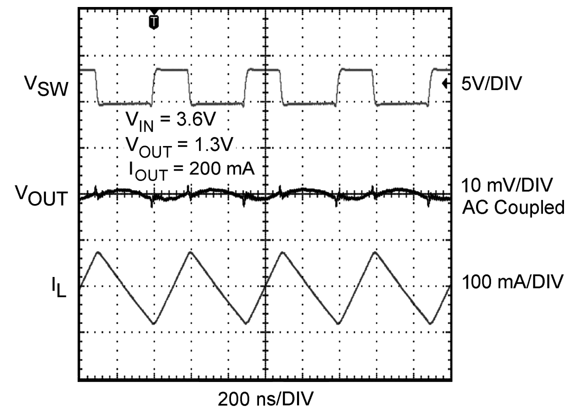
Output Voltage Ripple (V_{OUT} = 1.3V)



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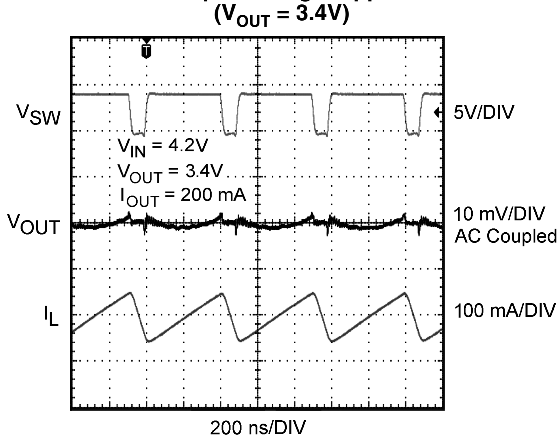
Output Voltage Ripple (V_{OUT} = 3.4V)



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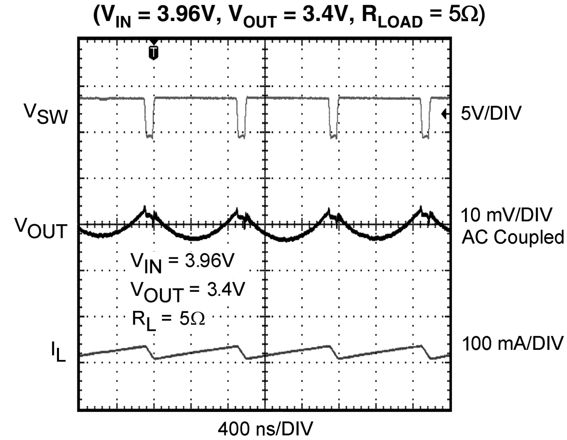
Output Voltage Ripple in Pulse Skip (V_{IN} = 3.96V, V_{OUT} = 3.4V, R_{LOAD} = 5Ω)



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Block Diagram

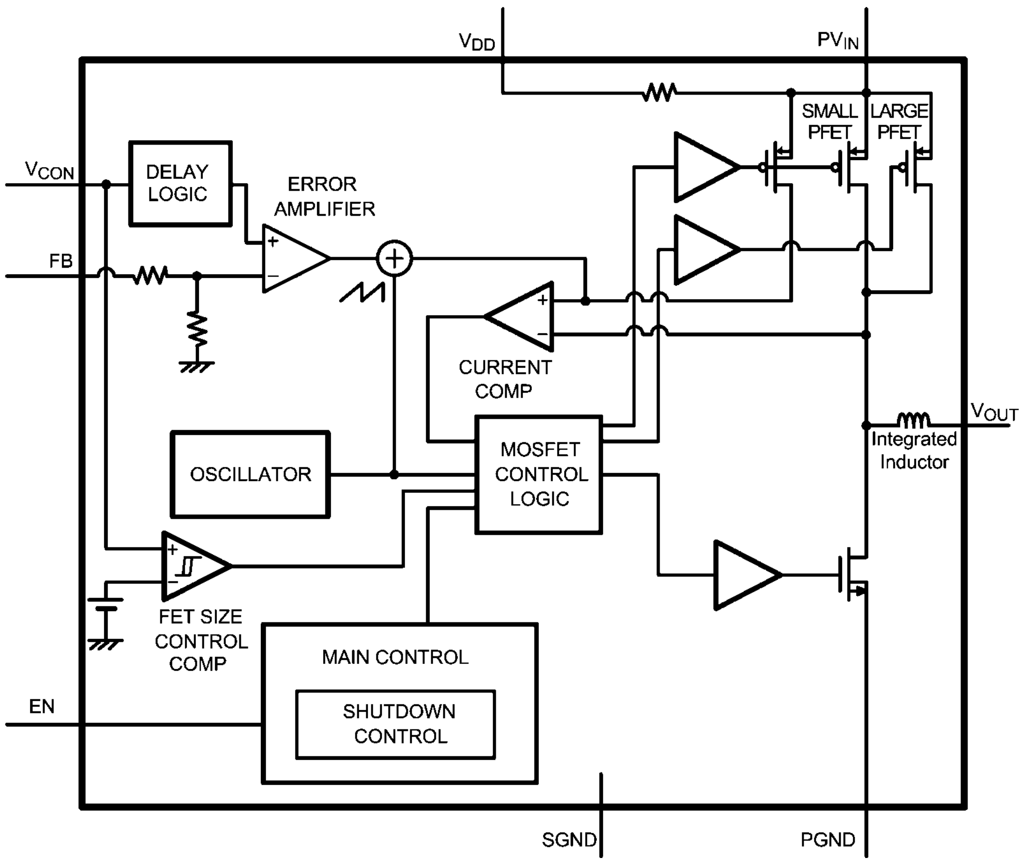

FIGURE 2. Functional Block Diagram

Operation Description

The LM3218 is a simple, step-down DC-DC converter with a 2.6 µH series inductor substrate optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on current mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 650 mA when V_{OUT} > 1.05V (typ.) and 400 mA when V_{OUT} < 1.00V (typ.) in PWM mode.

Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

Efficiency is typically around 95% for a 400 mA load with 3.4V output, 3.9V input. The LM3218 has an R_{DSON} management scheme to increase efficiency when $V_{OUT} \leq$ 1V. The output voltage is dynamically programmable from 0.8V to 3.6V by adjusting the voltage on the control pin without the need for external feedback resistors. This prolongs battery life by changing the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The LM3218 is constructed using a chip-scale 8-pin micro SMD package and a LTCC inductor substrate. This package offers the smallest possible integrated solution footprint for space-critical applications such as cell phones, where board area is an important design consideration. Use of a high switching frequency (2 MHz) reduces the size of external components. As shown in *Figure 1*, only two external capacitors are required for implementation. Use of this module requires special design considerations for implementation. (See *LTCC Module Package Assembly and Use* in the *Applications Information* section). The board mounting requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions. (See *Shutdown Mode* in the *Device Information* section.)

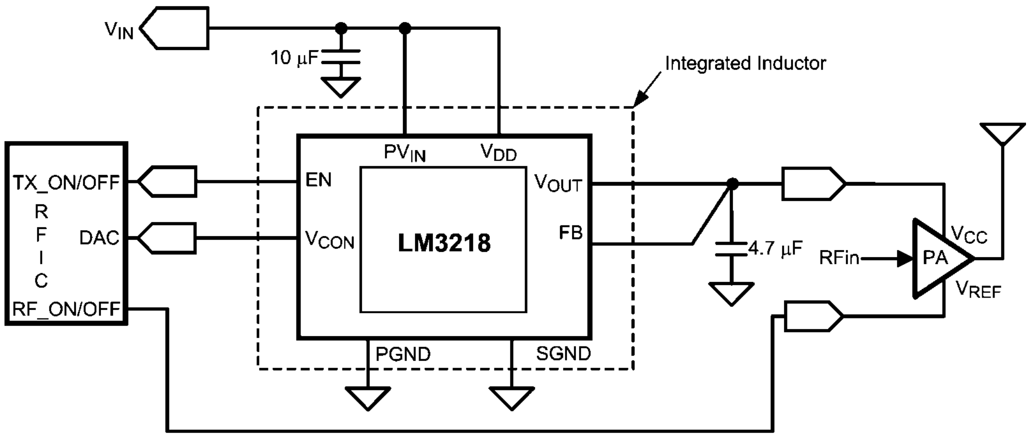

FIGURE 3. Typical Operating System Circuit

Circuit Operation

Referring to *Figure 1* and *Figure 2*, the LM3218 operates as follows: During the first part of each switching cycle, the control block in the LM3218 turns on the internal PFET (P-channel MOSFET) switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (V_{IN} - V_{OUT}) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET (N-channel MOSFET) synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around V_{OUT} / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the power MOSFET switch and synchronous rectifier to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the terminal of the power MOSFET inverter.

While in operation, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse width to control the peak inductor current. This is done by comparing the signal from the current-sense amplifier with a slope compensated error signal from the voltage-feedback error amplifier. At the beginning of each cycle, the clock turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator turns off the PFET switch and turns on the NFET synchronous rectifier, ending the first part of the cycle. If an increase in load pulls the output down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET. This increases the average current sent to the output and adjusts for the increase in the load. Before appearing at the PWM comparator, a slope compensation ramp from the oscillator is subtracted from the error signal for stability of the current feedback loop. The minimum on time of PFET is 55 ns (typ.)

Shutdown Mode

Setting the EN digital pin low (<0.5V) places the LM3218 in shutdown mode (0.01 µA typ.). During shutdown, the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuitry of the LM3218 are turned off. Setting EN high (>1.2V) enables normal operation.

EN should be set low to turn off the LM3218 during power-up and under-voltage conditions when the power supply is less than the 2.7V minimum operating voltage. The LM3218 is designed for compact portable applications, such as mobile phones. In such applications, the system controller determines power supply sequencing and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

Internal Synchronous Rectification

While in PWM mode, the LM3218 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

The internal NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

$R_{DSON(P)}$ Management

The LM3218 has a unique $R_{DSON(P)}$ management function to improve efficiency in the low output current region up to 100 mA. When the V_{CON} voltage is less than 0.40V (typ.), the device uses only a small part of the PFET to minimize drive loss of the PFET. When V_{CON} is greater than 0.42V (typ.), the entire PFET is used to minimize $R_{DSON(P)}$ loss. This threshold has about 20 mV (typ.) of hysteresis.

$V_{CON,ON}$

The output is disabled when V_{CON} is below 125 mV (typ.). It is enabled when V_{CON} is above 150 mV (typ.). The threshold has about 25 mV (typ.) of hysteresis.

Current Limiting

A current limit feature allows the LM3218 to protect itself and external components during overload conditions. In PWM mode, an 1100 mA (typ.) cycle-by-cycle current limit is normally used when V_{CON} is above 0.42V (typ.), and an 800 mA (typ.) is used when V_{CON} is below 0.40V (typ.). If an excessive load pulls the output voltage down to approximately 0.375V, then the device switches to a timed current limit mode when V_{CON} is above 0.42V (typ.). In timed current limit mode the internal PFET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 3.5us to force the instantaneous inductor current to ramp down to a safe value. The synchronous rectifier is off in timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Dynamically Adjustable Output Voltage

The LM3218 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.8V to 3.6V by changing the voltage on the analog V_{CON} pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. See *Setting the Output Voltage* in the *Application Information section* for further details. The LM3218 moves into Pulse Skipping mode when duty cycle is over 92% and the output voltage ripple increases slightly.

Thermal Overload Protection

The LM3218 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. Both the PFET and the NFET are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Application Information

SETTING THE OUTPUT VOLTAGE

The LM3218 features a pin-controlled variable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.8V to 3.6V by setting the voltage on the V_{CON} pin, as in the following formula:

$$V_{OUT} = 2.5 \times V_{CON}$$

When V_{CON} is between 0.32V and 1.44V, the output voltage will follow proportionally by 2.5 times of V_{CON}.

If V_{CON} is over 1.44V (V_{OUT} = 3.6V), sub-harmonic oscillation may occur because of insufficient slope compensation. If V_{CON} voltage is less than 0.32V (V_{OUT} = 0.8V), the output voltage may not be regulated due to the required on-time being less than the minimum on-time (55 ns). The output voltage can go lower than 0.8V providing a limited V_{IN} range is used. Refer to datasheet curve *(V_{CON} Voltage vs Output Voltage)* for details. This curve is for a typical part and there could be part-to-part variation for output voltages less than 0.8V over the limited V_{IN} range. When the control pin voltage is more than 0.15V (typ.), the switches are turned on. When it is less than 0.125V (typ.), the switches are turned off. This on/off function has 25 mV (typ.) hysteresis. The quiescent current when (V_{CON} = 0V and V_{EN} = Hi) is around 600 µA.

ESTIMATION OF MAXIMUM OUTPUT CURRENT CAPABILITY

Referring to *Figure 3*, the Inductor peak-to-peak ripple current can be estimated by:

$$I_{IND\_PP} = (V_{IN} - V_{OUT}) \times V_{OUT} / (L1 \times F_{SW} \times V_{IN})$$

Where, Fsw is switching frequency.

Therefore, maximum output current can be calculated by:

$$I_{OUT\_MAX} = I_{LIM} - 0.5 \times I_{IND\_PP}$$

For the worst case calculation, the following parameters should be used:

F_{SW} (Lowest switching frequency): 1.8 MHz

I_{LIM} (Lowest current limit value): 985 mA

L1 (Lowest inductor value): refer to inductor datasheet. Note that inductance will drop with DC bias current and temperature. The worst case is typically at 85°C.

For example, V_{IN} = 4.2V, V_{OUT} = 3.2V, L1 = 2.0 µH (Inductance value at 985 mA DC-bias current and 85°C), F_{SW} = 1.8 MHz , I_{LIM} = 985 mA.

$$I_{IND\_PP} = 212 \text{ mA}$$

$$I_{OUT\_MAX} = 985 - 106 = 876 \text{ mA}$$

The effects of switch, inductor resistance and dead time are ignored. In real application, the ripple current would be 10% to 15% higher than ideal case. This should be taken into account when calculating maximum output current. Special attention needs to be paid that a delta between maximum output current capability and the current limit is necessary to satisfy transient response requirements. In practice, transient response requirements may not be met for output current greater than 650 mA.

INDUCTOR SELECTION

The inductor is an integrated LTCC 2.6 µH substrate within the LM3218 module and has a saturation current rating over 1200 mA. The integrated inductor's low 1.2 mm maximum height provides ease of use into small design constraints. Integrating the inductor can eliminate layout issues associated with DC/DC converters and reduce potential EMI problems.

CAPACITOR SELECTION

The LM3218 is designed for use with ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for input and a 4.7 µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitor types such as X5R, X7R and B are recommended for both filters. *Table 1* lists some suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. If it is necessary to choose a 0603-size capacitor for C_{IN} and C_{OUT}, the operation of the LM3218 should be carefully evaluated on the system board. Use of multiple 2.2 µF or 1 µF capacitors in parallel may also be considered.

TABLE 1. Suggested Capacitors And Their Suppliers

Model	Vendor
C1608X5R0J106K, 10 µF, 6.3V	TDK
C1608X5R0J475M, 4.7 µF, 6.3V	TDK
0805ZD475KA 4.7 µF, 10V	AVX

The input filter capacitor supplies AC current drawn by the PFET switch of the LM3218 in the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

EN PIN CONTROL

Drive the EN pin using the system controller to turn the LM3218 ON and OFF. Use a comparator, Schmidt trigger or logic gate to drive the EN pin. Set EN high (>1.2V) for normal operation and low (<0.5V) for a 0.01 µA (typ.) shutdown mode and requirements for small package size outweigh the additional size required for inclusion of UVLO (Under Voltage Lock-Out) circuitry.

LTCC PACKAGE ASSEMBLY AND USE

The LTCC Integrated Inductor withLM3218 micro SMD package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the micro SMD package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metalization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, micro SMD devices are sensitive to light, in the red and infrared range, shining on the package's exposed die edges.

BOARD LAYOUT CONSIDERATIONS

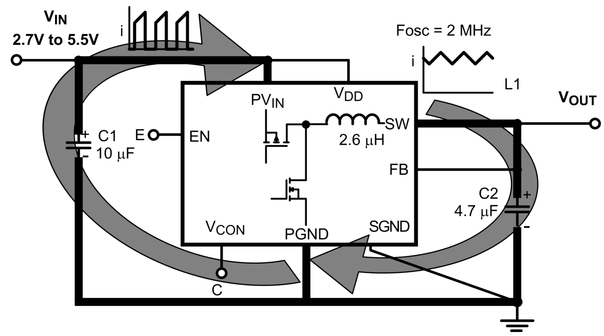

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FIGURE 4. Current Loop

The LM3218 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from PV_{IN} line into the output capacitor and the load through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line into the output capacitor and the load.

Referring to *Figure 4*, a pulse current flows in the left-hand side loop, and a ripple current flows in the right-hand side loop. Board layout and circuit pattern design of these two loops are the key factors for reducing noise radiation and stable operation. In other lines, such as from battery to C1 and C2 to the load, the current is mostly DC current. Therefore, it is not necessary to take so much care. Only pattern width (current capability) and DCR drop considerations are needed.

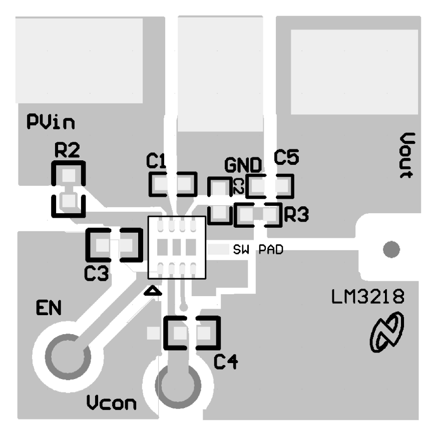

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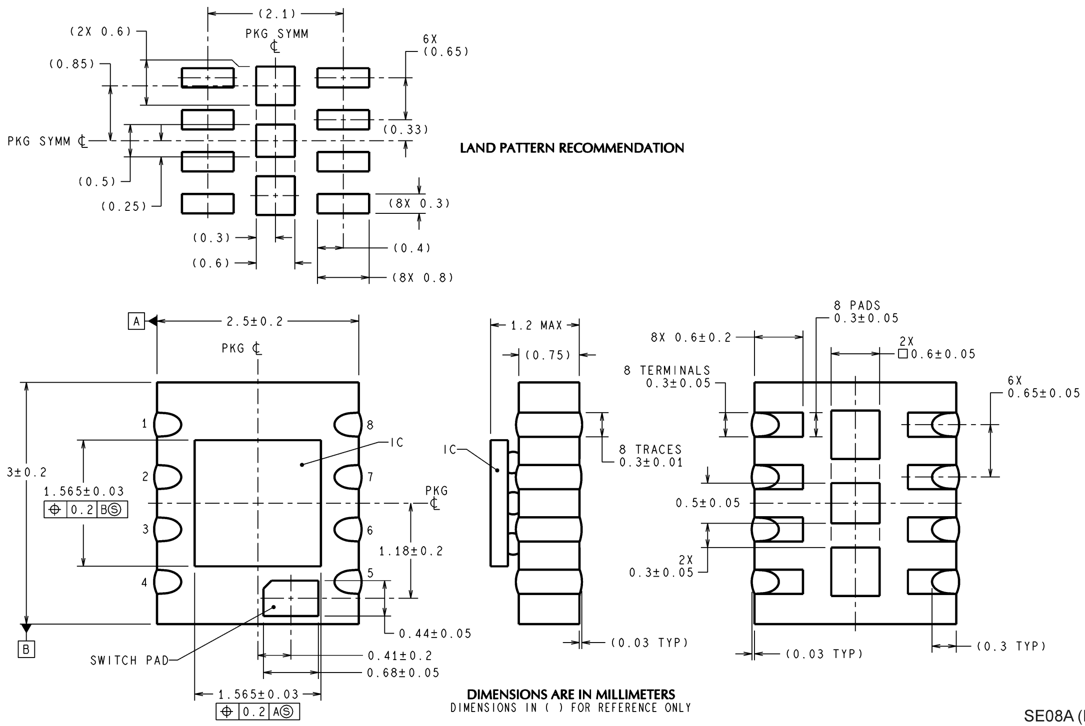
FIGURE 5. Evaluation Board Layout

Physical Dimensions inches (millimeters) unless otherwise noted



SE08A (Rev B)

NS Package Number SE08A

Notes

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