National Semiconductor

PRELIMINARY
March 31, 2008

LMH0036
SD SDI Reclocker with 4:1 Input Multiplexer

General Description

The LMH0036 SD SDI Reclocker with 4:1 Input Multiplexer retimes serial digital video data conforming to the SMPTE 259M (C) standard. The LMH0036 operates at the serial data rate of 270 Mbps, and also supports DVB-ASI operation at 270 Mbps. The LMH0036 includes an integrated 4:1 input multiplexer for selecting one of four input data streams for re-timing.

The LMH0036 retimes the incoming data to suppress accumulated jitter. The LMH0036 recovers the serial data-rate clock and optionally provides it as an output. The LMH0036 has two differential serial data outputs; the second output may be selected as a low-jitter, data-rate clock output. Controls and indicators are: serial clock or second serial data output select, manual rate select input, SD indicator output, lock detect output, auto/manual data bypass, and output mute. The serial data inputs, outputs, and serial data-rate clock outputs are differential LVPECL compatible. The CML serial data and serial data-rate clock outputs are suitable for driving 100Ω differentially terminated networks. The control logic inputs and outputs are LVCMOS compatible.

The LMH0036 is powered from a single 3.3V supply. Power dissipation is typically 360 mW. The device is housed in a 48-pin LLP package.

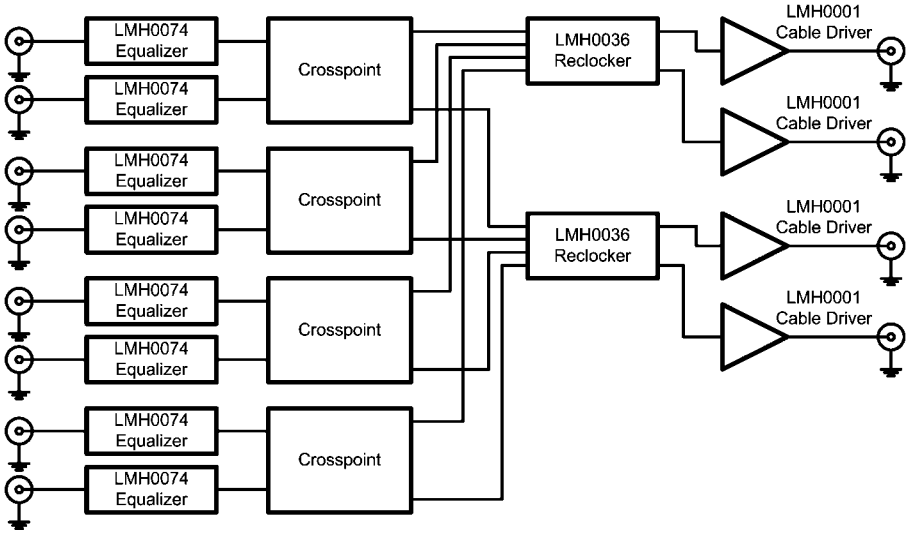
Features

- Supports SMPTE 259M (C) serial digital video standard
- Supports 270 Mbps serial data rate operation
- Supports DVB-ASI at 270 Mbps
- Single 3.3V supply operation
- 360 mW typical power consumption
- Integrated 4:1 multiplexed input
- Two differential, reclocked outputs
- Choice of second reclocked output or low-jitter, differential, data-rate clock output
- Single 27 MHz external crystal or reference clock input
- SD indicator output
- Lock Detect indicator output
- Output mute function for data and clock
- Auto/Manual reclocker bypass
- Differential LVPECL compatible serial data inputs and outputs
- LVCMOS control inputs and indicator outputs
- 48-Pin LLP package
- Industrial temperature range: -40°C to +85°C

Applications

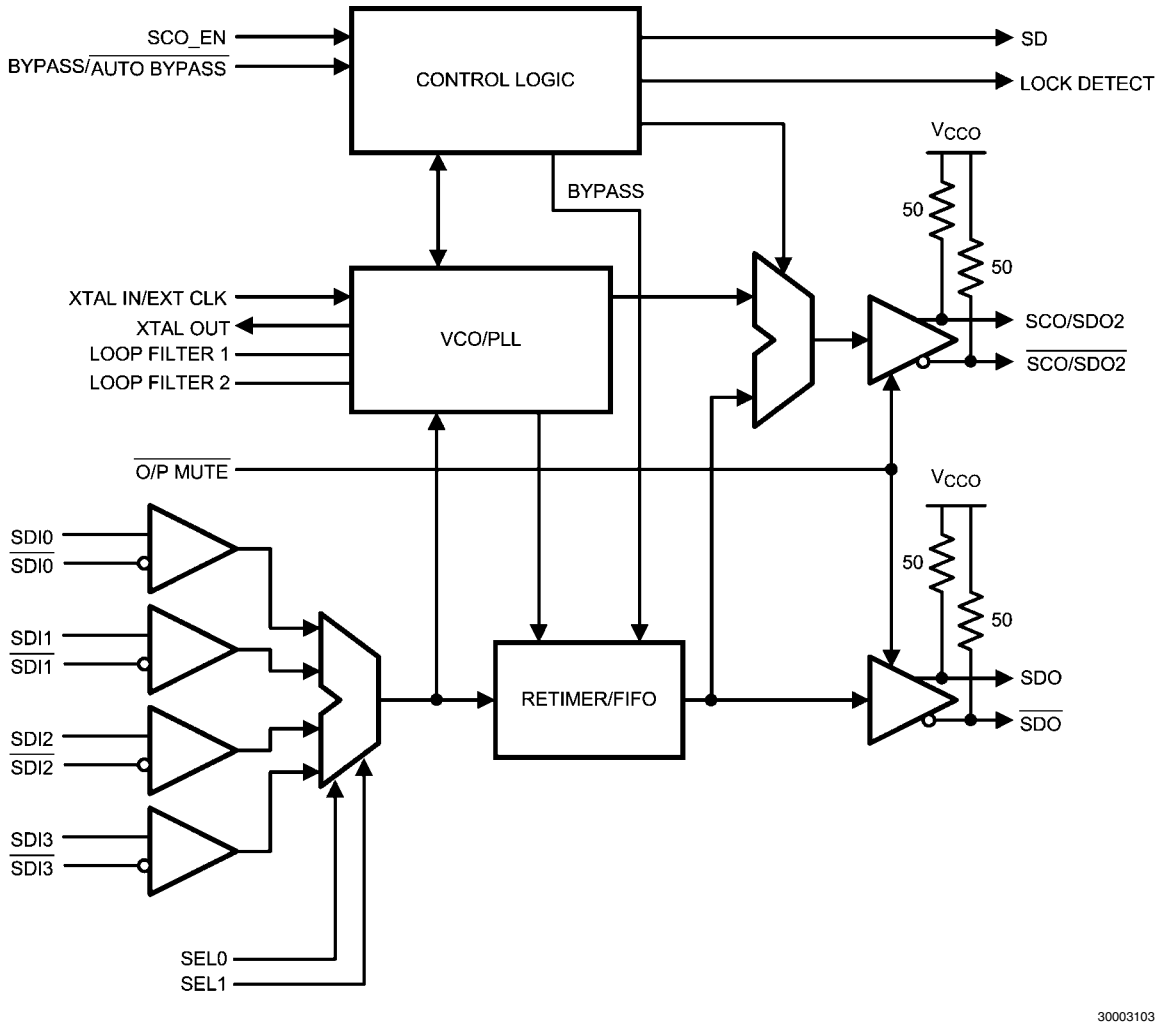
- SDTV serial digital video interfaces for:
  - Digital video routers and switchers
  - Digital video processing and editing equipment
  - DVB-ASI equipment
  - Video standards and format converters

Typical Application

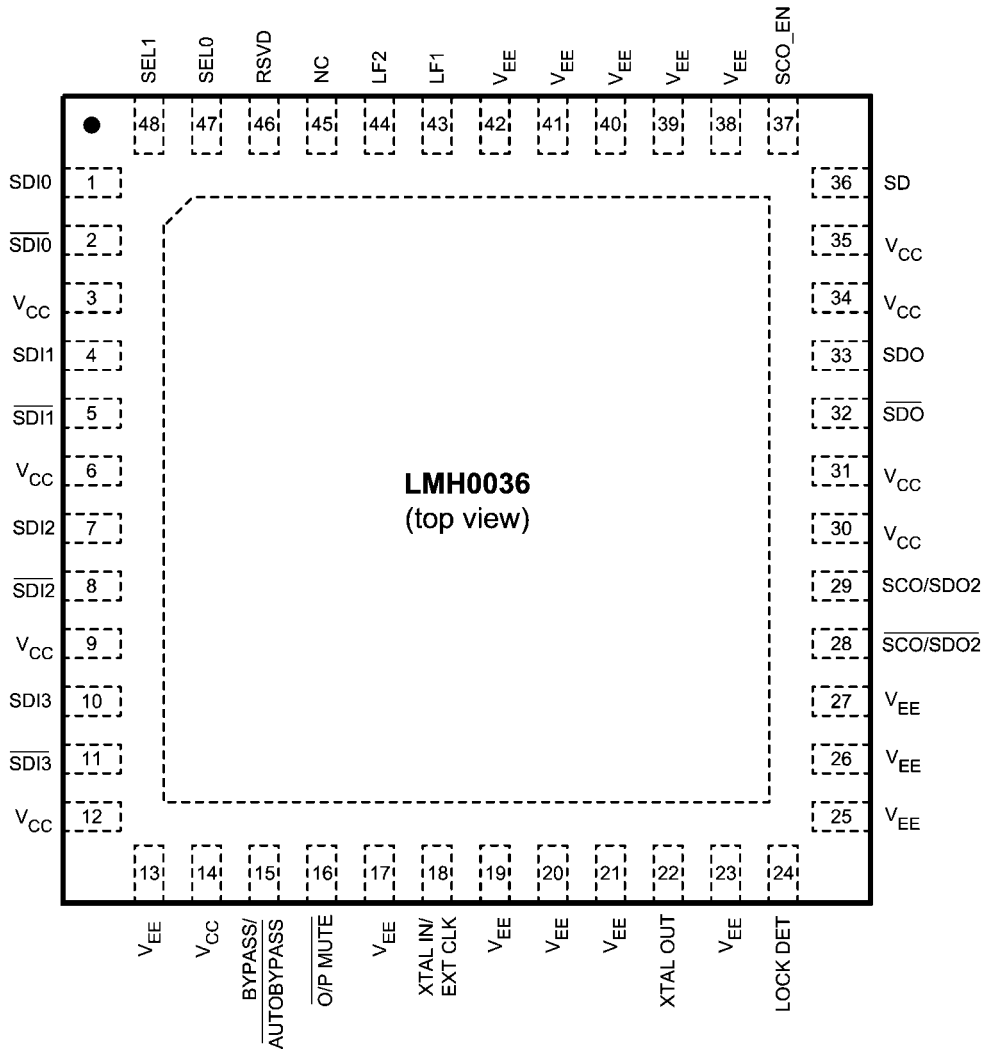


30003101

Block Diagram



Connection Diagram



30003102

The exposed die attach pad is the primary negative electrical terminal for this device. It must be connected to the negative power supply voltage.

48-Pin LLP
Order Number LMH0036SQ
See NS Package Number SQA48A

Pin Descriptions

Pin	Name	Description
1	SDI0	Data Input 0 True
2	$\overline{\text{SDI0}}$	Data Input 0 Complement
3	V_{CC}	Positive power supply input
4	SDI1	Data Input 1 True
5	$\overline{\text{SDI1}}$	Data Input 1 Complement
6	V_{CC}	Positive power supply input
7	SDI2	Data Input 2 True
8	$\overline{\text{SDI2}}$	Data Input 2 Complement
9	V_{CC}	Positive power supply input
10	SDI3	Data Input 3 True
11	$\overline{\text{SDI3}}$	Data Input 3 Complement
12	V_{CC}	Positive power supply input
13	V_{EE}	Negative power supply input
14	V_{CC}	Positive power supply input
15	BYPASS/$\overline{\text{AUTO BYPASS}}$	Bypass/Auto Bypass mode select
16	OUTPUT $\overline{\text{MUTE}}$	Data and Clock Output Mute input (active low)
17	V_{EE}	Negative power supply input
18	XTAL IN/EXT CLK	Crystal or External Oscillator input
19	V_{EE}	Negative power supply input
20	V_{EE}	Negative power supply input
21	V_{EE}	Negative power supply input
22	XTAL OUT	Crystal Oscillator output
23	V_{EE}	Negative power supply input
24	LOCK DETECT	PLL Lock Detect output (active high)
25	V_{EE}	Negative power supply input
26	V_{EE}	Negative power supply input
27	V_{EE}	Negative power supply input
28	$\overline{\text{SCO/SDO2}}$	Serial Clock or Serial Data Output 2 complement
29	SCO/SDO2	Serial Clock or Serial Data Output 2 true
30	V_{CC}	Positive power supply input
31	V_{CC}	Positive power supply input
32	$\overline{\text{SDO}}$	Data Output complement
33	SDO	Data Output true
34	V_{CC}	Positive power supply input
35	V_{CC}	Positive power supply input
36	SD	SD indicator output
37	SCO_EN	Serial Clock or Serial Data 2 Output select (active high enables serial clock output)
38	V_{EE}	Negative power supply input
39	V_{EE}	Negative power supply input
40	V_{EE}	Negative power supply input
41	V_{EE}	Negative power supply input
42	V_{EE}	Negative power supply input
43	LF1	Loop Filter
44	LF2	Loop Filter
45	NC	No Connect - Not bonded internally
46	RSVD	Reserved - Do not connect or connect to ground
47	SEL0	Data Input select input

Pin	Name	Description
48	SEL1	Data Input select input
DAP	V_{EE}	Connect exposed DAP to negative power supply (ground)

Absolute Maximum Ratings (Note 1)

It is anticipated that this device will not be offered in a military qualified version. If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}–V_{EE})	4.0V
Logic Supply Voltage (Vi)	V_{EE}–0.15V to V_{CC} +0.15V
Logic Input Current (single input):	
Vi = V_{EE}–0.15V	–5 mA
Vi = V_{CC}+0.15V	+5 mA
Logic Output Voltage (Vo)	V_{EE}–0.15V to V_{CC} +0.15V
Logic Output Source/Sink Current	±8 mA
Serial Data Input Voltage (V_{SDI})	V_{CC} to V_{CC}–2.0V
Serial Data Output Sink Current (I_{SDO})	24 mA
Package Thermal Resistance	
θ_{JA} 48-pin LLP	26.1°C/W
θ_{JC} 48-pin LLP	1.9°C/W
Storage Temp. Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C (Pb-free)
ESD Rating (HBM)	8 kV
ESD Rating (MM)	400V
ESD Rating (CDM)	1250V

Recommended Operating Conditions

Supply Voltage (V_{CC}–V_{EE})	3.3V ±5%
Logic Input Voltage	V_{EE} to V_{CC}
Differential Serial Input Voltage	800 mV ±10%
Serial Data or Clock Output Sink Current (I_{SO})	16 mA max.
Operating Free Air Temperature (T_A)	–40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic level inputs	2		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
I_{IH}	Input Current High Level	V_{IH} = V_{CC}			1	20	µA
I_{IL}	Input Current Low Level	V_{IL} = V_{EE}			–1	–20	µA
V_{OH}	Output Voltage High Level	I_{OH} = –2 mA	All logic level outputs	2			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				V_{EE} + 0.6	V
V_{SDID}	Serial Input Voltage, Differential		SDI	200		1600	mV_{P-P}
V_{CMI}	Input Common Mode Voltage	V_{SDID} = 200 mV	SDI	V_{EE}+1.2		V_{CC}–0.2	V
V_{SDOD}	Serial Output Voltage, Differential	100Ω differential load	SDO, SCO	720	800	880	mV_{P-P}
V_{CMO}	Output Common Mode Voltage	100Ω differential load	SDO, SCO		V_{CC}– V_{SDOD}		V
I_{CC}	Power Supply Current, 3.3V supply, Total	270 Mbps, NTSC color bar pattern			109		mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SD}	Serial Data Rate	SMPTE 259M (C)	SDI, SDO		270		Mbps
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (Notes 7, 8, 9)	SDI	>6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (Notes 7, 8, 10)	SDI	>0.6			UI_{P-P}
t_{JIT}	Serial Data Output Jitter	270 Mbps, (Notes 8, 11)	SDO		0.02	0.08	UI_{P-P}
BW_{LOOP}	Loop Bandwidth	270 Mbps, <0.1dB Peaking			300		kHz
F_{CO}	Serial Clock Output Frequency	270 Mbps data rate	SCO		270		MHz
t_{JIT}	Serial Clock Output Jitter				2	3	ps_{RMS}
	Serial Clock Output Alignment with respect to Data Interval		SDO, SCO	40		60	%
	Serial Clock Output Duty Cycle		SCO	45		55	%
T_{ACQ}	Acquisition Time	(Notes 4, 6)				15	ms
t_r, t_f	Input rise/fall time	10%–90%	Logic inputs		1.5	3	ns
t_r, t_f	Input rise/fall time	20%–80%	SDI			1500	ps
t_r, t_f	Output rise/fall time	10%–90%	Logic outputs		1.5	3	ns
t_r, t_f	Output rise/fall time	20%–80%,(Note 5)	SCO, SDO		90	130	ps
F_{REF}	Reference Clock Frequency				27		MHz
F_{TOL}	Ref. Clock Freq. Tolerance				±50		ppm

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are referenced to V_{EE} (equal to zero volts).

Note 3: Typical values are stated for: V_{CC} = +3.3V, T_A = +25°C.

Note 4: Specification is guaranteed by design.

Note 5: R_L = 100Ω differential.

Note 6: Measured from first SDI transition until Lock Detect (LD) output goes high (true).

Note 7: Peak-to-peak amplitude with sinusoidal modulation per SMPTE RP 184-1996 paragraph 4.1. The test data signal shall be color bars.

Note 8: This parameter is guaranteed by characterization over voltage and temperature limits.

Note 9: Refer to "A1" in Figure 1 of SMPTE RP 184-1996.

Note 10: Refer to "A2" in Figure 1 of SMPTE RP 184-1996.

Note 11: Serial Data Output Jitter is total output jitter with $0.2UI_{P-P}$ input jitter.

Device Description

The LMH0036 SD SDI Reclocker with 4:1 Input Multiplexer is used in many types of digital video signal processing equipment. The LMH0036 supports the SMPTE 259M (C) standard, with a corresponding serial data rate of 270 Mbps. DVB-ASI data at 270 Mbps may also be retimed. The LMH0036 retimes the serial data stream to suppress accumulated jitter. It provides two low-jitter, differential, serial data outputs. The second output may be selected to output either serial data or a low-jitter serial data-rate clock. Controls and indicators are: serial data-rate clock or second serial data output select, manual rate select input, SD indicator output, lock detect output, auto/manual data bypass and output mute.

Serial data inputs are CML and LVPECL compatible. Serial data and data-rate clock outputs are differential CML and produce LVPECL compatible levels. The output buffer design can drive AC or DC-coupled, terminated 100Ω differential loads. The differential output level is 800 mV_{P-P} ±10% into 100Ω AC or DC-coupled differential loads. Logic inputs and outputs are LVCMOS compatible.

The device package is a 48–pin LLP with an exposed die attach pad. The exposed die attach pad is electrically connected to device ground (V_{EE}) and is the primary negative electrical terminal for the device. This terminal must be connected to the negative power supply or circuit ground.

Serial Data Inputs, Serial Data and Clock Outputs

SERIAL DATA INPUT AND OUTPUTS

The differential serial data inputs, SDI0-SDI3, accept 270 Mbps serial digital video data. The serial data inputs are differential LVPECL compatible. These inputs are intended to be DC interfaced to devices such as the LMH0074 adaptive cable equalizer. These inputs are not internally terminated or biased. The inputs may be AC-coupled if a suitable input bias voltage is provided.

The LMH0036 provides four independent, multiplexed data inputs. The active input channel is selected via the SEL0 and SEL1 pins, as shown in *Table 1*. *Figure 1* shows the equivalent input circuit for SDI[3:0] and $\overline{\text{SDI[3:0]}}$.

The LMH0036 has two, retimed, differential, serial data outputs, SDO and SCO/SDO2. These outputs provide low jitter, differential, retimed data to devices such as the LMH0001 or LMH0002 cable driver. Output SCO/SDO2 is multiplexed and can provide either a second serial data output or a serial data-rate clock output. *Figure 2* shows the equivalent output circuit for SDO, $\overline{\text{SDO}}$, SCO/SDO2, and $\overline{\text{SCO/SDO2}}$.

The SCO_EN input controls the operating mode for the SCO/SDO2 output. When the SCO_EN input is high the SCO/SDO2 output provides a serial data-rate clock. When SCO_EN is low, the SCO/SDO2 output provides retimed serial data.

Both differential serial data outputs, SDO and SCO/SDO2, are muted when the $\overline{\text{MUTE}}$ input is a logic low level. SCO/SDO2 also mutes when the Bypass mode is activated when this output is operating as the serial clock output. When muted, SDO and $\overline{\text{SDO}}$ (or SDO2 and $\overline{\text{SDO2}}$) will assume opposite differential output levels. The CML serial data outputs are differential LVPECL compatible. These outputs have internal 50Ω pull-ups and are suitable for driving AC or DC-coupled, 100Ω center-tapped, AC grounded or 100Ω un-center-tapped, differentially terminated networks.

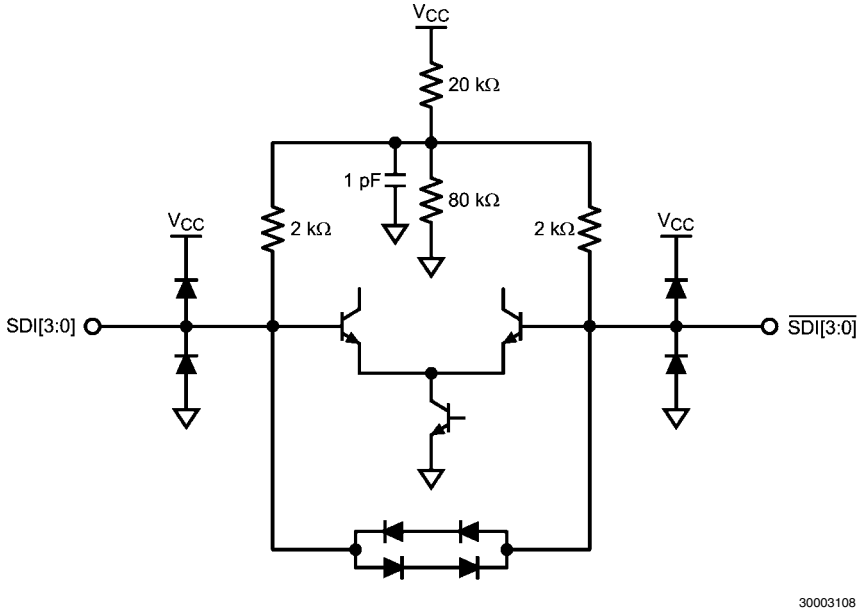


FIGURE 1. Equivalent SDI Input Circuit (SDI[3:0], $\overline{\text{SDI[3:0]}}$)

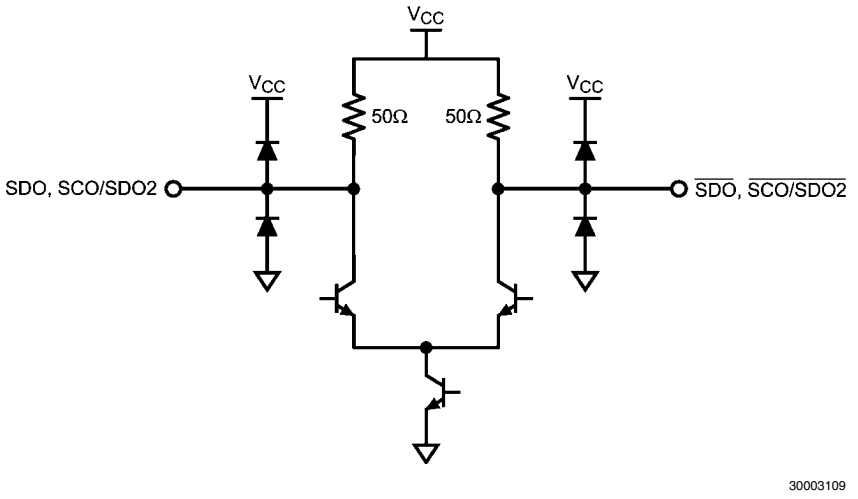


FIGURE 2. Equivalent SDO Output Circuit (SDO, $\overline{\text{SDO}}$, SCO/SDO2, $\overline{\text{SCO/SDO2}}$)

SERIAL DATA CLOCK/SERIAL DATA 2 OUTPUT

The Serial Data Clock/Serial Data 2 Output is controlled by the SCO_EN input and provides either a second retimed serial data output or a low jitter differential clock output appropriate to the serial data rate being processed. When operating as a serial clock output, the rising edge of the clock will be positioned within the corresponding serial data bit interval within 10% of the center of the data interval.

Differential output SCO/SDO2 functions as the second serial data output when the SCO_EN input is a logic-low level. This output functions as the serial data-rate clock output when the SCO_EN input is a logic-high level. The SCO_EN input has an internal pull-down device and the default state of SCO_EN is low (serial data output 2 enabled). SCO/SDO2 is muted when the $\overline{\text{MUTE}}$ input is a logic low level. When the Bypass mode is activated and this output is functioning as a serial clock output, the output will also be muted.

Control Inputs and Indicator Outputs

SERIAL DATA INPUT SELECTOR

The Serial Data Input Selector (SEL [1:0]) allows the user to select the active input channel. *Table 1* shows the input selected for a given state of SEL [1:0].

TABLE 1. Data Input Select Codes

SEL [1:0] Code	Selected Input
00	SDI0
01	SDI1
10	SDI2
11	SDI3

LOCK DETECT

The Lock Detect (LD) output, when high, indicates that data is being received and the PLL is locked. LD may be connected to the $\overline{\text{MUTE}}$ input to mute the data and clock outputs when no data signal is being received. See *Table 2*.

$\overline{\text{MUTE}}$

The $\overline{\text{MUTE}}$ input, when low, mutes the serial data and clock outputs. It may be connected to Lock Detect or externally driven to mute or un-mute the outputs. If $\overline{\text{MUTE}}$ is connected to LD, then the data and clock outputs are muted when the PLL is not locked. This function overrides the Bypass function: see *Table 2*. $\overline{\text{MUTE}}$ has an internal pull-up device to enable the output by default.

BYPASS/$\overline{\text{AUTO BYPASS}}$

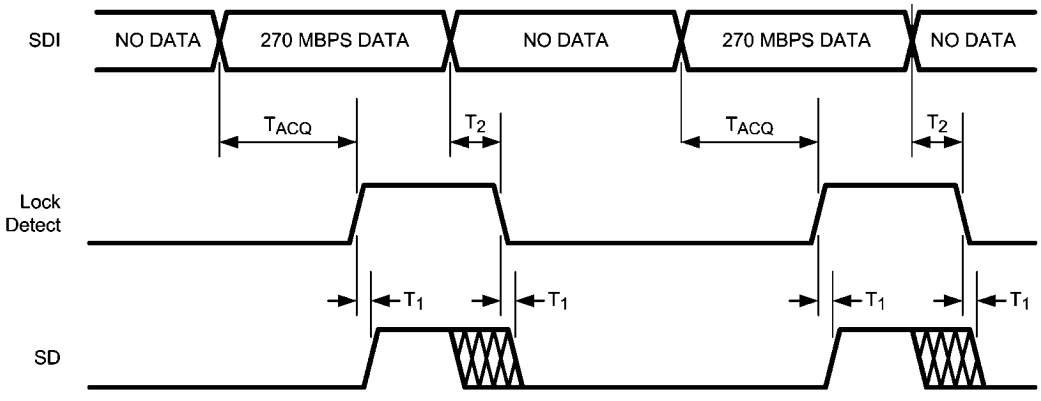
The Bypass/$\overline{\text{Auto Bypass}}$ input, when high, forces the device to output the data without reclocking it. When this input is low, the device automatically bypasses the reclocking function when the device is in an unlocked condition or the detected data rate is a rate which the device does not support. See *Table 2*. BYPASS/$\overline{\text{AUTO BYPASS}}$ has an internal pull-down device.

TABLE 2. Control Functionality

LOCK DETECT	OUTPUT $\overline{\text{MUTE}}$	BYPASS/$\overline{\text{AUTO BYPASS}}$	DEVICE STATUS
0	1	0	PLL unlocked, reclocker bypassed
1	1	0	PLL locked to supported data rate, reclocker not bypassed
X	0	X	Outputs muted
0	LOCK DETECT	X	Outputs muted
1	LOCK DETECT	0	PLL locked to supported data rate, reclocker not bypassed
1	LOCK DETECT	1	PLL locked to supported data rate, reclocker bypassed
X	1	1	Outputs not muted, reclocker bypassed

SD

The SD output indicates that the LMH0036 is locked and processing SD data rates. It may be used to control another device such as the LMH0002 cable driver. When this output is high it indicates that the data rate is 270 Mbps. The SD output is a registered function and is only valid when the PLL is locked and the Lock Detect output is high. The SD output is undefined for a short time after lock detect assertion or de-assertion due to a data change on the SDI input. See *Figure 3* for a timing diagram showing the relationship between SDI, Lock Detect, and SD.



T_{ACQ} = Acquisition Time, defined in the AC Electrical Characteristics Table

T_1 = Time from Lock Detect assertion or deassertion until SD output is valid, typically 37ns (one 27 MHz clock period)

T_2 = Time from SDI input change until Lock Detect de-assertion, 1 ms maximum. SD output is not valid during this time.

30003105

FIGURE 3. SDI, Lock Detect, and SD

SCO_EN

Input SCO_EN enables the SCO/SDO2 differential output to function either as a serial data-rate clock or second serial data output. SCO/SDO2 functions as a serial data-rate clock when SCO_EN is high. This pin has an internal pull-down device. The default state (low) enables the SCO/SDO2 output as a second serial data output.

CRYSTAL OR EXTERNAL CLOCK REFERENCE

The LMH0036 uses a 27 MHz crystal or external clock signal as a timing reference input. A 27 MHz parallel resonant crystal and load network may be connected to the XTAL IN/EXT CLK and XTAL OUT pins. Alternatively, a 27 MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK. Parameters for a suitable crystal are given in *Table 3*.

TABLE 3. Crystal Parameters

Parameter	Value
Frequency	27 MHz
Frequency Stability	±100 ppm @ recommended drive level
Operating Mode	Fundamental mode, Parallel Resonant
Load Capacitance	20 pF
Shunt Capacitance	7 pF
Series Resistance	40Ω max.
Recommended Drive Level	100 µW
Maximum Drive Level	500 µW
Operating Temperature Range	−10°C to +60°C

Application Information

Figure 4 shows the application circuit for the LMH0036.

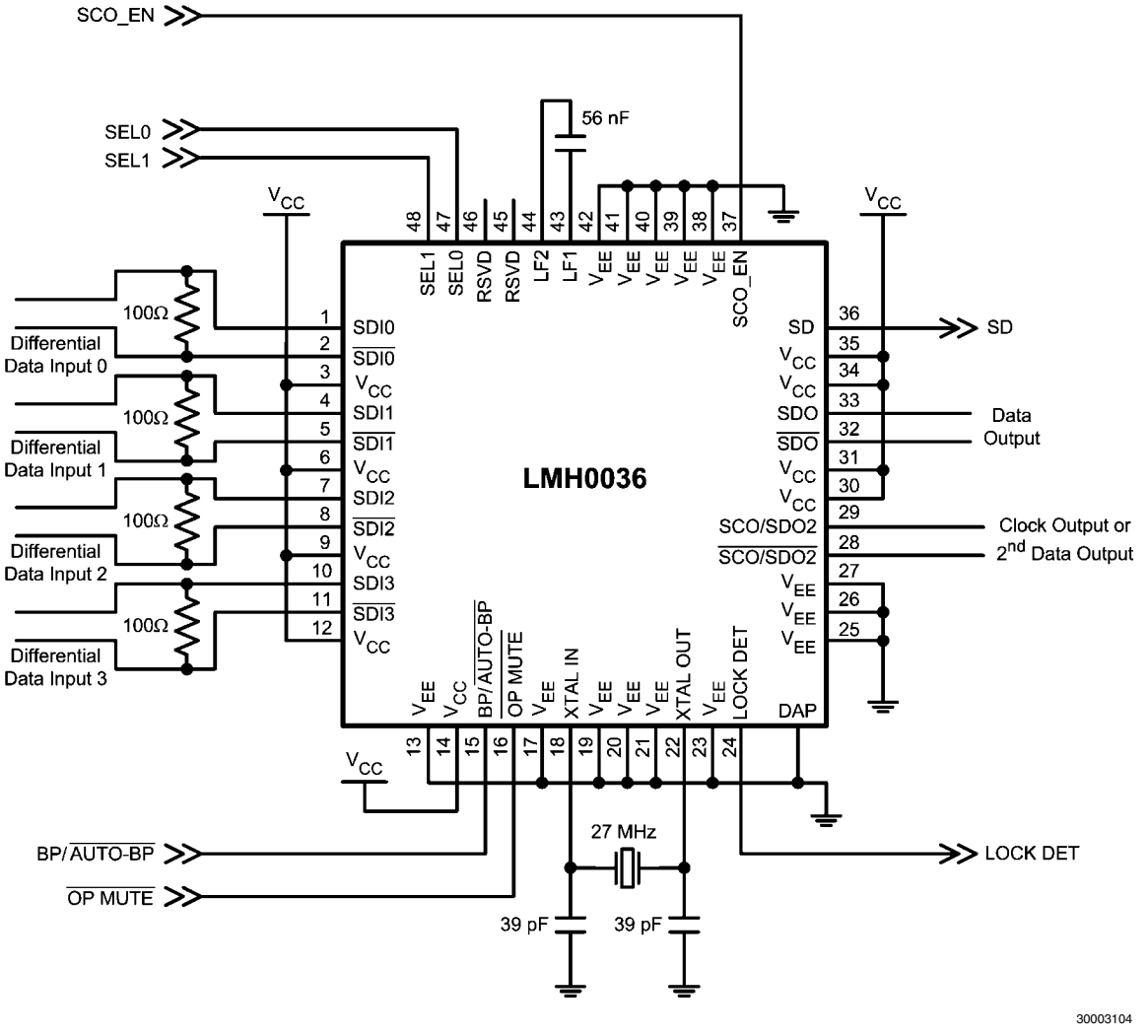
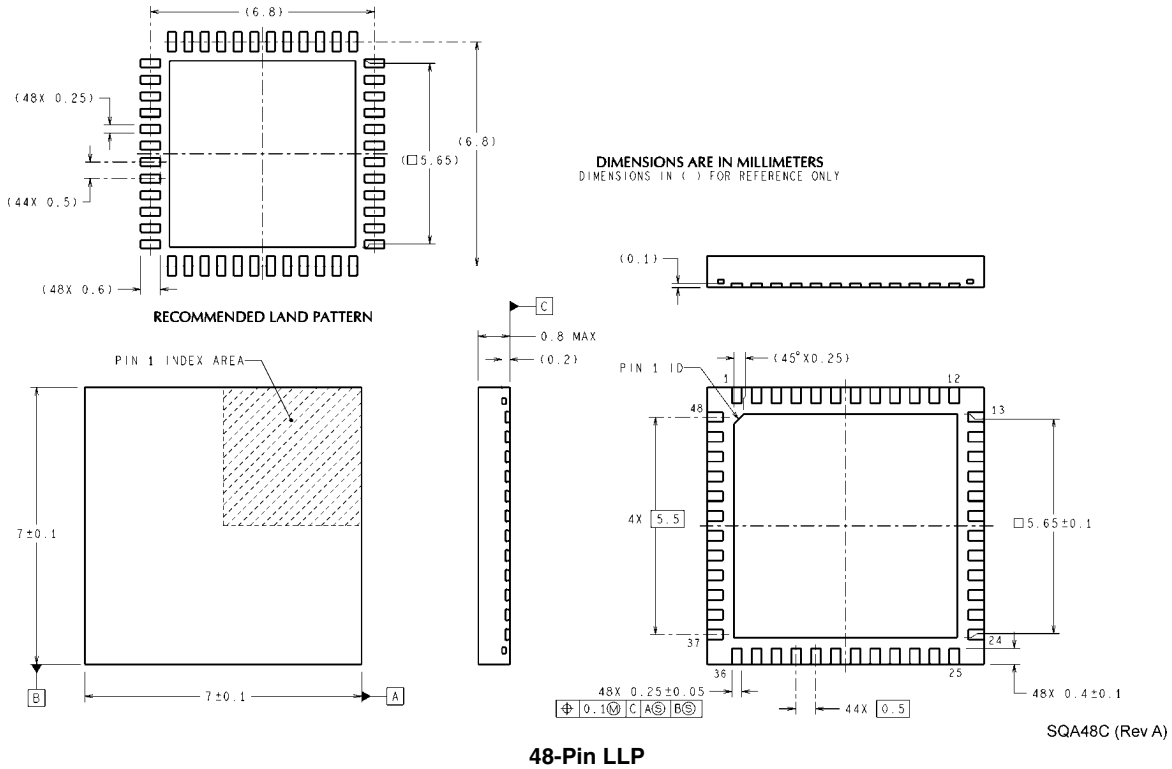


FIGURE 4. Application Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



48-Pin LLP
Order Number LMH0036SQ
NS Package Number SQA48A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

National Semiconductor Americas Technical Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com