National Semiconductor

PRELIMINARY
May 30, 2008

LMH6518
825 MHz, Digital Controlled, Variable Gain Amplifier

General Description

The LMH6518 is a digitally controlled variable gain amplifier whose total gain can be varied from –1.16 dB to 38.84 dB for a 40 dB range in 2 dB steps. The –3 dB bandwidth is 825 MHz at all gains. Gain accuracy at each setting is typically 0.1 dB. When used in conjunction with a National Semiconductor Gsample/second (Gsps) ADC with adjustable full scale (FS) range, the LMH6518 gain adjustment will accommodate full scale input signals from 6.8 mV_{PP} to 920 mV_{PP}.

The LMH6518 gain is programmed via a SPI-1 serial bus. A signal path combined gain resolution of 8.5 mdB can be achieved when the LMH6518's gain and the Gsps ADC's FS input are both manipulated. Propagation Delay variation across gain settings is typically 100 ps. 2nd/3rd order harmonic distortion is –50/–53 dBc at 100 MHz.

Inputs and outputs are dc-coupled. The outputs are differential with individual Common Mode (CM) voltage control (for Main and Auxiliary outputs) and have a selectable bandwidth limiting circuitry (common to both Main & Auxiliary) of 20, 100, 200, 350, 650 MHz, 750 MHz or full bandwidth. The Auxiliary output ("OUT PA" and "OUT NA") follows the Main output and is intended for use in Oscilloscope trigger function circuitry but may have other uses in other applications.

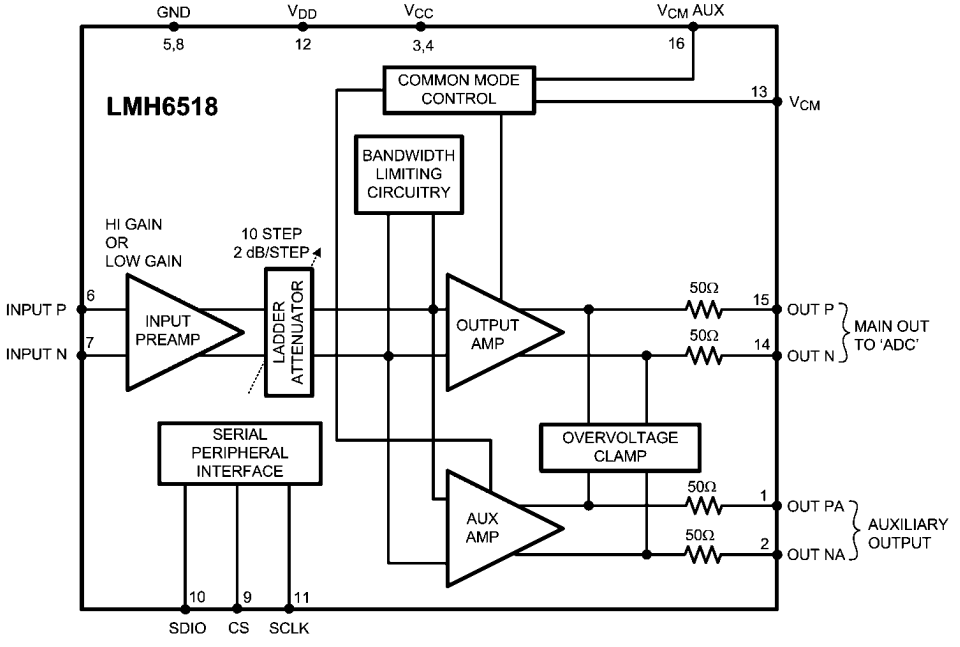
Features

- Gain range 40 dB
- Gain step size 2 dB
- Combined gain resolution with Gsample/second ADC's 8.5 mdB
- Min gain –1.16 dB
- Max gain 38.84 dB
- –3 dB BW 825 MHz
- Rise/fall time 500 ps
- Recovery time 5 ns
- Propagation delay variation 100 ps
- HD2 @ 100 MHz –50 dBc
- HD3 @ 100 MHz –53 dBc
- Input-referred noise (max gain) 0.93 nV/√Hz
- Power consumption 1.1W

Applications

- Oscilloscope programmable gain amplifier
- Differential ADC drivers
- High frequency single ended input to differential conversion
- Precision gain control applications
- Medical applications
- RF/ IF applications

Functional Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	
V_{CC} (5V nominal)	TBD
V_{DD} (3.3V nominal)	TBD

Operating Ratings (Note 1)

Supply Voltage	V_{CC} = 5V (±5%)
	V_{DD} = 3.3V (±5%)
Temperature Range	−40°C to 85°C

Thermal Properties

Junction-to-Ambient	
Thermal Resistance (θJ_A), LLP	45°C/W
Junction Temperature	150°C max

Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, Input CM = 2.5V, V_{CM} = 1.2V, V_{CM} AUX = 1.2V, V_{CC} = 5V, V_{DD} = 3.3V, R_L = 100Ω differential, V_{OUT} = 0.7 V_{PP} differential, Main and Auxiliary Output Specifications, full bandwidth setting, gain = 18.84 dB (Preamp HG, 0 dB ladder attenuation), Full Power setting (Note 3). **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Dynamic Performance						
LSBW	−3 dB Bandwidth	All Gains	750	825		MHz
Peaking	Peaking	All Gains		0.5		dB
GF_0.1dB	±0.1 dB Gain Flatness	All Gains		200		MHz
GF_1dB	±1 dB Gain Flatness	All Gains		600		MHz
TRS	Rise Time			500	TBD	ps
TRL	Fall Time			500	TBD	
OS	Overshoot	Main Output		7		%
t_{s_long}	Long Term Settling time	Main Output, ±0.5%		10		ns
t_{s_short}	Short Term Settling time	Main Output, ±0.05%		14		
t_recover_1	Recovery Time (Note 2)	Preamp HG, 0 dB Ladder ΔV_{IN} = 12 mV_{PP}		5		ns
t_recover_2		Preamp HG, 20 dB Ladder ΔV_{IN} = 120 mV_{PP}		TBD		
t_recover_3		Preamp LG, 0 dB Ladder ΔV_{IN} = 120 mV_{PP}		TBD		
t_recover_4		Preamp LG, 20 dB Ladder ΔV_{IN} = 1.2 V_{PP}		TBD		
PD	Propagation Delay			1.6		ns
PD_var	Propagation Delay Variation	Gain Varied		100		ps
Noise, Distortion, and RF Specifications						
e_{n_1}	Input Noise Spectral Density	Max Gain, 10 MHz		0.93		$nV/\sqrt{Hz}$
e_{n_2}		Preamp LG and 0 dB Ladder Attenuation, 10 MHz		4.3		
e_{no_1}	RMS Output Noise	Preamp LG and 0 dB Ladder Attenuation, 100 Hz to 400 MHz		940		µV
e_{no_2}		Max Gain, 100 Hz to 400 MHz		2.2		mV
NF_1	Noise Figure	Preamp LG and 0 dB Ladder Attenuation, R_S = 50Ω each Input		13.5		dB
NF_2		Max Gain, R_S = 50Ω each Input		3.8		
HD2/ HD3_1	2nd/ 3rd Harmonic Distortion	Main Output, 100 MHz, All Gains		−50/ −53		dBc
HD2/ HD3_2		Auxiliary Output, 100 MHz, All Gains		−48/ −50		
HD2/ HD3_3		Main Output, 250 MHz, All Gains		−44/ −50		
HD2/ HD3_4		Auxiliary Output, 250 MHz, All Gains		−42/ −42		
IMD3	Intermodulation Distortion	f = 250 MHz, Main output		−65		dBc

Symbol	Parameter	Condition	Min	Typ	Max	Units
OIP3_1	Intermodulation Intercept	Main Output, 250 MHz		26		dBm
OIP3_2		Auxiliary Output, 250 MHz		TBD		
P_1dB_main	−1 dB Compression	Main Output, 250 MHz		TBD		dBm
P_1dB_aux		Auxiliary Output, 250 MHz		TBD		
Gain Parameters						
A_{V_MAX}	Max Gain	Up to 50 MHz	37.84	38.84	39.84	dB
A_{V_MIN}	Min Gain		−2.16	−1.16	−0.16	dB
Gain_step	Gain Step Size	Up to 50 MHz	1.8	2	2.2	dB
	Gain Step Size with ADC See (Note 1)	ADC FS Adjusted		8.5		mdB
Gain_Range	Gain Range		39	40	41	dB
TC_A_V	Gain Temp Coefficient	0 to 40°C		−1	±10	mdB/°C
$Gain\_A_{CC}$	Absolute Gain Accuracy	Up to 50 MHz	TBD	0.1	TBD	dB
Matching Specifications						
Gain_match	Gain Matching Main/Auxiliary	All Gains		±0.1		dB
BW_match	−3 dB Bandwidth Matching Main/ Auxiliary	All Gains		5		%
RT_match	Rise Time Matching Main/ Auxiliary	All Gains		5		%
PD_match	Propagation Delay Matching Main/ Auxiliary	All Gains		TBD		ps
Analog I/O						
V_{IN_MAX}	Maximum Differential Input voltage	Min Gain	TBD	0.8		V_{PP}
CMVR	Common Mode Voltage Range		TBD	2V to 3V	TBD	V
Z_{in_diff}	Differential Input Impedance	All Gains		150||1.5		KΩ || pF
Z_{in_CM}	CM Input impedance	Preamp HG		420||1.7		
		Preamp LG		900||1.7		
FS_{OUT1}	Full Scale Voltage Swing	Main Output, THD < −40 dBc @ 100 MHz	770	800		mV_{PP}
FS_{OUT2}		Auxiliary Output	TBD	700		
I_{OUT_1}	Maximum Output Current	Main Output, Sourcing		TBD		mA
I_{OUT_2}		Auxiliary Output, Sourcing		TBD		
I_{OUT_3}		Main Output, Sinking		TBD		
I_{OUT_4}		Auxiliary Output, Sinking		TBD		
Z_{out_diff}	Differential Output Impedance		TBD	100	TBD	Ohms
V_{OOS}	Output Offset Voltage	All Gain Settings		TBD	**±50**	mV
TCV_{OOS}	Output Offset Voltage Drift	0 to 40°C		500	TBD	µV/°C
VOCM	Output CM voltage range		**0.95**	1.2	**1.45**	V
V_{OS_CM}	Output CM offset voltage			15	**TBD**	mV
$TC\_V_{OS\_CM}$	CM Offset Voltage Temp Coefficient			TBD		mV/°C
BAL_Error_DC	Output Gain Balance Error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$		-70		dB
BAL_Error_AC		f = 750 MHz, $\frac{v_{O\_CM}}{v_{OUT}}$		-45		
BAL_Error_AC_ Phase	Output Phase Balance Error	f = 750 MHz, (V_{OUT+} - V_{OUT-}) Phase		±0.8		deg
PSRR1	Output Referred Differential Power Supply Rejection	Preamp HG		−80		dB
PSRR2		Preamp LG		−70		
PSRR_CM	CM Power Supply Rejection			TBD		dB
CMRR	CM Rejection Ratio	2V < CMVR < 3V , DC (see definition)		TBD		dB

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CM_I}	V_{CM} Input Bias Current			1	**TBD**	nA
$V_{CM\_AUX\_I}$	V_{CM_AUX} Input Bias Current			1	**TBD**	
Digital I/O & Timing						
Logic	Input/Output Levels		**3.0**	3.3	**3.6**	V
I_in	Input Bias Current			TBD		nA
CLK_max	Maximum SCLK Rate			TBD		KHz
Power Requirements						
I_{S1}	Supply Current	V_{CC}		210	TBD	mA
I_{S1_off}		V_{CC} Aux off		150	TBD	
I_{S2}		V_{DD}		160	TBD	µA
P_{O_FP}	Power Consumption	Full Power		1.1		W
$P_{O\_AUX\_off}$		Aux off		0.75		
Bandwidth Limiting Filter Specifications						
Filter	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Units**
20 MHz	Pass Band Tolerance	−3 dB Bandwidth		−0, +20		%
	Pass Band Tolerance (Gain Varied)			TBD		
	Stop Band Attenuation	at 40 MHz		−7		dB
100 MHz	Pass Band Tolerance	−3 dB Bandwidth		−0, +20		%
	Pass Band Tolerance (Gain Varied)			TBD		
	Stop Band Attenuation	at 200 MHz		−7		dB
200 MHz	Pass Band Tolerance	−3 dB Bandwidth		−0, +20		%
	Pass Band Tolerance (Gain Varied)			TBD		
	Stop Band Attenuation	at 400 MHz		−6.5		dB
350 MHz	Pass Band Tolerance	−3 dB Bandwidth		±10		%
	Pass Band Tolerance (Gain Varied)			±25		
	Stop Band Attenuation	at 750 MHz		−8		dB
650 MHz	Pass Band Tolerance	−3 dB Bandwidth		±10		%
	Pass Band Tolerance (Gain Varied)			±25		
	Stop Band Attenuation	at 1 GHz		−9		dB
750 MHz	Pass Band Tolerance	−3 dB Bandwidth		±10		%
	Pass Band Tolerance (Gain Varied)			±25		
	Stop Band Attenuation	at TBD		TBD		dB

Definition of Terms and Specifications

1.	CMRR (dB)	Differential Gain – CM Gain (from input to output).
2.	CM	Common Mode
3.	ΔV_{O_CM}	Variation in output common mode voltage (V_{O_CM}).
4.	ΔV_{OUT}	Change in differential output voltage (Corrected for DC offset (Voos)).
5.	Voos	DC offset voltage. Differential output voltage measured with inputs shorted together to $V_{CC}/2$.
6.	ΔV_{IN} (V)	Differential voltage across device inputs.
7.	$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$	Balance Error. Measure of the output swing balance of “out P” and “out N”, as reflected on the output common mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common mode voltage change (ΔV_{O_CM}) divided by the output differential voltage change (ΔV_{OUT}, which is nominally around 700 mV_{PP}).
8.	Out P	Positive Main Output
9.	Out N	Negative Main Output
10.	Out PA	Positive Auxiliary Output
11.	Out NA	Negative Auxiliary Output
12.	PSRR	Differential output change (ΔV_{OUT}) with respect to V_{CC} voltage change (ΔV_{CC}) with nominal differential output.
13.	PSRR_CM	Output common mode voltage change (ΔV_{O_CM}) with respect to V_{CC} voltage change (ΔV_{CC}).
14.	HG	Preamp High Gain
15.	LG	Preamp Low Gain
16.	Ladder	Ladder Attenuator setting (0-20 dB
17.	Min Gain	Gain = −1.16 dB
18.	Max Gain	Gain = 38.84 dB

Note 1: Gain Step Size with ADC: With the National Semiconductor GigaSample/second ADC Full Scale (FS) adjustment (512 steps from 0.56V to 0.84V), the worst case gain step size would be:

$$\text{Gain step size} = 20 \log \frac{0.56 + \left(\frac{0.84 - 0.56}{2 \times 512}\right)}{0.56 - \left(\frac{0.84 - 0.56}{2 \times 512}\right)} = 8.5 \text{ mdB}$$

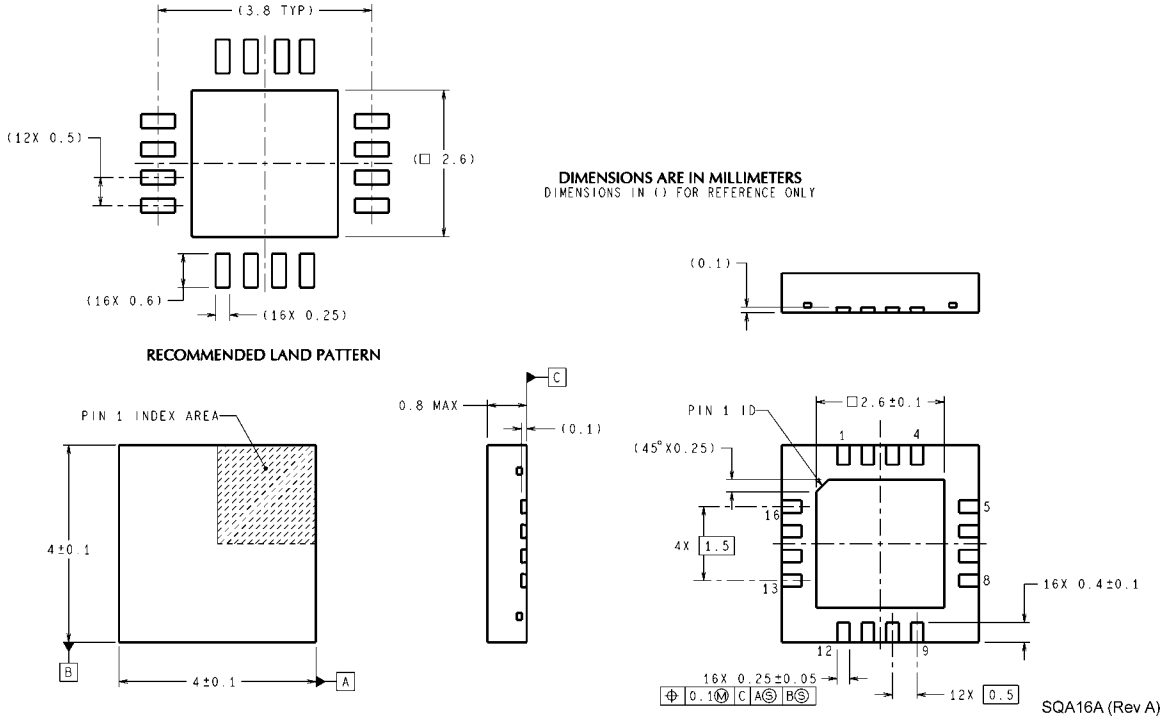
Note 2: “Recovery time” is the slower of the Main and Auxiliary outputs. Measured values correspond to time it takes to return to zero.

Note 3: ”Full Power” setting is with Auxiliary output turned on.

Pin Out

Pin Out	Function
P1 = Out PA	Auxiliary positive output
P2 = Out NA	Auxiliary negative output
P3 = V_{CC} (5V)	Analog power supply
P4 = V_{CC} (5V)	Analog power supply
P5 = Gnd	Ground, electrically connected to the LLP heat sink
P6 = Input P	Positive Input
P7 = Input N	Negative Input
P8 = Gnd	Ground, electrically connected to the LLP heat sink
P9 = CS	SPI interface, Chip Select, Active low
P10 = SDIO	SPI interface, Serial Data Input/Output
P11 = SCLK	SPI interface, Clock
P12 = V_{DD} (3.3V)	Digital power supply
P13 = V_{CM}	Input from ADC to control main output CM
P14 = Out N	Main positive output
P15 = Out P	Main negative output
P16 = V_{CM_AUX}	Input from ADC to control auxiliary output CM

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin Package
NS Package Number SQA16A

Notes

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