July 24, 2008

National Semiconductor

LMH6586
32x16 Video Crosspoint Switch

General Description

The LMH6586 is a non-blocking 32x16 analog video crosspoint switch. It can be used to route standard composite video signals, (NTSC and PAL) and any one of the 32 inputs can be routed to any one of the 16 outputs. The LMH6586 can operate in broadcast mode as well as individual mode. The outputs have programmable 1X or 2X gain output buffers and can drive loads of 150Ω. Each input has an integrated DC-restore clamp for AC-coupled operation.

The LMH6586 operates from a common single +5V supply for its analog sections as well as its digital logic and I²C interface. The LMH6586 also has two types of input signal detection ideal for security camera monitoring. It can be configured to output a flag upon the loss of sync with an external voltage control pin used to set the sync detection threshold level. It can also be configured to output a flag upon the detection of presence or absence of video with an 8-level programmable video detection threshold.

The crosspoint switch matrix configuration is programmed via a 100 kHz I²C compatible interface. The device address is 2-bit programmable, accommodating up to four LMH6586's on a common I²C bus, facilitating expansion of the Crosspoint matrix.

The LMH6586 is offered in a space-saving 80-pin TQFP.

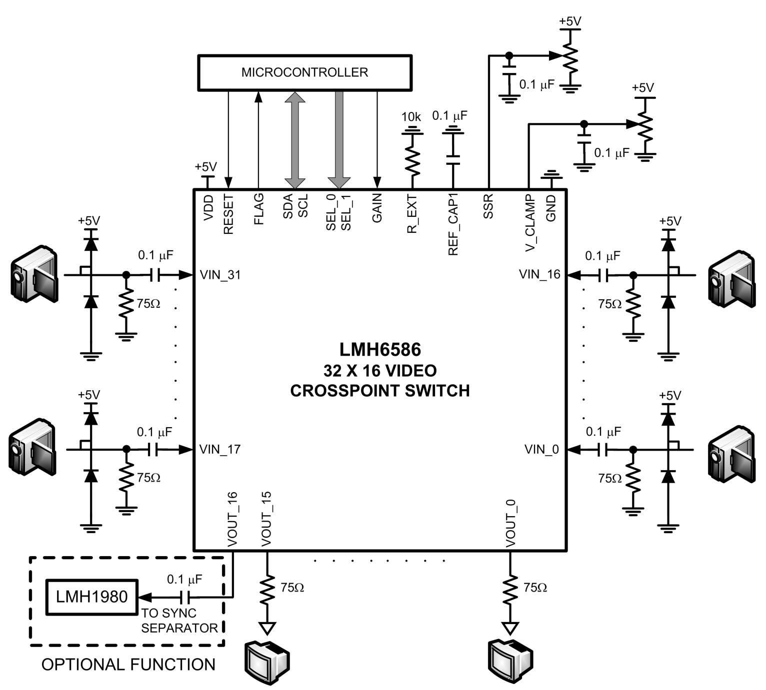
Features

- 32x16 Non-blocking Switch with buffered inputs and outputs.
- 100 kHz I²C compatible interface
- Individually addressable outputs
- Input video clamp
- Selectable output buffer gain (+1V/V or +2V/V)
- −3 dB Bandwidth = 66 MHz
- DG = 0.05%, DP = 0.05° @ R_L = 150Ω
- −70 dB off-isolation @ 6 MHz
- I²C compatible interface with 2-bit programmable slave address
- Single +5V supply operation
- Input and output amp power shutdowns
- Video detect with 8 adjustable programmable threshold level
- Sync detect with adjustable programmable threshold level
- Extra video output for external sync separator (OUT16)

Applications

- CCTV security systems
- Video routing

Typical Operating Circuit



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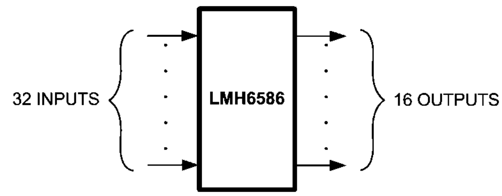


INTERNAL BLOCK DIAGRAM

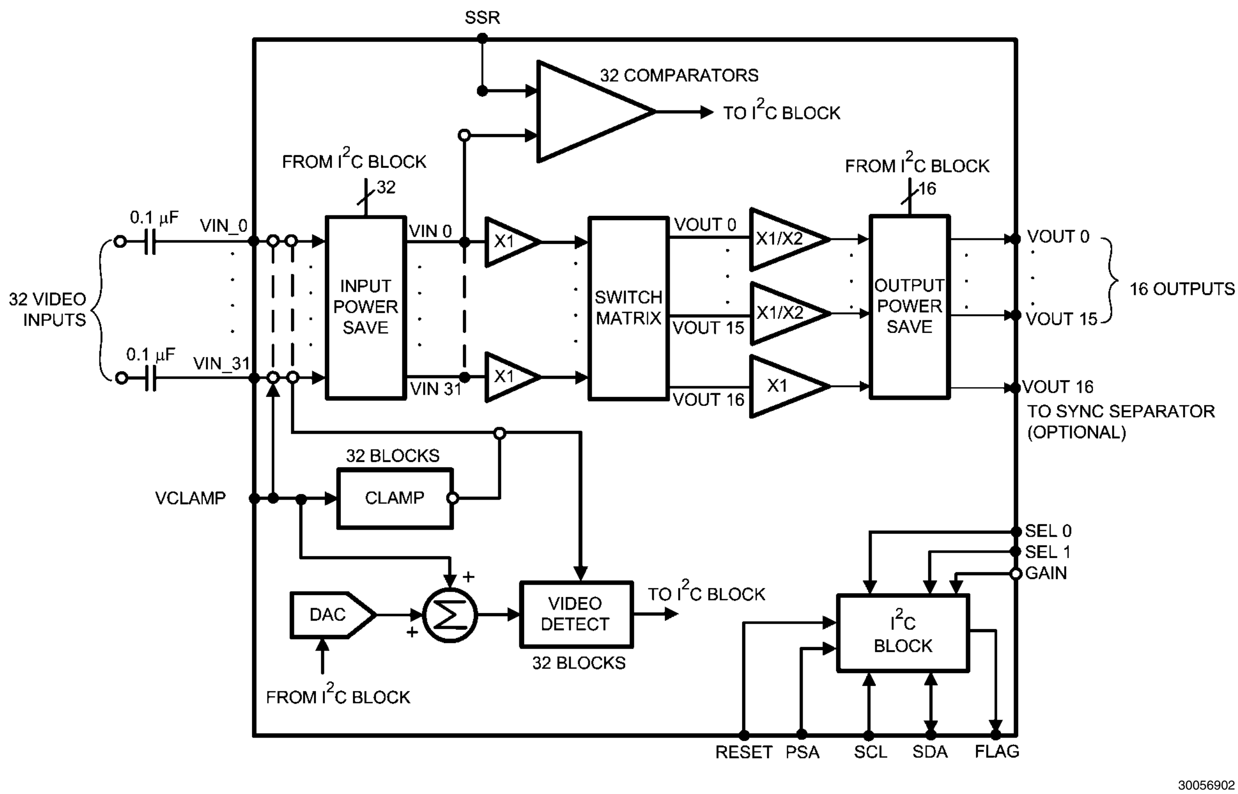
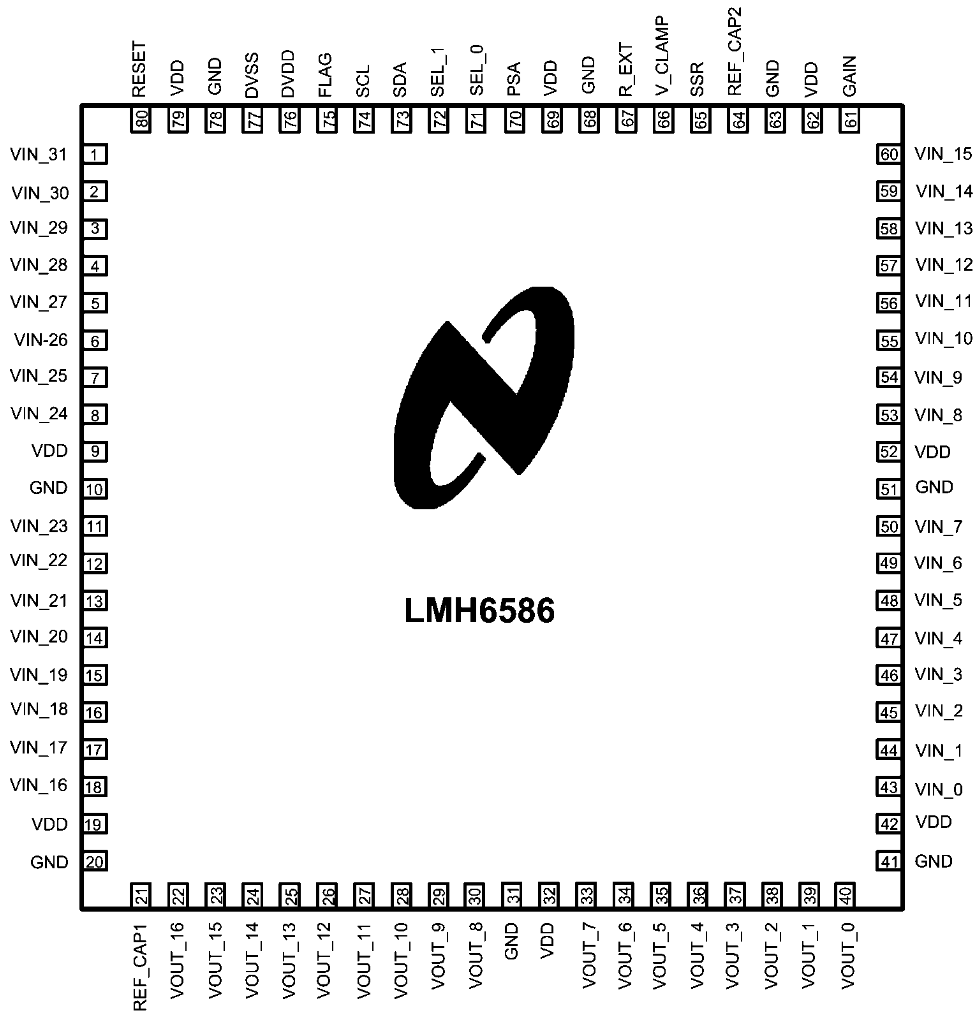


FIGURE 1. Functional Diagram

Connection Diagram



Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
80-Pin TQFP	LMH6586VS	LMH6586VS	160 Units/Tray	VHB80A

Pin Description

Pin #	Pin Description	Pin #	Pin Description
1	VIDEO INPUT 31	41	GND
2	VIDEO INPUT 30	42	V_{DD} +5V SUPPLY
3	VIDEO INPUT 29	43	VIDEO INPUT 0
4	VIDEO INPUT 28	44	VIDEO INPUT 1
5	VIDEO INPUT 27	45	VIDEO INPUT 2
6	VIDEO INPUT 26	46	VIDEO INPUT 3
7	VIDEO INPUT 25	47	VIDEO INPUT 4
8	VIDEO INPUT 24	48	VIDEO INPUT 5
9	V_{DD} +5V SUPPLY	49	VIDEO INPUT 6
10	GND	50	VIDEO INPUT 7
11	VIDEO INPUT 23	51	GND
12	VIDEO INPUT 22	52	V_{DD} +5V SUPPLY
13	VIDEO INPUT 21	53	VIDEO INPUT 8
14	VIDEO INPUT 20	54	VIDEO INPUT 9
15	VIDEO INPUT 19	55	VIDEO INPUT 10
16	VIDEO INPUT 18	56	VIDEO INPUT 11
17	VIDEO INPUT 17	57	VIDEO INPUT 12
18	VIDEO INPUT 16	58	VIDEO INPUT 13
19	V_{DD} +5V Supply	59	VIDEO INPUT 14
20	GND	60	VIDEO INPUT 15
21	REF_CAP1	61	GAIN
22	VIDEO OUTPUT 16	62	V_{DD} +5V SUPPLY
23	VIDEO OUTPUT 15	63	GND
24	VIDEO OUTPUT 14	64	REF_CAP2 (external coupling cap 0.1 µF)
25	VIDEO OUTPUT 13	65	SSR (Sync separator reference)
26	VIDEO OUTPUT 12	66	V_CLAMP
27	VIDEO OUTPUT 11	67	R_EXT (external resistor for bias)
28	VIDEO OUTPUT 10	68	GND
29	VIDEO OUTPUT 9	69	V_{DD} +5V SUPPLY
30	VIDEO OUTPUT 8	70	POWER SAVE ENABLE (complete chip)
31	GND	71	ADDRESS SELECT [0]
32	V_{DD} +5V SUPPLY	72	ADDRESS SELECT [1]
33	VIDEO OUTPUT 7	73	SDA
34	VIDEO OUTPUT 6	74	SCL
35	VIDEO OUTPUT 5	75	INPUT DETECT FLAG
36	VIDEO OUTPUT 4	76	DIGITAL V_{DD} +5V SUPPLY
37	VIDEO OUTPUT 3	77	DIGITAL GND
38	VIDEO OUTPUT 2	78	GND
39	VIDEO OUTPUT 1	79	V_{DD} +5V SUPPLY
40	VIDEO OUTPUT 0	80	RESET

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2500V
Machine Model	250V
Supply Voltage (V_{DD})	5V
Video Input Voltage Range, V_{IN}	−0.3V to V_{DD} +0.3V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	+150°C

Operating Ratings (Note 1)

Supply Voltage (V_{DD})	+5V ±10%
Ambient Temperature Range	−40°C ≤ T_A ≤85°C
θ_{JA}	25°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{DD} = +5V, R_{EXT} = 10 kΩ 1%, V_{CLAMP} = 0.3V, R_L = 150Ω, C_L = 12 pF.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Specifications						
V_{DD}	Operating Supply Voltage		4.5		5.5	V
I_{DD}	Supply Current	No Load, A_V = 1 V/V		300	360	mA
	Power Save Supply Current	No Load, A_V = 1 V/V			1.4	μA
A_V	Gain	2x Gain Buffer	1.92	2.00	2.07	V/V
		1x Gain Buffer	0.95	0.99	1.03	
ΔA_{V_CH-CH}	Gain Matching (Ch to Ch)	A_V = 1 V/V		1.2	3	%
V_{OS}	Output Offset Voltage	A_V = 1 V/V, No Load (referenced to DC restored input)		60		mV
V_{DET_LSB}	Video Detect Threshold LSB		85	95	105	mV
V_{DET}	Video Detect Threshold Offset	Video detection threshold offset measured above sync tip		±50		mV
AC Specifications						
BW_{SS}	Small Signal Bandwidth (–3 dB)	V_{OUT} = 20 mV_{PP}		66		MHz
BW_{LS}	Large Signal Bandwidth (–3 dB)	V_{OUT} = 1.5 V_{PP}		29		MHz
t_r/t_f	Rise/Fall Time	10% to 90%, V_{OUT} = 2 V_{PP}		35		ns
tp	Propagation Delay	50% to 50%, V_{OUT} = 2 V_{PP}		5		ns
t_{pCh-Ch}	Ch-Ch Propagation Delay	50% to 50%, V_{OUT} = 2 V_{PP}		5		ns
CT	Adjacent CH Crosstalk	f = 6 MHz, A_V = 2 V/V		–58		dB
Off Iso	Input-Output Off-Isolation	f = 6 MHz, A_V = 2 V/V		–70		dB
DG	Differential Gain Error for NTSC	A_V = 2 V/V, 3.5 MHz		0.05		%
DP	Differential Phase Error for NTSC	A_V = 2 V/V, 3.5 MHz		0.05		deg
I²C Interface and Digital Pin Logic Levels						
V_{IL}	Low Input Voltage				1.5	V
V_{IH}	High Input Voltage		3.3			V
I_{IN}	Input Current			±1		μA
V_{OL}	Low Output Voltage	I_{OL} = 3 mA		0.5		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$ and θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: All voltages are measured with respect to GND, unless otherwise specified.

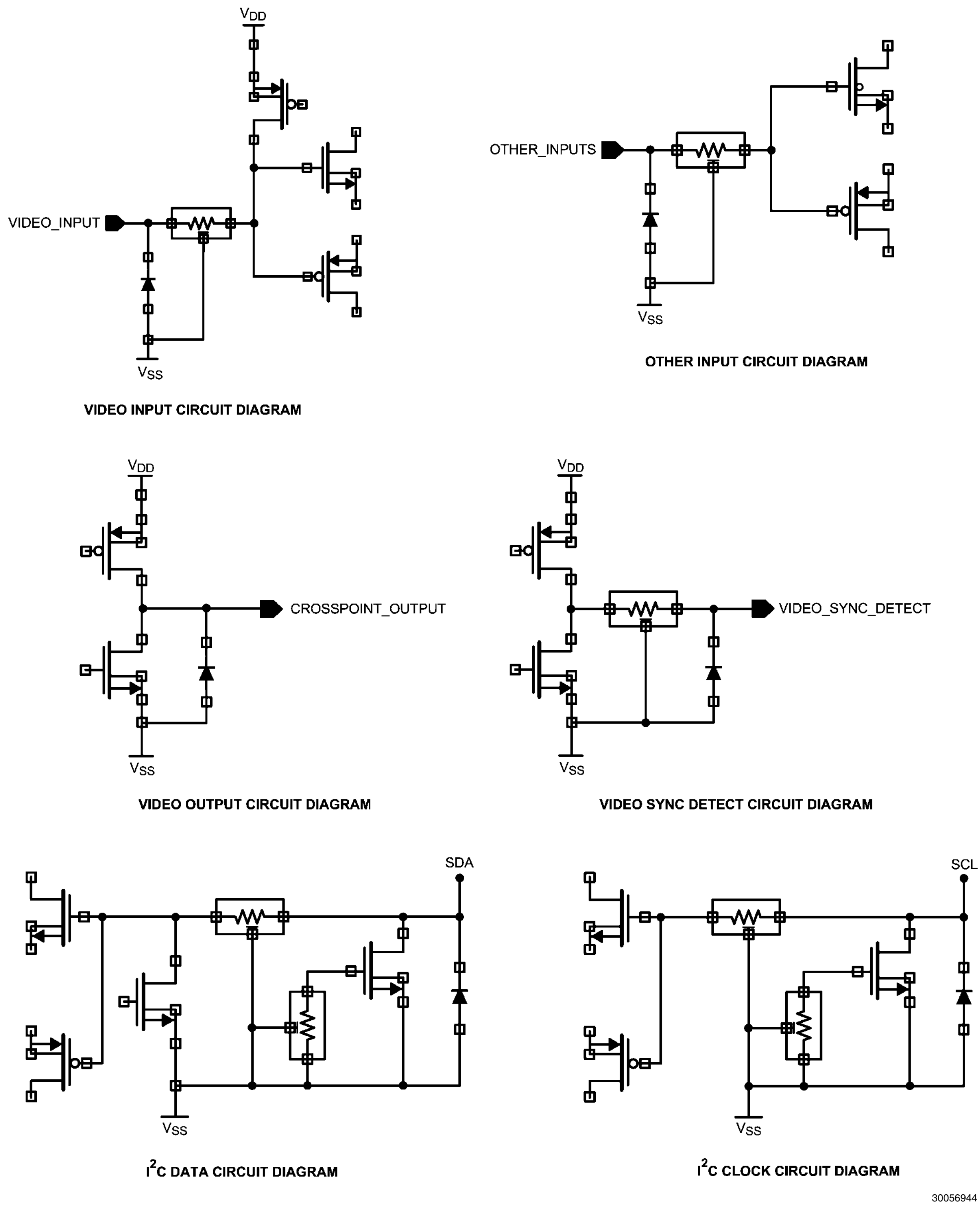
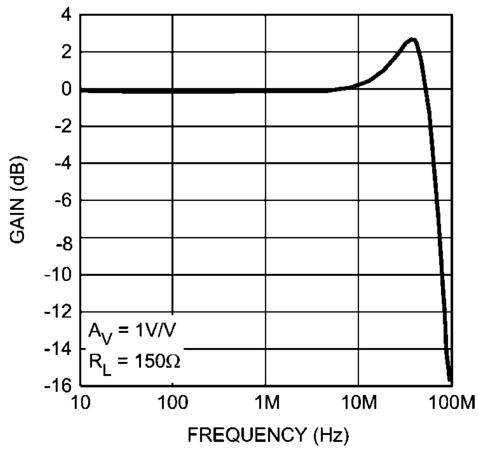


FIGURE 2. Logic Diagram

Typical Performance Characteristics

Small Signal Bandwidth



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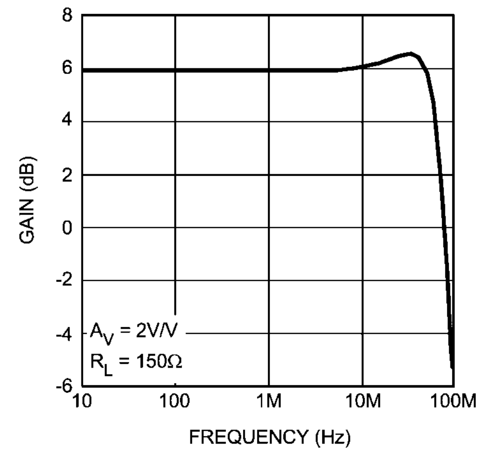
Small Signal Bandwidth



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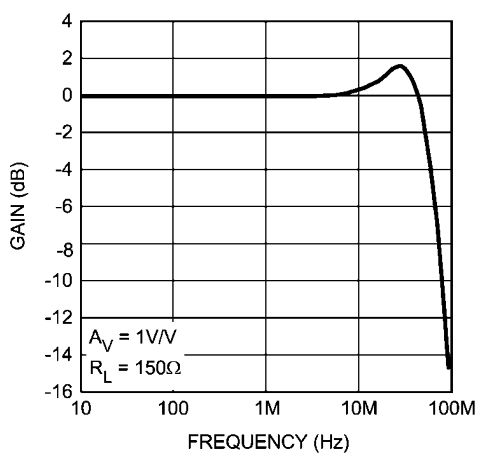
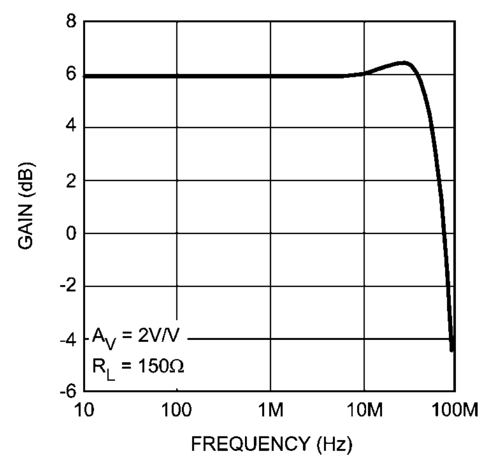
Medium Signal Bandwidth



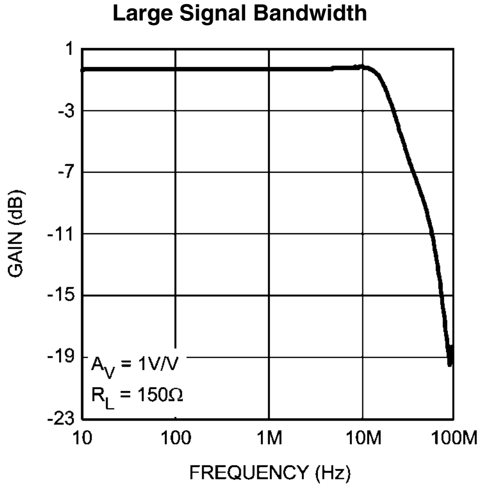
30056908

Medium Signal Bandwidth



30056909

Large Signal Bandwidth



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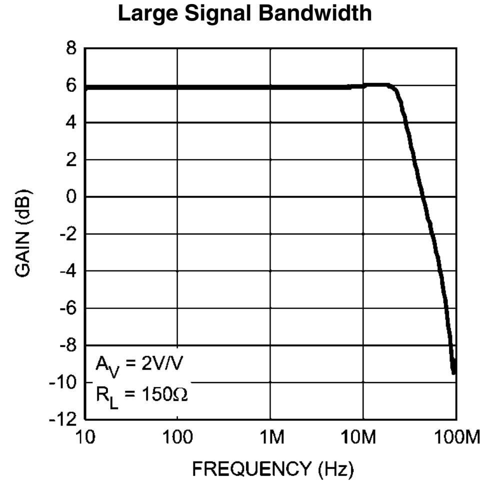
Large Signal Bandwidth



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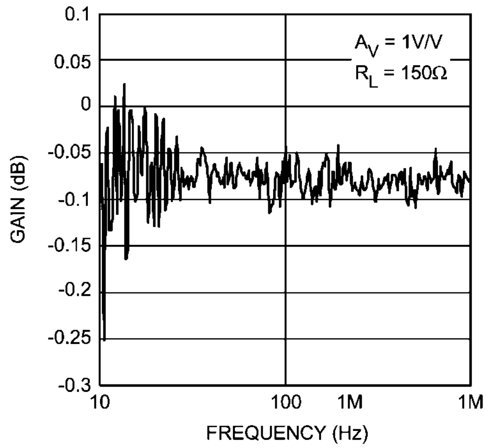
Small Signal Gain Flatness



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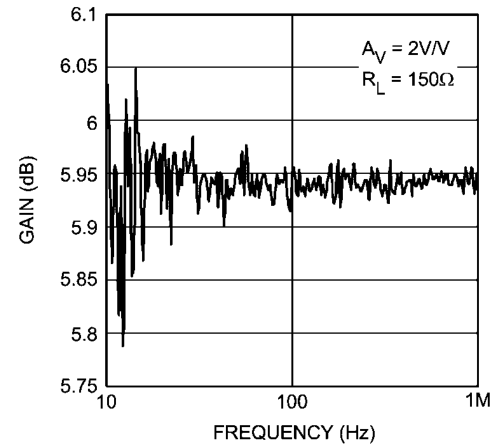
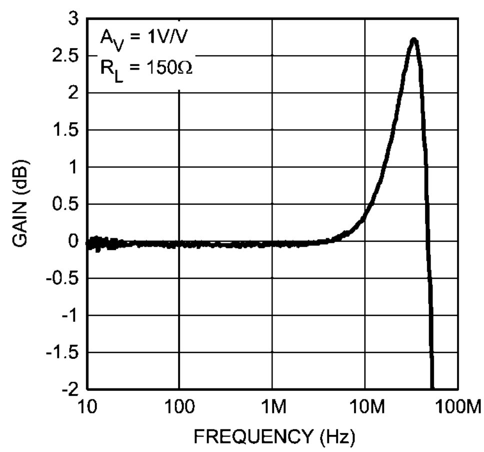
Small Signal Gain Flatness



30056913

Small Signal Gain Peaking



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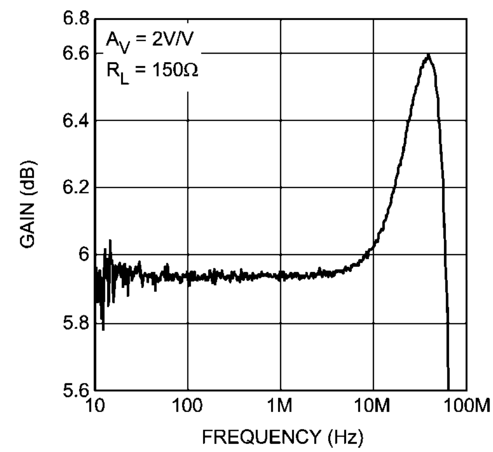
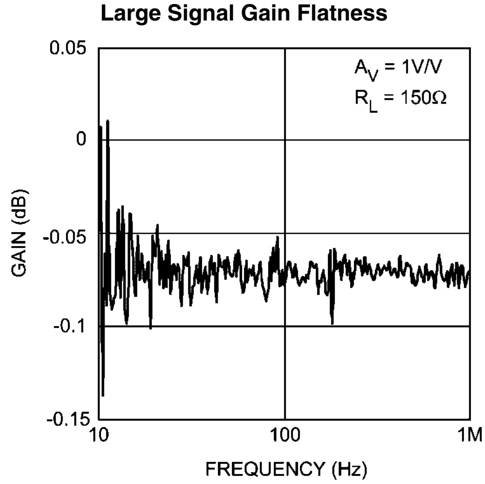
Small Signal Gain Peaking



30056915

Large Signal Gain Flatness



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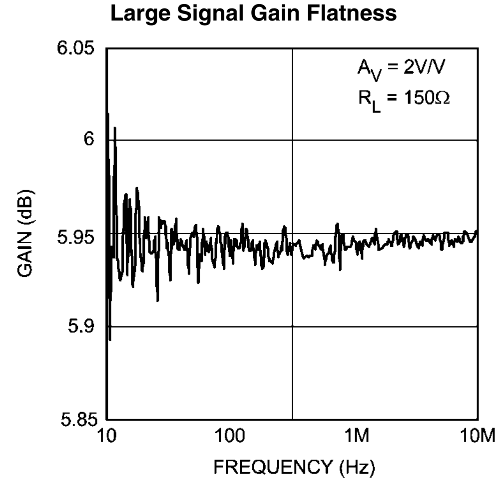
Large Signal Gain Flatness



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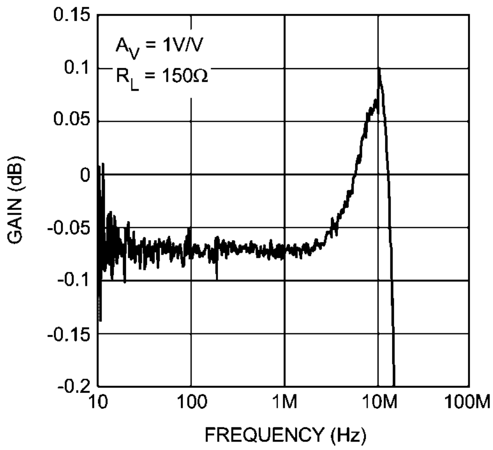
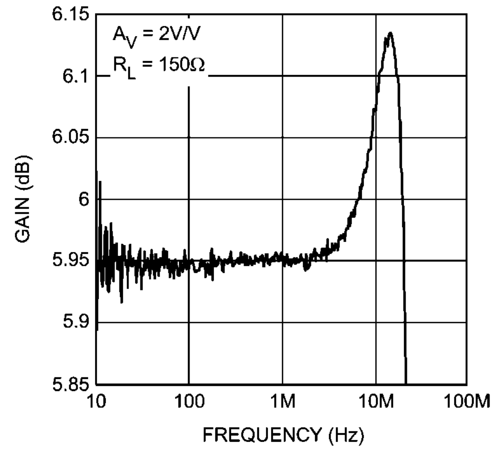
Large Signal Gain Peaking



30056918

Large Signal Gain Peaking



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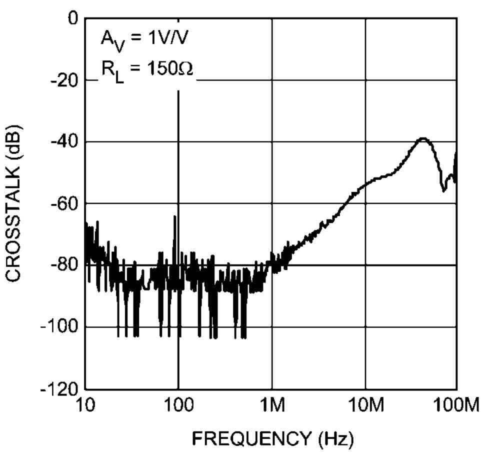
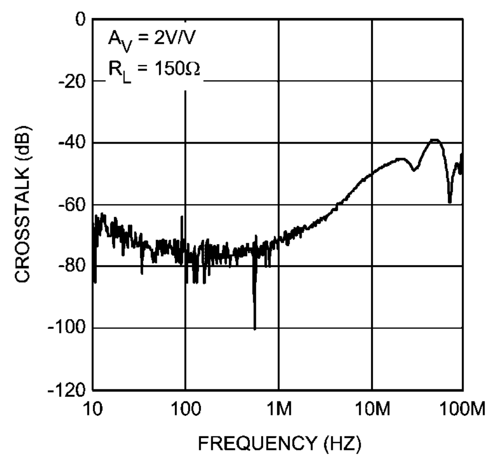
Adjacent Channel Crosstalk



30056920

Adjacent Channel Crosstalk



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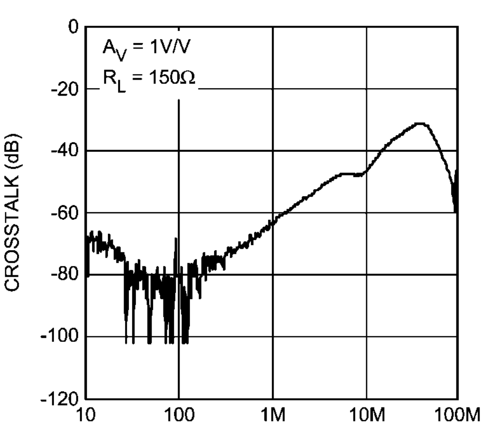
All Hostile Crosstalk



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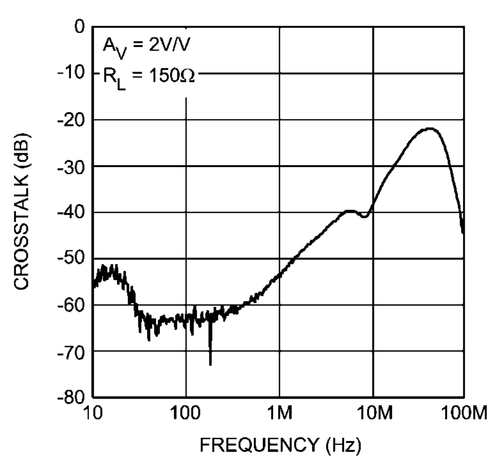
All Hostile Crosstalk



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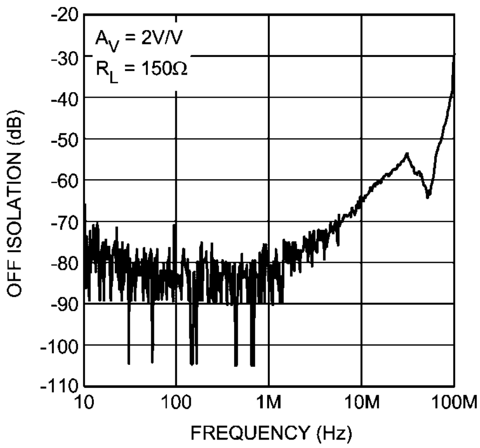
Off Isolation



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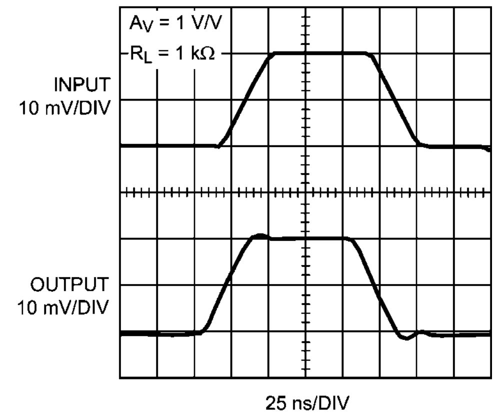
Small Signal Pulse Response



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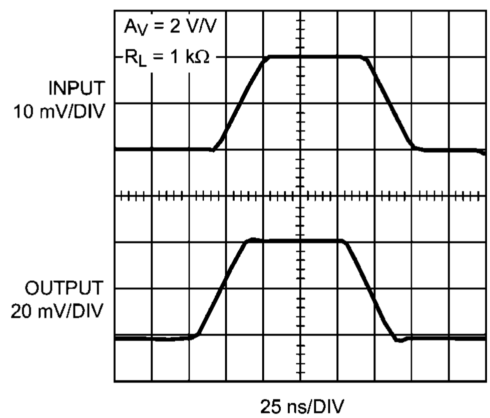

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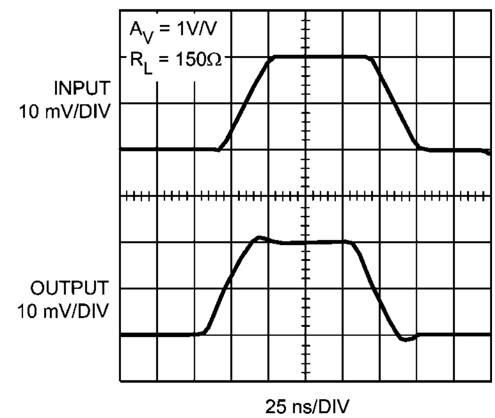
Small Signal Pulse Response



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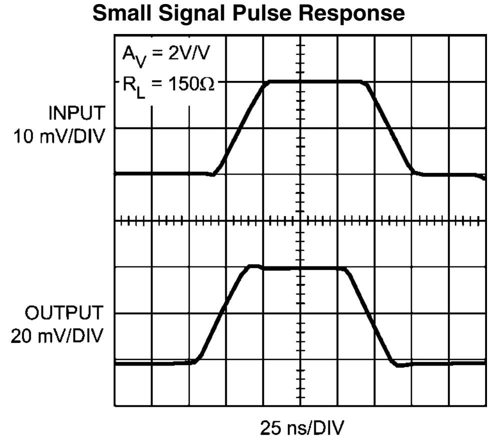
Small Signal Pulse Response



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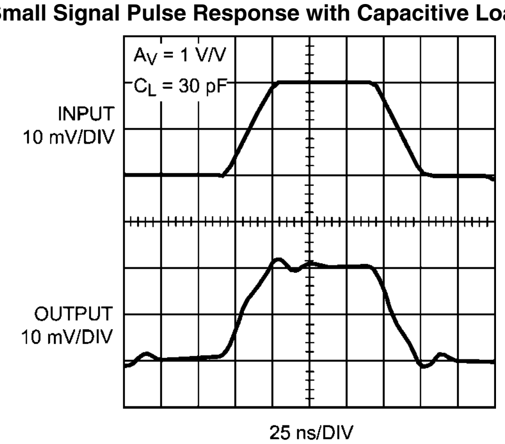
Small Signal Pulse Response with Capacitive Load



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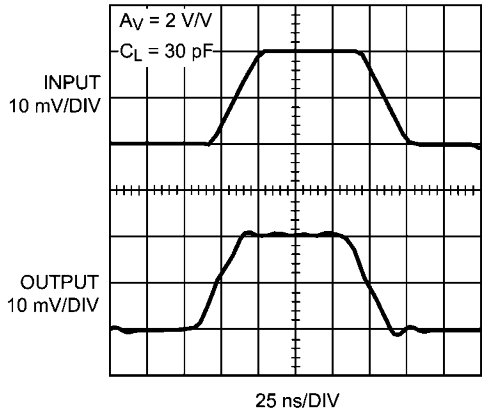

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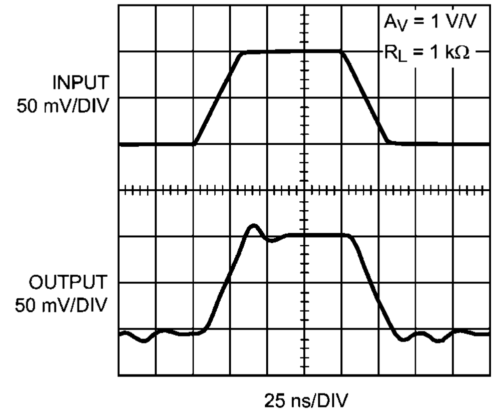
Medium Signal Pulse Response



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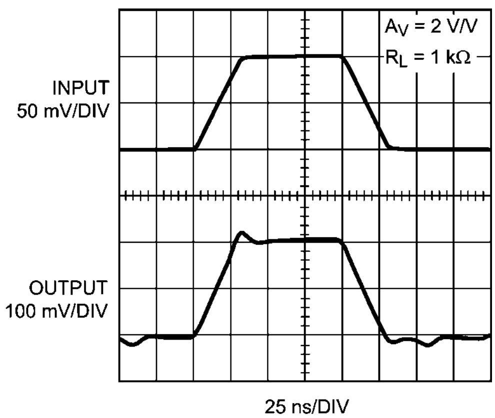
Medium Signal Pulse Response



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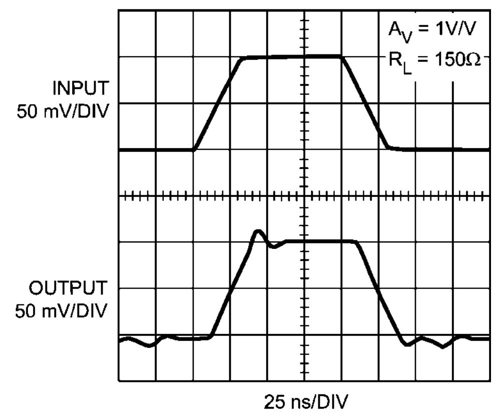
Medium Signal Pulse Response



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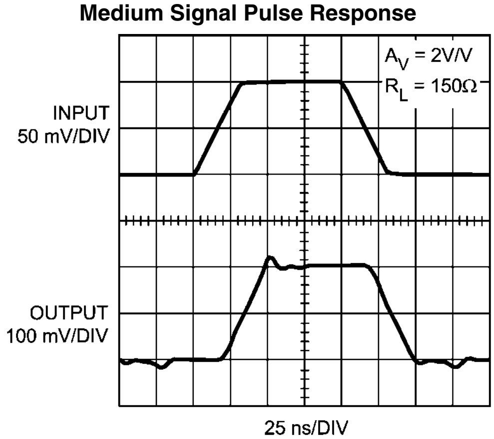
Medium Signal Pulse Response



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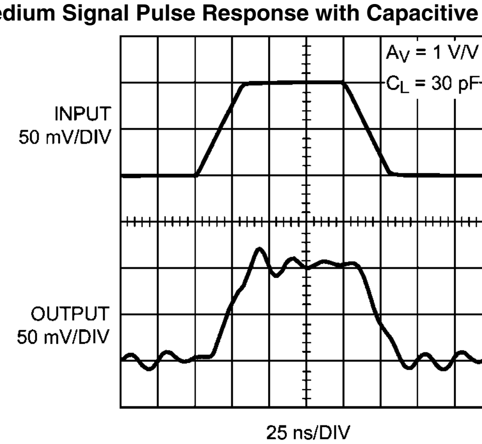
Medium Signal Pulse Response with Capacitive Load



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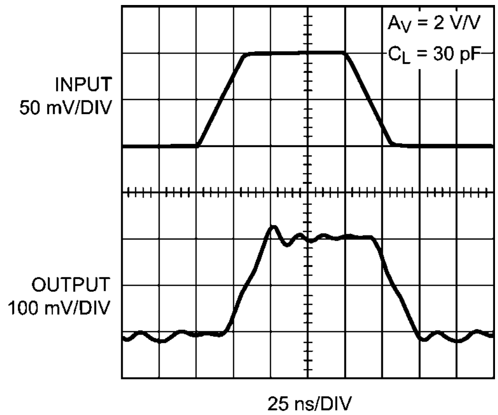
Medium Signal Pulse Response with Capacitive Load



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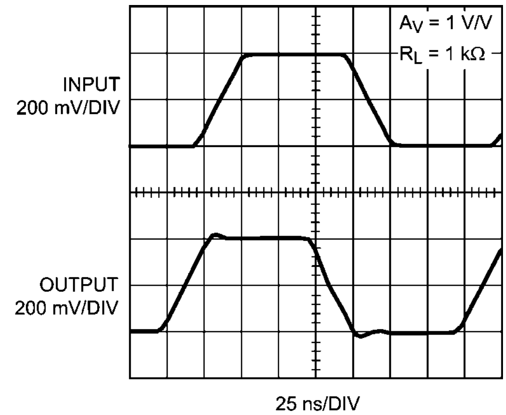
Large Signal Pulse Response



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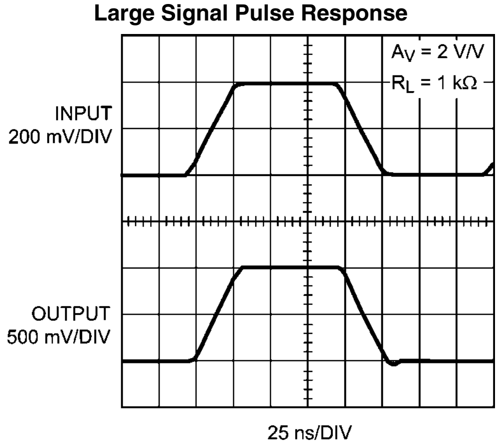

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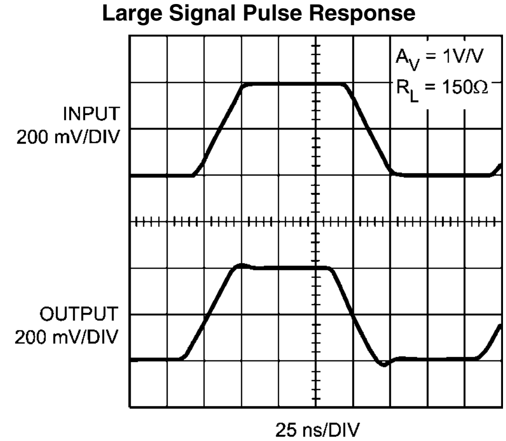

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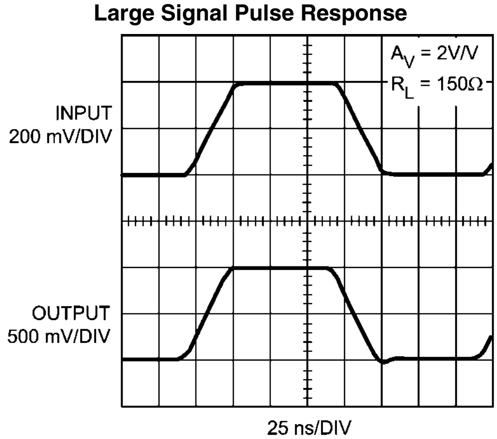
Large Signal Pulse Response



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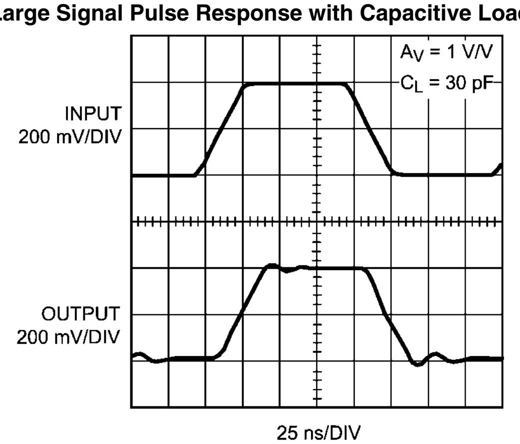
Large Signal Pulse Response with Capacitive Load



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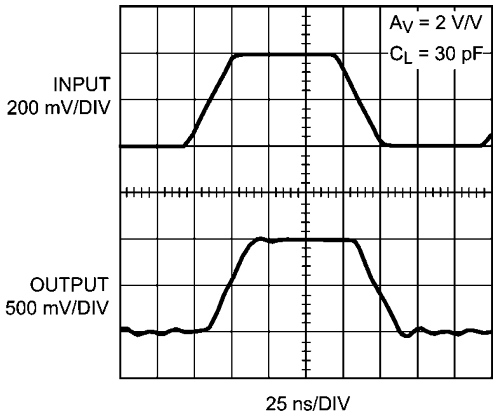
Large Signal Pulse Response with Capacitive Load



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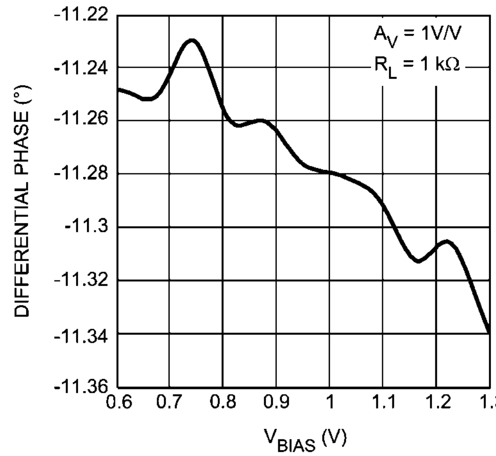
Differential Phase



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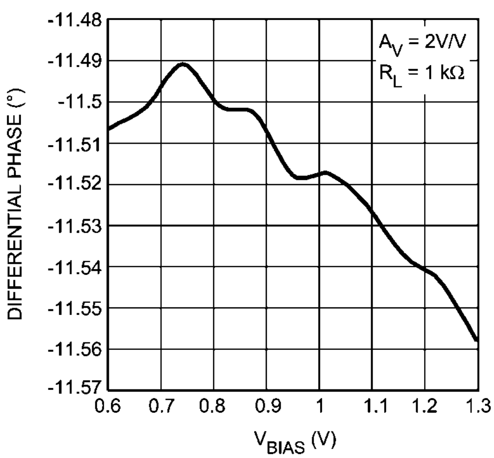
Differential Phase



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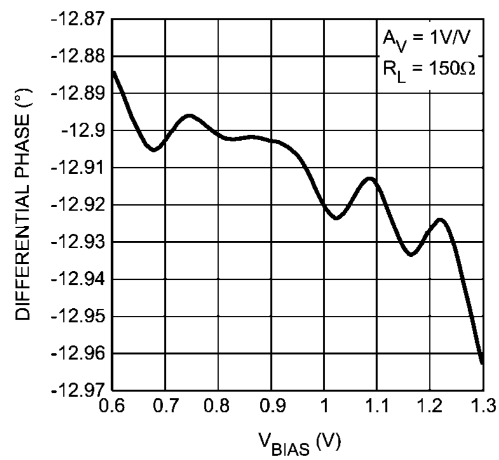
Differential Phase



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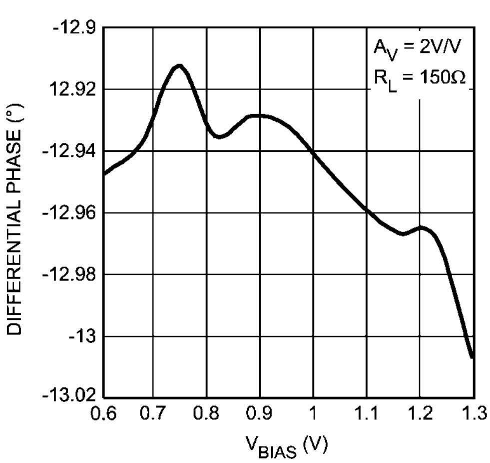
Differential Phase



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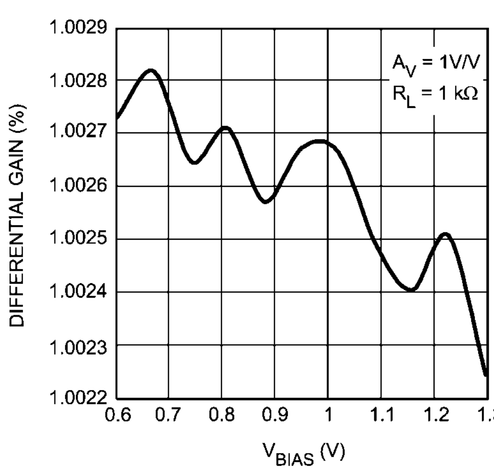
Differential Gain



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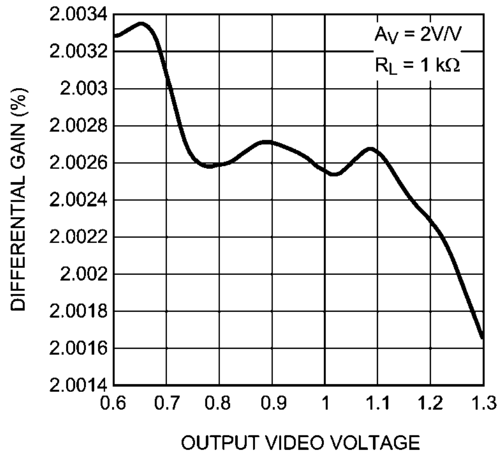
Differential Gain



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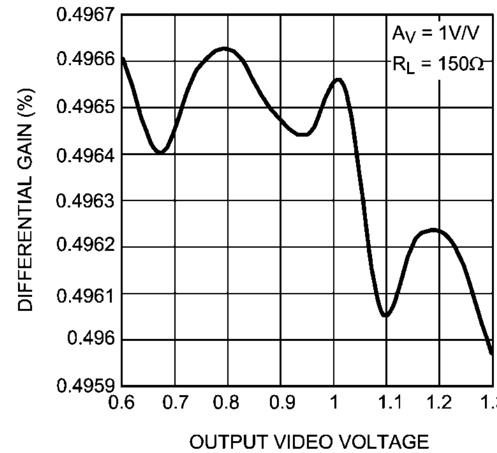
0.6 black level to 1.3 white Level

Differential Gain



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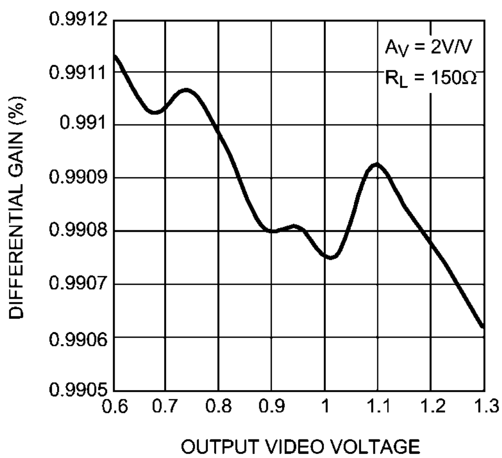
0.6 black level to 1.3 white Level

Differential Gain



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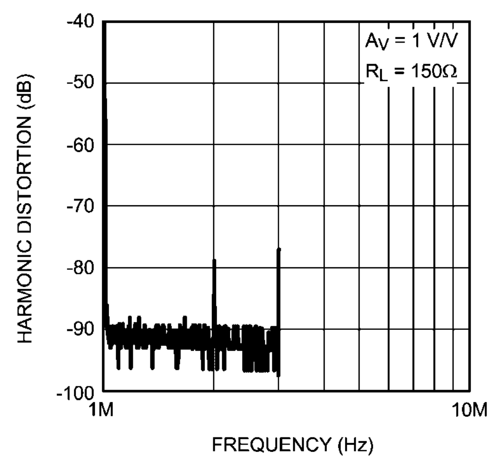
0.6 black level to 1.3 white Level

Harmonic Distortion



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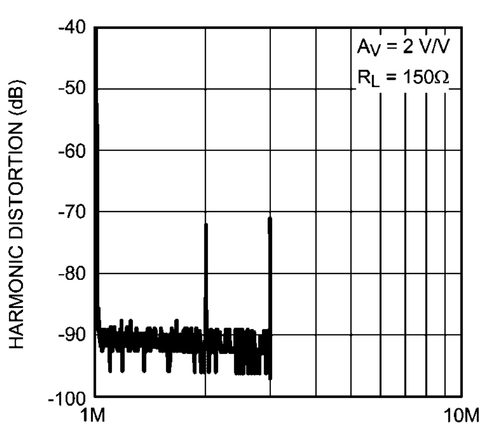
Harmonic Distortion



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Note: Large Signal Input Voltage = 750 mV
Medium Signal Input Voltage = 200 mV
Small Signal Input voltage = 20 mV

Application Information

FUNCTIONAL OVERVIEW

The LMH6586 is a 32 input 16 output analog video Crosspoint switch. Each input and each output is fully buffered. The output buffers can be programmed to provide 1X or 2X gain. Each input and each output can be placed in power save mode individually using the input and output power save register respectively. The Flag pin (pin 75) is used for video detection and sync detection. The LMH6586 has an additional 17th output which has only a 1X gain output buffer which can be sent to an external sync separator.

OUTPUT BUFFER GAIN

The LMH6586 has an output buffer with a selectable gain of 1X or 2X. When the GAIN SELECT pin (pin 61) is set to logic LOW, output channels 0 -15 will have a gain of 1X, and when it is set to logic HIGH, they will have a gain of 2X. Output channel 16 has only a 1X gain buffer. This channel output can be optionally sent to an external sync separator through a 0.1 μF capacitor.

VIDEO DETECTION

The LMH6586 features a video detection circuit that can detect the presence of video relative to the absence of video or the loss of video relative to the presence of video. The detection threshold level can be set with a 3-bit programmable register. Video detection may be implemented in an application where there is low level or black level video at steady state, and when there is a change in video level detected by the LMH6586, a video recorder is triggered to begin recording. In other implementations, the loss of video may be useful to detect.

Each of the 32 video input channels can be configured individually to detect video or the loss of video. Registers 0x0C to 0x0F are used for setting these configurations, where the register bit for the input channel is set to a logic LOW if loss of video detection is desired or set to a logic HIGH if presence of video detection is desired. The 3 least significant bits in register, 0x1D, are used to set the detection threshold level in 95 mV increments above the sync tip. Registers 0x04 to 0x07 are read-only registers, whose bits output a logic HIGH to indicate that video or the loss of video has been detected on each video input channel.

TABLE 1. Video Detect Reference Voltage

0x1D [2:0]			Threshold level above the sync tip*
0	0	0	491 mV
0	0	1	587 mV
0	1	0	683 mV
0	1	1	778 mV
1	0	0	873 mV
1	0	1	968 mV
1	1	0	1062 mV
1	1	1	1156 mV

* See Electrical Characteristics – DC Specifications

SYNC DETECTION

The LMH6586 also features a sync detection circuit that can detect the loss of sync relative to the presence of sync. An external voltage control (pin 65, SSR) is used to set the desired threshold level using a resistor divider network. For correct operation the recommended voltage level at the SSR pin is 0.35V.

INPUT DETECT FLAG

Pin 75 is an output flag pin whose level will be a logic HIGH, if either video detection or sync detection is triggered based on the user-defined video and sync detection configurations and threshold levels (0x1D). The outputs of both the video detection and sync detection blocks of all 32 input channels can be OR'd into this single output flag pin. Registers 0x10 to 0x13 are used to enable or disable the Input Detect Flag feature for video detect, where the register bit for the input channel is set to a logic LOW if the feature is to be disabled, or HIGH if it is to enabled. Similarly, registers 0x14 to 0x17 are used for sync detect. Therefore, the flag will only operate for the channel(s) and type(s) of detection that are specifically enabled. The typical flag switching time is 300 ms.

SWITCH MATRIX

The LMH6586 has 512 CMOS analog switches, forming a 32x16 crosspoint switch. The LMH6586 is a non-blocking Crosspoint switch which means that any one of the 32 inputs can be routed to any of the 16 outputs. The programming is done using an I^2C interface bus.

DC RESTORATION

The LMH6586 is used only in AC coupled mode using a coupling capacitor of 0.1 μF. Please refer to the following section for details on how to select a coupling capacitor. Since the composite video signal swings in the positive direction from 0V to 700 mV and in the negative direction from 0V to –300 mV some level shifting is typically required in a single supply device such as the LMH6586. The LMH6586 offers an integrated DC restore circuit to enable AC coupled operation.

For video signals without sync tips the LMH6586 cannot be used. For correct operation the REF_CAP1 pin (pin 21) should be connected to ground through a 0.1 μF capacitor.

AC COUPLING

The LMH6586 offers an integrated DC restoration clamp circuit, which is used to clamp the sync tip of the input video signal to the V_CLAMP level during AC coupled operation. For this operation, the CLAMP ENABLE (pin 21) must be set to logic HIGH. For AC-coupled operation, the LMH6586 requires video signals with sync tips.

When AC-coupling, the LMH6586 will restore the DC level by clamping the sync tip of the input video signal to the V_CLAMP level, which is adjustable within the range of 0.3V to 1V at pin 66 via an external voltage. For optimum performance and minimized power consumption, V_CLAMP is recommended to be set at 300 mV. Therefore, the bottom of the sync tip will be clamped to 300 mV above ground, and the peak white video level would be at 1.3V.

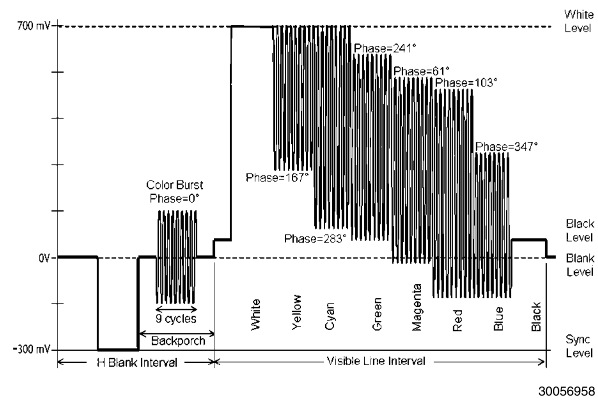


FIGURE 3. Input Video Signal Before DC Restore Clamp

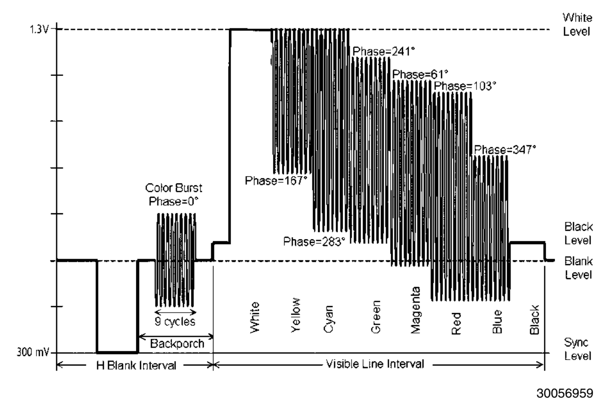


FIGURE 4. Input Video Signal After DC Restore Clamp

The equivalent DC restore clamp circuit is shown below.

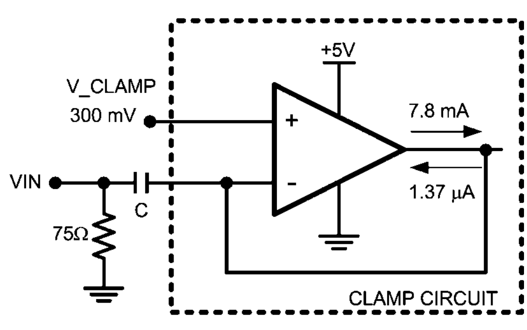


FIGURE 5. Clamp Circuit

Typically the clamp voltage is set to 300 mV. Thus during the sync timing the clamp circuit amplifier sources current and the coupling capacitor will not discharge. However, during the active video amplifier will sink current and cause the coupling capacitor to discharge through the 75Ω resistor. To limit this discharge to an acceptable value we must choose an appropriate value of the coupling capacitor. The value of the DC coupling capacitor for each input is calculated as follows:

Cap Discharge Time T = Line Period – Sync Timing
T = 63.5 µs – 4.7 µs
T= 58.8 µs

Discharge current I = 1.37 µA
Charge Q = I*T
Q = 1.37 µA * 58.8 µs
Q = 80.55 pC

Q = C*V
C = Q/V
Typical acceptable voltage drop V = 0.1% of 700 mV
V = 0.7 mV

Capacitor Value C = 80.55 pC/ 0.7 mV
C = 0.115 µF
Thus the suggested AC coupling capacitor value is 0.1 µF.

VIDEO INPUTS AND OUTPUTS

The LMH6586 has 32 inputs which accept standard composite video signals (NTSC and PAL). Each input is buffered before the switch matrix. Each input can be routed to all 16 outputs at a time. Each input can be individually placed in power save mode by shutting down the respective input amplifier using the input power save registers. The inputs of the LMH6586 are high impedance. The LMH6586 works only in AC coupled mode thus each video input needs to be connected to a 0.1 µF coupling capacitor for proper operation.

The LMH6586 has 16 video outputs each of which is buffered through a programmable 1X or 2X gain output buffer. The outputs are capable of driving 150Ω loads. The output signal sync tip is set to 300 mV for a gain of 1X or 600 mV for a gain of 2X (It is basically set to the V_CLAMP voltage level) Each output can be individually placed in power save mode by shutting down the respective output amplifier using the output power save registers. When disabled the outputs are high impedance, thus enabling multiple outputs to be connected together for expanding the Crosspoint matrix. Output short circuit protection is not provided.

INPUT EXPANSION

The LMH6586 has the capability for creating larger switching matrices. Depending on the number of input and output channels required, the number of IC's required can be calculated. To implement 128 X 16 non-blocking matrix arrange the building blocks in a grid. The inputs are connected in parallel while the outputs are wired-or together. When using this configuration care must be taken to ensure that only one of the four outputs is active. The other three outputs should be placed in power save mode by using the appropriate power save bit in the power save registers. By doing so the loading effects from the disabled outputs are minimized.

The figure below shows the 128 input X 16 output switching matrix using 4 LMH6586's. To construct larger matrices use the same technique with more devices.

Since the LMH6586 is two bit addressable up to 4 LMH6586's can be connected to a common I^{2}C bus. For more devices additional I^{2}C buses will be required.

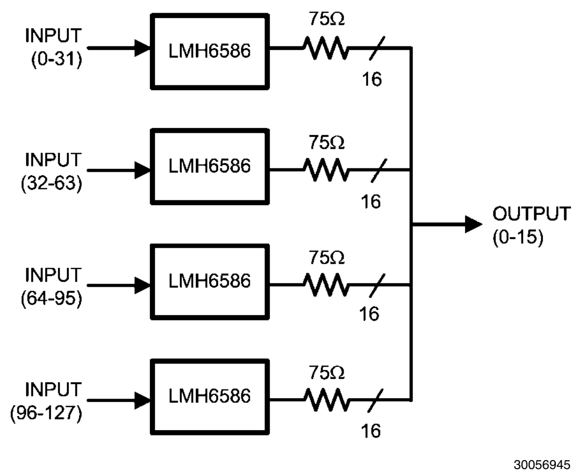


FIGURE 6. 128 x 16 Crosspoint Array

DRIVING CAPACITIVE LOAD

When many outputs are wired together as in the case of expansion each output buffer sees the normal load impedance and the disabled impedance of all the other outputs. This impedance has a resistive and a capacitive component. The resistive components reduce the total effective load for the driving output. Total capacitance is the sum of the capacitance of all the outputs and depends on the size of the matrix. As the size of the matrix increases, the length of the PC board traces also increases, adding more capacitance. The output buffers have been designed to drive more than 30 pF of capacitance while still maintaining a good AC response. If the output capacitance exceeds this amount then the AC response will be degraded. To prevent this, one option is to reduce the number of output wired-or together by using more LMH6586's. The other option is to put a resistor in series with the output before the capacitive load to limit excessive ringing and oscillations.

A low pass filter is created from the series resistor and parasitic capacitance to ground. A single R-C does not affect the performance at video frequencies, however, in large system, there may be many such R-Cs cascaded in series. This may result in high frequency roll off resulting in "softening of the picture". There are two solutions to improve performance in this case. One way is to design the PC board traces with some inductance. By routing the traces in a repeating "S" configuration, the traces that are nearest each other will exhibit a mutual inductance increasing the total inductance. This series inductance causes the amplitude response to increase or peak at higher frequencies, offsetting the roll off from the parasitic capacitance. Another solution is to add a small-value inductor to the output.

THERMAL MANAGEMENT

The LMH6586 operates on a +5V supply and draws a load current of approximately 300 mA. Thus it dissipates approximately 1.75W of power. In addition, each equivalent video load (150Ω) connected to the outputs should be budgeted 30 mW of power.

The following calculations show the thermal resistance, θ_{JA}, required, to ensure safe operation and to prevent exceeding the maximum junction temperature, given the maximum power dissipation.

$$P_{DMAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$$

Where:

- T_{JMAX} = Maximum junction temperature = 150°C
- T_{AMAX} = Maximum ambient temperature = +85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$P_{DMAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 300 mA
- V_{OUT} = Maximum output voltage of the application = 2.6V
- R_L = Load resistance tied to ground = 150Ω
- n = 1 to 16 channels

Calculating :

P_{DMAX} = 2.2656

The required θ_{JA} to dissipate P_{DMAX} is = $(T_{JMAX} - T_{AMAX})/P_{DMAX}$

The table below shows the θ_{JA} values with airflow and different heatsinks.

LMH6586VS 80-Pin TQFT LMHXPT Analog Video Crosspoint Board	0 LFPM @ 0.50 watt	0 LFPM @ 1.0watt	0 LFPM @ 2.0 watt	0 LFPM @ 0.2.8 watt	225 LFPM @ 2.8 watt	500 LFPM @ 2.8 watt
NO Heat Sink	32.2	30.9	29.4	28.6	26.8	25.3
Small Tower x y = 9.57x9.69 mm/ht. 6.28 mm	25.5	24.6	23.6	22.9	19.2	15.9
Aluminum 12 rail x y = 9.82x10.73 mm/ht.10.07 mm	25.2	24.1	23.0	22.2	16.4	14.2
Anodized 9 rail x y = 6.10x7.30 mm/ht. 13.67 mm	24.4	23.3	22.1	21.3	15.6	13.6
Round Tower diameter = 14.35 mm/ht. 4.47 mm	24.2	23.9	22.9	22.4	18.2	15.4

REXT RESISTOR

The REXT external resistor (Pin 67) establishes the internal bias current and precise reference voltage for the LMH6586. For optimal performance, REXT should be a 10 kΩ 1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a REXT resistor with less precision may result in reduced performance against temperature, supply voltage, input signal, or part-to-part variations.

SYNC SEPARATOR OUT (OUT 16)

In addition to the 16 video outputs the LMH6586 has an additional 17th output (OUT16). OUT16 only has a gain of 1 buffer at its output. This video signal output can be AC coupled to an external sync separator such as the LMH1980 to extract the timing information. The value of the coupling capacitor should be 0.1 µF. Refer to the LMH1980 datasheet for more information.

LMH6586 I²C INTERFACE

The microcontroller interfaces to the LMH6586 preamp using the I²C compatible interface. The protocol of the interface begins with a Start Pulse followed by a byte comprised of a 7-bit Slave Device Address and a Read/Write bit. Although the power-up default Slave Device Address of the LMH6586 is 0x00, it can be programmed via pins 70 and 71 to accommodate up to four LMH6586 devices on a common I²C bus. With the default Slave Device Address of "000 0011," the address byte of the LMH6586 for writing is 0x06 and the address for reading is 0x07, since the first byte is composed of both the 7-bit address and the read/write bit. *Figure 7* and *Figure 8* show a write and read sequence on the I²C compatible interface.

WRITE SEQUENCE

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. Assuming that the default Slave Device Address is used, the Write Address, 0x00, is sent next. Each byte that is sent is followed by an acknowledge bit. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The register to be written to is next sent in two bytes, the least significant byte being sent first. The master can then send the data, which consists of one or more bytes. Each data byte is followed by an acknowledge bit. If more than one data byte is sent the data will increment to the next address location. See *Figure 7*.

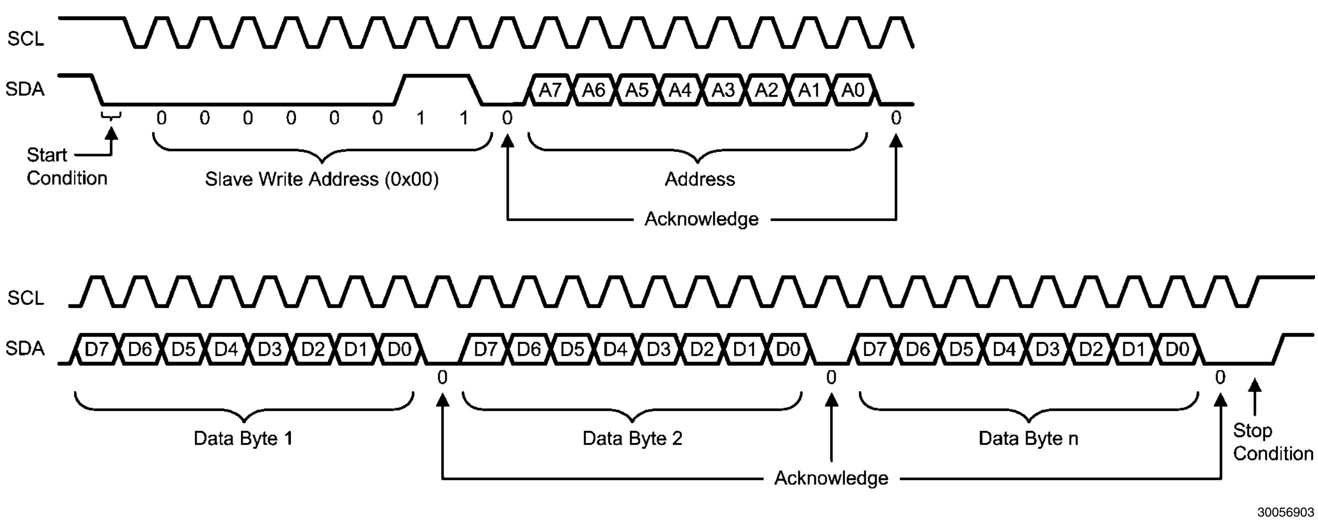


FIGURE 7. I²C Compatible Write Sequence

READ SEQUENCE

Read sequences are comprised of two I²C compatible transfer sequences: The first is a write sequence that only transfers the two byte address to be accessed. The second is a read sequence that starts at the address transferred in the previous address only write access and increments to the next address upon every data byte read. This is shown in *Figure 8*. The write sequence consists of the Start Pulse, the Slave Device Write Address (0x06 for this example), and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access. Next the read data access will be performed beginning with the Start Pulse, the Slave Device Read Address (0x07), and the Acknowledge bit. The next 8 bits will be the read data driven out by the LMH6586 preamp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations. Each data byte is separated from the other data bytes by an Acknowledge bit.

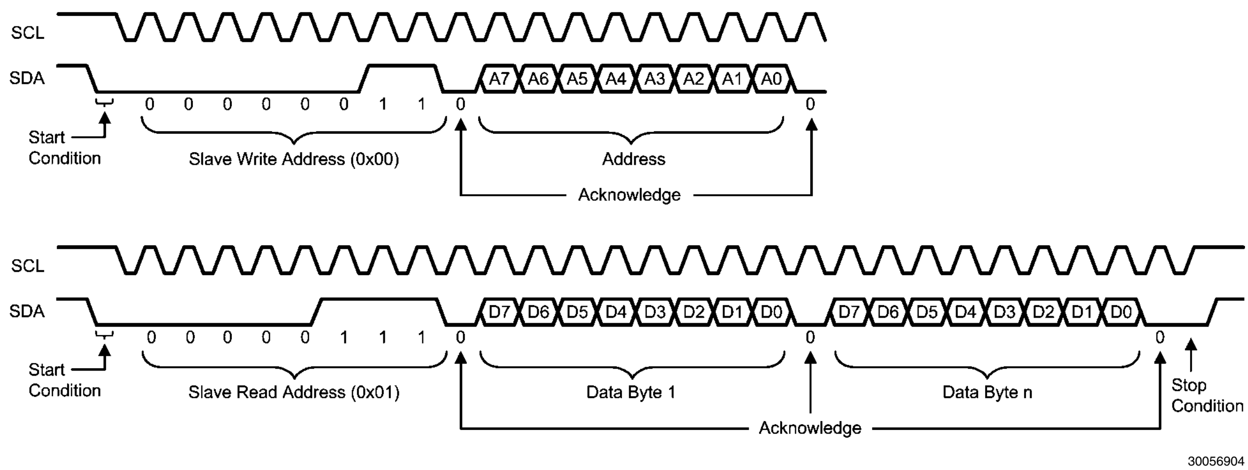


FIGURE 8. I²C Compatible Read Sequence

REGISTER DESCRIPTIONS

LMH6586 Video and Sync Detection Output Registers

Registers 0x00 to 0x03 are sync detect out registers and registers 0x04 to 0x07 are video detect out registers. These are read only registers and are used to detect sync and video on each input. In the presence of sync or video, the respective bit corresponding to each input in each register is 0. In the absence of sync or video, that bit is 1. Thus these registers can be used to detect the presence or loss of sync and video.

LMH6586 Video & Sync Detection Control Registers

Video Detect Invert Registers:

Registers 0X0C to 0X0 Fare video detect invert registers. These registers are used to set the LMH6586 to either detect the presence of video or the loss of video. If the respective bits for each input are set to 1 then the LMH6586 detects the presence of video on that input and if the bit is set to 0 then the LMH6586 detects the loss of video on that input.

Video/Sync Detect Enable Registers:

Registers 0x10 to 0x13 are sync detect enable registers and registers 0x14 to 0x17 are video detect enable registers. To enable video or sync detect for any input, the enable bit corresponding to that input in the enable registers should be set to 1. On setting the appropriate values for the video detect invert and video and sync detect enable registers the FLAG pin (pin 75) of the LMH6586 will function as described above.

Video Detect Threshold Level Register

The video detect threshold level is set by programming the appropriate value in register 0x1Ch. Table 1 shows the voltages for the different levels.

Video Shutdown/Power save Registers

Each input channel and each output channel can be independently placed in shutdown or power save mode. Registers 0x18 to 0x1B are the input power save registers and registers 0x1E and 0x1F are the output power save registers. To place any channel in power save mode the respective bit in the corresponding to that channel is set to 1. To put the whole chip in power save mode, the power save enable pin (Pin 70) should be asserted high.

Video Input Selection Registers

The registers 0x20 to 0x30 are used to control the routing of the LMH6586 crosspoint switch. Each register is used to program the routing for the corresponding output channels.

LMH6586 REGISTER MAP

TABLE 2. Video & Sync Detection Output Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC DETECT OUT (CH 0-7)	0x00h	R		SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
SYNC DETECT OUT (CH 8-15)	0x01h	R		SD_15	SD_14	SD_13	SD_12	SD_11	SD_10	SD_9	SD_8
SYNC DETECT OUT (CH 16-23)	0x02h	R		SD_23	SD_22	SD_21	SD_20	SD_19	SD_18	SD_17	SD_16
SYNC DETECT OUT (CH 24-31)	0x03h	R		SD_31	SD_30	SD_29	SD_28	SD_27	SD_26	SD_24	SD_24
VIDEO DETECT OUT (CH 0-7)	0x04h	R		VD_7	VD_6	VD_5	VD_4	VD_3	VD_2	VD_1	VD_0
VIDEO DETECT OUT (CH 8-15)	0x05h	R		VD_15	VD_14	VD_13	VD_12	VD_11	VD_10	VD_9	VD_8
VIDEO DETECT OUT (CH 16-23)	0x06h	R		VD_23	VD_22	VD_21	VD_20	VD_19	VD_18	VD_17	VD_16
VIDEO DETECT OUT (CH 24-31)	0x07h	R		VD_31	VD_30	VD_29	VD_28	VD_27	VD_26	VD_24	VD_24

TABLE 3. LMH6586 Video & Sync Detection Control Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	0x08h 0x0Bh	R/W	0x00	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
VIDEO DETECT INVERT (CH 0-7)	0x0Ch	R/W	0x00	VD_INV_7	VD_INV_6	VD_INV_5	VD_INV_4	VD_INV_3	VD_INV_2	VD_INV_1	VD_INV_0
VIDEO DETECT INVERT (CH 8-15)	0x0Dh	R/W	0x00	VD_INV_15	VD_INV_14	VD_INV_13	VD_INV_12	VD_INV_11	VD_INV_10	VD_INV_9	VD_INV_8
VIDEO DETECT INVERT (CH 16-23)	0x0Eh	R/W	0x00	VD_INV_23	VD_INV_22	VD_INV_21	VD_INV_20	VD_INV_19	VD_INV_18	VD_INV_17	VD_INV_16
VIDEO DETECT INVERT (CH 24-31)	0x0Fh	R/W	0x00	VD_INV_31	VD_INV_30	VD_INV_29	VD_INV_28	VD_INV_27	VD_INV_26	VD_INV_24	VD_INV_24
SYNC DETECT ENABLE (CH 0-7)	0x10h	R/W	0x00	SD_EN_7	SD_EN_6	SD_EN_5	SD_EN_4	SD_EN_3	SD_EN_2	SD_EN_1	SD_EN_0
SYNC DETECT ENABLE (CH 8-15)	0x11h	R/W	0x00	SD_EN_15	SD_EN_14	SD_EN_13	SD_EN_12	SD_EN_11	SD_EN_10	SD_EN_9	SD_EN_8
SYNC DETECT ENABLE (CH 16-23)	0x12h	R/W	0x00	SD_EN_23	SD_EN_22	SD_EN_21	SD_EN_20	SD_EN_19	SD_EN_18	SD_EN_17	SD_EN_16
SYNC DETECT ENABLE (CH 24-31)	0x13h	R/W	0x00	SD_EN_31	SD_EN_30	SD_EN_29	SD_EN_28	SD_EN_27	SD_EN_26	SD_EN_25	SD_EN_24
VIDEO DETECT ENABLE (CH 0-7)	0x14h	R/W	0x00	VD_EN_7	VD_EN_6	VD_EN_5	VD_EN_4	VD_EN_3	VD_EN_2	VD_EN_1	VD_EN_0
VIDEO DETECT ENABLE (CH 8-15)	0x15h	R/W	0x00	VD_EN_15	VD_EN_14	VD_EN_13	VD_EN_12	VD_EN_11	VD_EN_10	VD_EN_9	VD_EN_8

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VIDEO DETECT ENABLE (CH 16-23)	0x16h	R/W	0x00	VD_ EN_23	VD_ EN_22	VD_ EN_21	VD_ EN_20	VD_ EN_19	VD_ EN_18	VD_ EN_17	VD_ EN_16
VIDEO DETECT ENABLE (CH 24-31)	0x17h	R/W	0x00	VD_ EN_31	VD_ EN_30	VD_ EN_29	VD_ EN_28	VD_ EN_27	VD_ EN_26	VD_ EN_25	SD_ EN_24

TABLE 4. LMH6586 Video & Sync Detection Level Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VIDEO DETECTION THRESHOLD	0x1Dh	R/W	0x00	RSV					VDT_2	VDT_1	VDT_0

TABLE 5. LMH6586 Video Shutdown/Power Save Registers

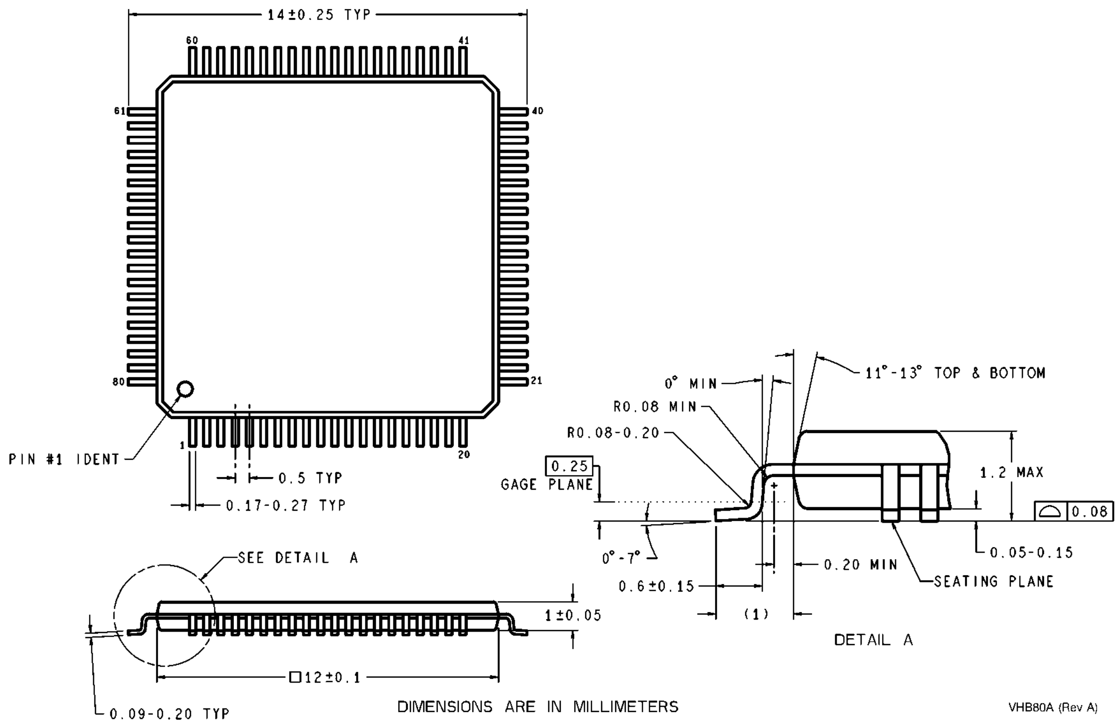
Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INPUT SHUTDOWN (CH 0-7)	0x18h	R/W	0x00	IN_ PS_7	IN_ PS_6	IN_ PS_5	IN_ PS_4	IN_ PS_3	IN_ PS_2	IN_ PS_1	IN_ PS_0
INPUT SHUTDOWN (CH 8-15)	0x19h	R/W	0x00	IN_ PS_15	IN_ PS_14	IN_ PS_13	IN_ PS_12	IN_ PS_11	IN_ PS_10	IN_ PS_9	IN_ PS_8
INPUT SHUTDOWN (CH 16-23)	0x1Ah	R/W	0x00	IN_ PS_23	IN_ PS_22	IN_ PS_21	IN_ PS_20	IN_ PS_19	IN_ PS_18	IN_ PS_17	IN_ PS_16
INPUT SHUTDOWN (CH 24-31)	0x1Bh	R/W	0x00	IN_ PS_31	IN_ PS_30	IN_ PS_29	IN_ PS_28	IN_ PS_27	IN_ PS_26	IN_ PS_25	IN_ PS_24
OUTPUT SHUTDOWN (CH 0-7)	0x1Eh	R/W	0x00	OUT_ PS_7	OUT_ PS_6	OUT_ PS_5	OUT_ PS_4	OUT_ PS_3	OUT_ PS_2	OUT_ PS_1	OUT_ PS_0
OUTPUT SHUTDOWN (CH 8-15)	0x1Fh	R/W	0x00	OUT_ PS_15	OUT_ PS_14	OUT_ PS_13	OUT_ PS_12	OUT_ PS_11	OUT_ PS_10	OUT_ PS_9	OUT_ PS_8

TABLE 6. LMH6586 Video Input Selection Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH 0 OUTPUT	0x20h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 1 OUTPUT	0x21h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 2 OUTPUT	0x22h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 3 OUTPUT	0x23h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 4 OUTPUT	0x24h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 5 OUTPUT	0x25h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 6 OUTPUT	0x26h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 7 OUTPUT	0x27h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 8 OUTPUT	0x28h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 9 OUTPUT	0x29h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 10 OUTPUT	0x2Ah	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 11 OUTPUT	0x2Bh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 12 OUTPUT	0x2Ch	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 13 OUTPUT	0x2Dh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 14 OUTPUT	0x2Eh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 15 OUTPUT	0x2Fh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 16 OUTPUT (FOR SYNC SEP)	0x30h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				

Note: At initial power-up, all 17 outputs are driven by input channel 0.

Physical Dimensions inches (millimeters) unless otherwise noted



80-Pin TQFP
NS Package Number VHB80A

Notes

Notes

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