

LMH6618 Single/LMH6619 Dual 130 MHz, 1.25 mA RRIO Operational Amplifiers

General Description

The LMH6618 (single, with shutdown) and LMH6619 (dual) are 130 MHz rail-to-rail input and output amplifiers designed for ease of use in a wide range of applications requiring high speed, low supply current, low noise, and the ability to drive complex ADC and video loads. The operating voltage range extends from 2.7V to 11V and the supply current is typically 1.25 mA per channel at 5V. The LMH6618 and LMH6619 are members of the PowerWise® family and have an exceptional power-to-performance ratio.

The amplifier's voltage feedback design topology provides balanced inputs and high open loop gain for ease of use and accuracy in applications such as active filter design. Offset voltage is typically 0.1 mV and settling time to 0.01% is 120 ns which combined with an 100 dBc SFDR at 100 kHz makes the part suitable for use as an input buffer for popular 8-bit, 10-bit, 12-bit and 14-bit mega-sample ADCs.

The input common mode range extends 200 mV beyond the supply rails. On a single 5V supply with a ground terminated 150Ω load the output swings to within 37 mV of the ground rail, while a mid-rail terminated 1 kΩ load will swing to 77 mV of either rail, providing true single supply operation and maximum signal dynamic range on low power rails. The amplifier output will source and sink 35 mA and drive up to 30 pF loads without the need for external compensation.

The LMH6618 has an active low disable pin which reduces the supply current to 72 μA and is offered in the space saving 6-Pin TSOT23 package. The LMH6619 is offered in the 8-Pin SOIC package. The LMH6618 and LMH6619 are available with a -40°C to +125°C extended industrial temperature grade.

Features

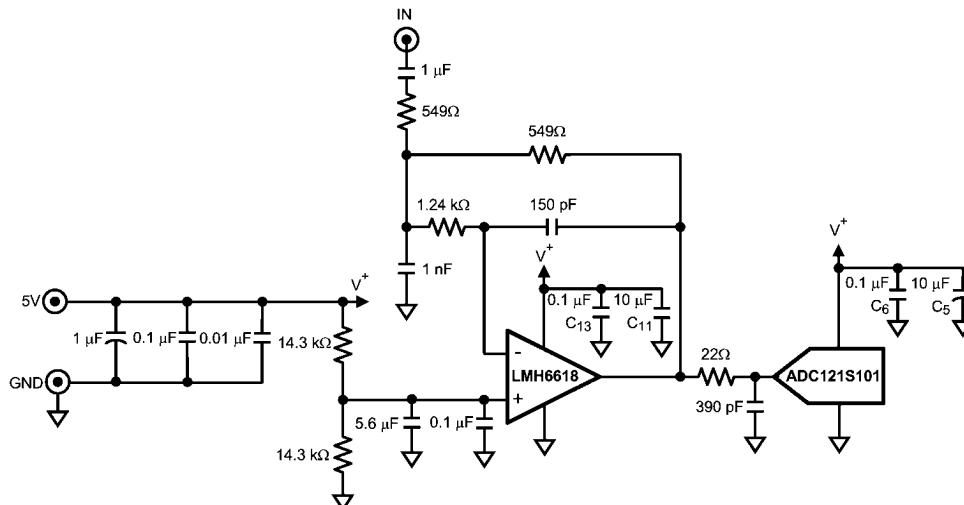
$V_S = 5V$, $R_L = 1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ and $A_V = +1$, unless otherwise specified.

- | | |
|---|-----------------|
| ■ Operating voltage range | 2.7V to 11V |
| ■ Supply current per channel | 1.25 mA |
| ■ Small signal bandwidth | 130 MHz |
| ■ Slew rate | 55 V/μs |
| ■ Settling time to 0.1% | 90 ns |
| ■ Settling time to 0.01% | 120 ns |
| ■ SFDR ($f = 100\text{ kHz}$, $A_V = +1$, $V_{OUT} = 2 V_{PP}$) | 100 dBc |
| ■ 0.1 dB bandwidth ($A_V = +2$) | 15 MHz |
| ■ Low voltage noise | 10 nV/√Hz |
| ■ Industrial temperature grade | -40°C to +125°C |
| ■ Rail-to-Rail input and output | |

Applications

- ADC driver
- DAC buffer
- Active filters
- High speed sensor amplifier
- Current sense amplifier
- Portable video
- STB, TV video amplifier

Typical Application



20195829

WEBENCH® is a registered trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)

Human Body Model

For input pins only

2000V

For all other pins

2000V

Machine Model

200V

Supply Voltage ($V_S = V^+ - V^-$)

12V

Junction Temperature (Note 3)

150°C max

Operating Ratings (Note 1)Supply Voltage ($V_S = V^+ - V^-$)

2.7V to 11V

Ambient Temperature Range (Note 3)

-40°C to +125°C

Package Thermal Resistance (θ_{JA})

6-Pin TSOT23

231°C/W

8-Pin SOIC

160°C/W

+3V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = +25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $\text{DISABLE} = 3\text{V}$, $V_{CM} = V_O = V^+/2$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\text{k}\Omega$ for $A_V \neq +1$, $R_L = 1\text{k}\Omega \parallel 5\text{pF}$.

Boldface Limits apply at temperature extremes. (Note 4)

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Response						
SSBW	-3 dB Bandwidth Small Signal	$A_V = 1$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 0.2 V_{PP}$		120		MHz
		$A_V = 2, -1$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 0.2 V_{PP}$		56		
GBW	Gain Bandwidth (LMH6618)	$A_V = 10$, $R_F = 2\text{k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 0.2 V_{PP}$	55	71		MHz
GBW	Gain Bandwidth (LMH6619)	$A_V = 10$, $R_F = 2\text{k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 0.2 V_{PP}$	55	63		MHz
LSBW	-3 dB Bandwidth Large Signal	$A_V = 1$, $R_L = 1\text{k}\Omega$, $V_{OUT} = 2 V_{PP}$		13		MHz
		$A_V = 2$, $R_L = 150\Omega$, $V_{OUT} = 2 V_{PP}$		13		
Peak	Peaking	$A_V = 1$, $C_L = 5\text{pF}$		1.5		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$, $V_{OUT} = 0.5 V_{PP}$, $R_F = R_G = 825\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$, 4.43 MHz, $0.6\text{V} < V_{OUT} < 2\text{V}$, $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$, 4.43 MHz, $0.6\text{V} < V_{OUT} < 2\text{V}$, $R_L = 150\Omega$ to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, $A_V = 1$		36		ns
SR	Slew Rate	2V Step, $A_V = 1$	36	46		V/ μs
$t_{s,0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s,0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	$f_C = 100\text{kHz}$, $V_{OUT} = 2 V_{PP}$, $R_L = 1\text{k}\Omega$		100		dBc
		$f_C = 1\text{MHz}$, $V_{OUT} = 2 V_{PP}$, $R_L = 1\text{k}\Omega$		61		
		$f_C = 5\text{MHz}$, $V_{OUT} = 2 V_{PP}$, $R_L = 1\text{k}\Omega$		47		
e_n	Input Voltage Noise Density	$f = 100\text{kHz}$		10		nV/ $\sqrt{\text{Hz}}$
i_n	Input Current Noise Density	$f = 100\text{kHz}$		1		pA/ $\sqrt{\text{Hz}}$
CT	Crosstalk (LMH6619)	$f = 5\text{MHz}$, $V_{IN} = 2 V_{PP}$		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	$V_{CM} = 0.5\text{V}$ (pnp active) $V_{CM} = 2.5\text{V}$ (nnp active)		0.1	± 0.6 ± 1.0	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(Note 5)		0.8		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = 0.5\text{V}$ (pnp active)		-1.4	-2.6	μA
		$V_{CM} = 2.5\text{V}$ (nnp active)		+1.0	+1.8	
I_{OS}	Input Offset Current			0.01	± 0.27	μA

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units	
C_{IN}	Input Capacitance			1.5		pF	
R_{IN}	Input Resistance			8		M Ω	
CMVR	Common Mode Voltage Range	DC, CMRR \geq 65 dB	-0.2		3.2	V	
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from -0.1V to 1.4V	78	96		dB	
		V_{CM} Stepped from 2.0V to 3.1V	81	107			
A_{OL}	Open Loop Voltage Gain	$R_L = 1\text{ k}\Omega$ to +2.7V or +0.3V	85	98		dB	
		$R_L = 150\Omega$ to +2.6V or +0.4V	76	82			
Output DC Characteristics							
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to V+/2		50	56 62	mV from either rail	
		$R_L = 150\Omega$ to V+/2		160	172 198		
	Output Voltage Swing Low (LMH6618) (Voltage from V- Supply Rail)	$R_L = 1\text{ k}\Omega$ to V+/2		60	66 74		
		$R_L = 150\Omega$ to V+/2		170	184 217		
		$R_L = 150\Omega$ to V-		29	39 43		
	Output Voltage Swing High (LMH6619) (Voltage from V+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to V+/2		50	56 62		mV from either rail
		$R_L = 150\Omega$ to V+/2		160	172 198		
	Output Voltage Swing Low (LMH6619) (Voltage from V- Supply Rail)	$R_L = 1\text{ k}\Omega$ to V+/2		62	68 76		
		$R_L = 150\Omega$ to V+/2		175	189 222		
		$R_L = 150\Omega$ to V-		34	44 48		
	I_{OUT}	Linear Output Current	$V_{OUT} = V+/2$ (Note 6)	± 25	± 35		
	R_{OUT}	Output Resistance	f = 1 MHz		0.17		Ω
Enable Pin Operation							
	Enable High Voltage Threshold	Enabled	2.0			V	
	Enable Pin High Current	$V_{DISABLE} = 3V$		0.04		μA	
	Enable Low Voltage Threshold	Disabled			1.0	V	
	Enable Pin Low Current	$V_{DISABLE} = 0V$		1		μA	
t_{on}	Turn-On Time			25		ns	
t_{off}	Turn-Off Time			90		ns	
Power Supply Performance							
PSRR	Power Supply Rejection Ratio	DC, $V_{CM} = 0.5V$, $V_S = 2.7V$ to 11V	84	104		dB	
I_S	Supply Current (LMH6618)	$R_L = \infty$		1.2	1.5 1.7	mA	
	Supply Current (LMH6619) (per channel)	$R_L = \infty$		1.2	1.5 1.75		
I_{SD}	Disable Shutdown Current	$\overline{DISABLE} = 0V$		59	85	μA	

+5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_J = +25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $\text{DISABLE} = 5\text{V}$, $V_{\text{CM}} = V_O = V^+/2$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\text{k}\Omega$ for $A_V \neq +1$, $R_L = 1\text{k}\Omega \parallel 5\text{pF}$.

Boldface Limits apply at temperature extremes.

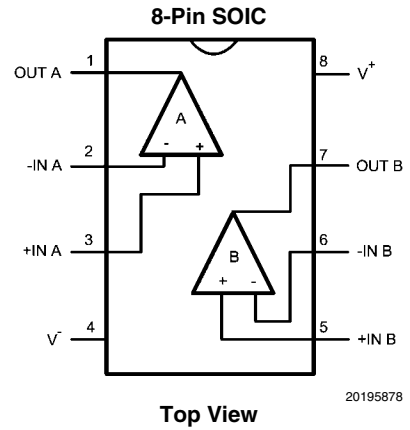
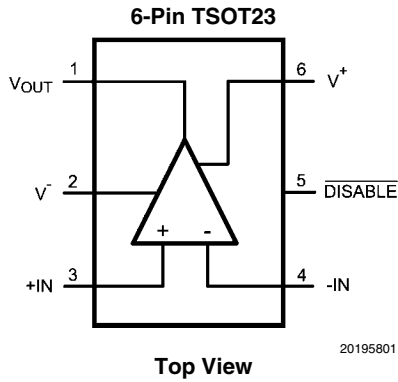
Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Response						
SSBW	-3 dB Bandwidth Small Signal	$A_V = 1$, $R_L = 1\text{k}\Omega$, $V_{\text{OUT}} = 0.2 V_{\text{PP}}$		130		MHz
		$A_V = 2, -1$, $R_L = 1\text{k}\Omega$, $V_{\text{OUT}} = 0.2 V_{\text{PP}}$		53		
GBW	Gain Bandwidth (LMH6618)	$A_V = 10$, $R_F = 2\text{k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{k}\Omega$, $V_{\text{OUT}} = 0.2 V_{\text{PP}}$	54	64		MHz
GBW	Gain Bandwidth (LMH6619)	$A_V = 10$, $R_F = 2\text{k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{k}\Omega$, $V_{\text{OUT}} = 0.2 V_{\text{PP}}$	54	57		MHz
LSBW	-3 dB Bandwidth Large Signal	$A_V = 1$, $R_L = 1\text{k}\Omega$, $V_{\text{OUT}} = 2 V_{\text{PP}}$		15		MHz
		$A_V = 2$, $R_L = 150\Omega$, $V_{\text{OUT}} = 2 V_{\text{PP}}$		15		
Peak	Peaking	$A_V = 1$, $C_L = 5\text{pF}$		0.5		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$, $V_{\text{OUT}} = 0.5 V_{\text{PP}}$, $R_F = R_G = 1\text{k}\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$, 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$, $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$, 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$, $R_L = 150\Omega$ to $V^+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, $A_V = 1$		30		ns
SR	Slew Rate	2V Step, $A_V = 1$	44	55		V/ μs
$t_{s,0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s,0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
Distortion and Noise Performance						
SFDR	Spurious Free Dynamic Range	$f_C = 100\text{kHz}$, $V_{\text{OUT}} = 2 V_{\text{PP}}$, $R_L = 1\text{k}\Omega$		100		dBc
		$f_C = 1\text{MHz}$, $V_{\text{OUT}} = 2 V_{\text{PP}}$, $R_L = 1\text{k}\Omega$		88		
		$f_C = 5\text{MHz}$, $V_O = 2 V_{\text{PP}}$, $R_L = 1\text{k}\Omega$		61		
e_n	Input Voltage Noise Density	$f = 100\text{kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Current Noise Density	$f = 100\text{kHz}$		1		$\text{pA}/\sqrt{\text{Hz}}$
CT	Crosstalk (LMH6619)	$f = 5\text{MHz}$, $V_{\text{IN}} = 2 V_{\text{PP}}$		80		dB
Input, DC Performance						
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = 0.5\text{V}$ (pnp active) $V_{\text{CM}} = 4.5\text{V}$ (nnp active)		0.1	± 0.6 ± 1.0	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(Note 5)		0.8		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{\text{CM}} = 0.5\text{V}$ (pnp active)		-1.5	-2.4	μA
		$V_{\text{CM}} = 4.5\text{V}$ (nnp active)		+1.0	+1.9	
I_{OS}	Input Offset Current			0.01	± 0.26	μA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		$\text{M}\Omega$
CMVR	Common Mode Voltage Range	DC, $\text{CMRR} \geq 65\text{dB}$	-0.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from -0.1V to 3.4V	81	98		dB
		V_{CM} Stepped from 4.0V to 5.1V	84	108		
A_{OL}	Open Loop Voltage Gain	$R_L = 1\text{k}\Omega$ to +4.6V or +0.4V	84	100		dB
		$R_L = 150\Omega$ to +4.5V or +0.5V	78	83		

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Output DC Characteristics						
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V^+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		60	73 82	mV from either rail
		$R_L = 150\Omega$ to $V^+/2$		230	255 295	
	Output Voltage Swing Low (LMH6618) (Voltage from V^- Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		75	83 96	
		$R_L = 150\Omega$ to $V^+/2$		250	270 321	
		$R_L = 150\Omega$ to V^-		32	43 45	
	Output Voltage Swing High (LMH6619) (Voltage from V^+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		60	73 82	
		$R_L = 150\Omega$ to $V^+/2$		230	255 295	
	Output Voltage Swing Low (LMH6619) (Voltage from V^- Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		77	85 98	
		$R_L = 150\Omega$ to $V^+/2$		255	275 326	
$R_L = 150\Omega$ to V^-			37	48 50		
I_{OUT}	Linear Output Current	$V_{OUT} = V^+/2$ (Note 6)	± 25	± 35		mA
R_{OUT}	Output Resistance	$f = 1\text{ MHz}$		0.17		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled	3.0			V
	Enable Pin High Current	$V_{DISABLE} = 5V$		1.2		μA
	Enable Low Voltage Threshold	Disabled			2.0	V
	Enable Pin Low Current	$V_{DISABLE} = 0V$		2.5		μA
t_{on}	Turn-On Time			25		ns
t_{off}	Turn-Off Time			90		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, $V_{CM} = 0.5V$, $V_S = 2.7V$ to $11V$	84	104		dB
I_S	Supply Current (LMH6618)	$R_L = \infty$		1.25	1.5 1.7	mA
	Supply Current (LMH6619) (per channel)	$R_L = \infty$		1.3	1.5 1.75	
I_{SD}	Disable Shutdown Current	$\overline{DISABLE} = 0V$		72	105	μA
<p>$\pm 5V$ Electrical Characteristics Unless otherwise specified, all limits are guaranteed for $T_J = +25^\circ C$, $V^+ = 5V$, $V^- = -5V$, $\overline{DISABLE} = 5V$, $V_{CM} = V_O = 0V$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\text{ k}\Omega$ for $A_V \neq +1$, $R_L = 1\text{ k}\Omega \parallel 5\text{ pF}$. Boldface Limits apply at temperature extremes.</p>						
Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Frequency Domain Response						
SSBW	-3 dB Bandwidth Small Signal	$A_V = 1$, $R_L = 1\text{ k}\Omega$, $V_{OUT} = 0.2 V_{PP}$		140		MHz
		$A_V = 2$, -1 , $R_L = 1\text{ k}\Omega$, $V_{OUT} = 0.2 V_{PP}$		53		
GBW	Gain Bandwidth (LMH6618)	$A_V = 10$, $R_F = 2\text{ k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{ k}\Omega$, $V_{OUT} = 0.2 V_{PP}$	54	65		MHz
GBW	Gain Bandwidth (LMH6619)	$A_V = 10$, $R_F = 2\text{ k}\Omega$, $R_G = 221\Omega$, $R_L = 1\text{ k}\Omega$, $V_{OUT} = 0.2 V_{PP}$	54	58		MHz

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
LSBW	-3 dB Bandwidth Large Signal	$A_V = 1, R_L = 1 \text{ k}\Omega, V_{OUT} = 2 V_{PP}$		16		MHz
		$A_V = 2, R_L = 150\Omega, V_{OUT} = 2 V_{PP}$		15		
Peak	Peaking	$A_V = 1, C_L = 5 \text{ pF}$		0.05		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2, V_{OUT} = 0.5 V_{PP},$ $R_F = R_G = 1.21 \text{ k}\Omega$		15		MHz
DG	Differential Gain	$A_V = +2, 4.43 \text{ MHz}, 0.6V < V_{OUT} < 2V,$ $R_L = 150\Omega \text{ to } V+/2$		0.1		%
DP	Differential Phase	$A_V = +2, 4.43 \text{ MHz}, 0.6V < V_{OUT} < 2V,$ $R_L = 150\Omega \text{ to } V+/2$		0.1		deg
Time Domain Response						
t_r/t_f	Rise & Fall Time	2V Step, $A_V = 1$		30		ns
SR	Slew Rate	2V Step, $A_V = 1$	45	57		V/ μ s
$t_{s,0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s,0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
Noise and Distortion Performance						
SFDR	Spurious Free Dynamic Range	$f_C = 100 \text{ kHz}, V_{OUT} = 2 V_{PP}, R_L = 1 \text{ k}\Omega$		100		dBc
		$f_C = 1 \text{ MHz}, V_{OUT} = 2 V_{PP}, R_L = 1 \text{ k}\Omega$		88		
		$f_C = 5 \text{ MHz}, V_{OUT} = 2 V_{PP}, R_L = 1 \text{ k}\Omega$		70		
e_n	Input Voltage Noise Density	$f = 100 \text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Current Noise Density	$f = 100 \text{ kHz}$		1		$\text{pA}/\sqrt{\text{Hz}}$
CT	Crosstalk (LMH6619)	$f = 5 \text{ MHz}, V_{IN} = 2 V_{PP}$		80		dB
Input DC Performance						
V_{OS}	Input Offset Voltage	$V_{CM} = -4.5V$ (pnp active) $V_{CM} = 4.5V$ (nnp active)		0.1	± 0.6 ± 1.0	mV
TCV_{OS}	Input Offset Voltage Temperature Drift	(Note 5)		0.9		$\mu\text{V}/^\circ\text{C}$
I_B	Input Bias Current	$V_{CM} = -4.5V$ (pnp active)		-1.5	-2.4	μA
		$V_{CM} = 4.5V$ (nnp active)		+1.0	+1.9	
I_{OS}	Input Offset Current			0.01	± 0.26	μA
C_{IN}	Input Capacitance			1.5		pF
R_{IN}	Input Resistance			8		M Ω
CMVR	Common Mode Voltage Range	DC, $CMRR \geq 65 \text{ dB}$	-5.2		5.2	V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from -5.1V to 3.4V	84	100		dB
		V_{CM} Stepped from 4.0V to 5.1V	83	108		
A_{OL}	Open Loop Voltage Gain	$R_L = 1 \text{ k}\Omega \text{ to } +4.6V \text{ or } -4.6V$	86	95		dB
		$R_L = 150\Omega \text{ to } +4.3V \text{ or } -4.3V$	79	84		

Symbol	Parameter	Condition	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Units
Output DC Characteristics						
V_{OUT}	Output Voltage Swing High (LMH6618) (Voltage from V^+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		100	111 126	mV from either rail
		$R_L = 150\Omega$ to GND		430	457 526	
	Output Voltage Swing Low (LMH6618) (Voltage from V^- Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		110	121 136	
		$R_L = 150\Omega$ to GND		440	474 559	
		$R_L = 150\Omega$ to V^-		35	51 52	
	Output Voltage Swing High (LMH6619) (Voltage from V^+ Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		100	111 126	
		$R_L = 150\Omega$ to GND		430	457 526	
	Output Voltage Swing Low (LMH6619) (Voltage from V^- Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		115	126 141	
		$R_L = 150\Omega$ to GND		450	484 569	
$R_L = 150\Omega$ to V^-			45	61 62		
I_{OUT}	Linear Output Current	$V_{OUT} = V^+/2$ (Note 6)	± 25	± 35		mA
R_{OUT}	Output Resistance	$f = 1\text{ MHz}$		0.17		Ω
Enable Pin Operation						
	Enable High Voltage Threshold	Enabled	0.5			V
	Enable Pin High Current	$V_{DISABLE} = +5V$		16		μA
	Enable Low Voltage Threshold	Disabled			-0.5	V
	Enable Pin Low Current	$V_{DISABLE} = -5V$		17		μA
t_{on}	Turn-On Time			25		ns
t_{off}	Turn-Off Time			90		ns
Power Supply Performance						
PSRR	Power Supply Rejection Ratio	DC, $V_{CM} = -4.5V$, $V_S = 2.7V$ to 11V	84	104		dB
I_S	Supply Current (LMH6618)	$R_L = \infty$		1.35	1.6 1.9	mA
	Supply Current (LMH6619) (per channel)	$R_L = \infty$		1.45	1.65 2.0	
I_{SD}	Disable Shutdown Current	$\overline{DISABLE} = -5V$		103	140	μA
<p>Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.</p> <p>Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).</p> <p>Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.</p> <p>Note 4: Boldface limits apply to temperature range of $-40^\circ C$ to $125^\circ C$</p> <p>Note 5: Voltage average drift is determined by dividing the change in V_{OS} by temperature change.</p> <p>Note 6: Do not short circuit the output. Continuous source or sink currents larger than the I_{OUT} typical are not recommended as it may damage the part.</p> <p>Note 7: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.</p> <p>Note 8: Limits are 100% production tested at $25^\circ C$. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.</p>						

Connection Diagrams



Ordering Information

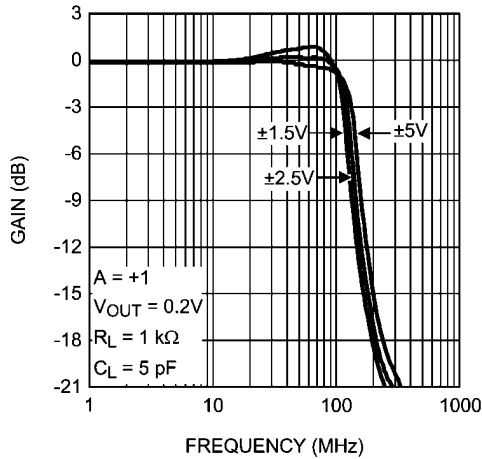
Package	Part Number	Package Marking	Transport Media	NSC Drawing
6-Pin TSOT23	LMH6618MK	AE4A	1k Units Tape and Reel	MK06A
	LMH6618MKE		250 Units Tape and Reel	
	LMH6618MKX		3k Units Tape and Reel	
8-Pin SOIC	LMH6619MA	LMH6619MA	95 Units/Rail	M08A
	LMH6619MAE		250 Units Tape and Reel	
	LMH6619MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

unless otherwise specified.

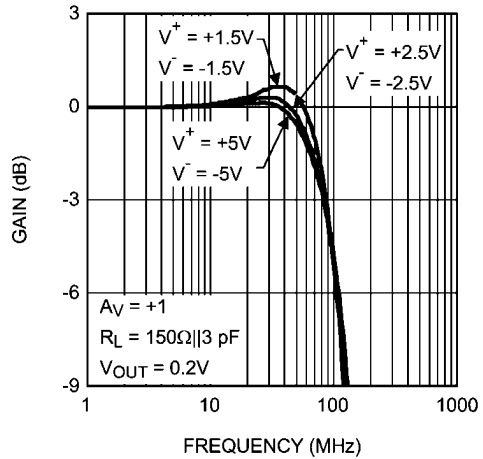
At $T_J = 25^\circ\text{C}$, $A_V = +1$ ($R_F = 0\Omega$), otherwise $R_F = 2\text{ k}\Omega$ for $A_V \neq +1$,

Closed Loop Frequency Response for Various Supplies



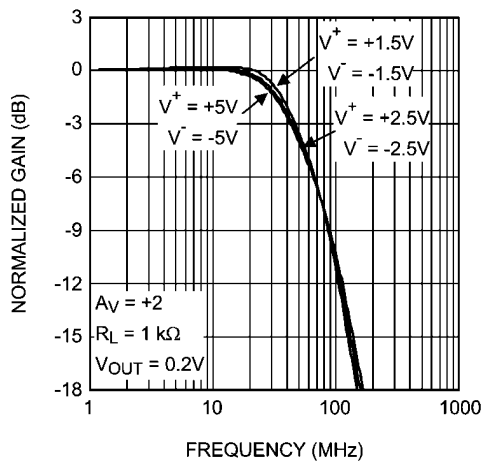
20195831

Closed Loop Frequency Response for Various Supplies



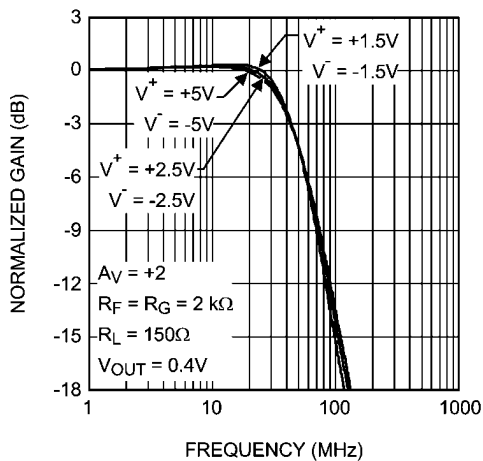
20195816

Closed Loop Frequency Response for Various Supplies



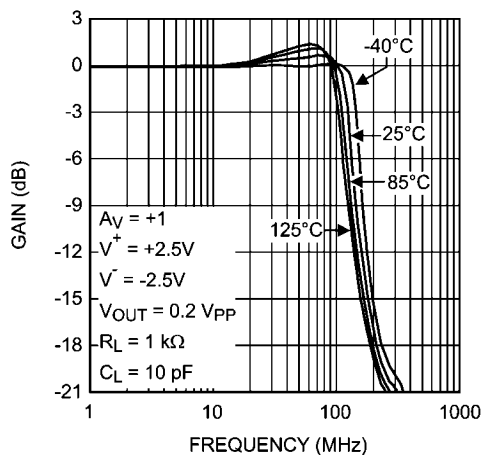
20195815

Closed Loop Frequency Response for Various Supplies



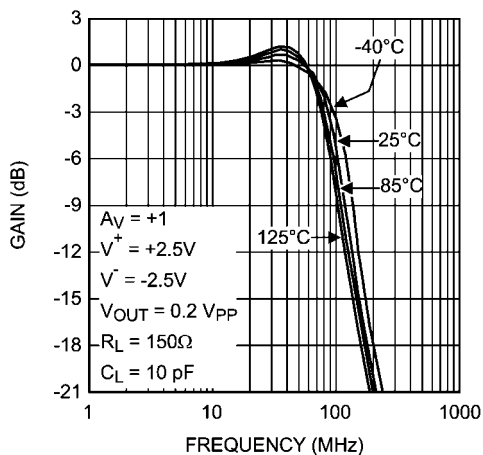
20195817

Closed Loop Frequency Response for Various Temperatures



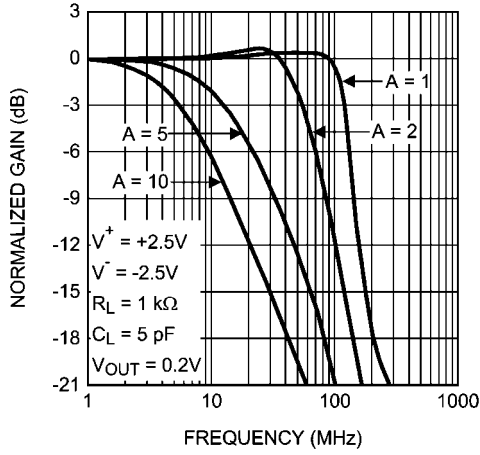
20195819

Closed Loop Frequency Response for Various Temperatures



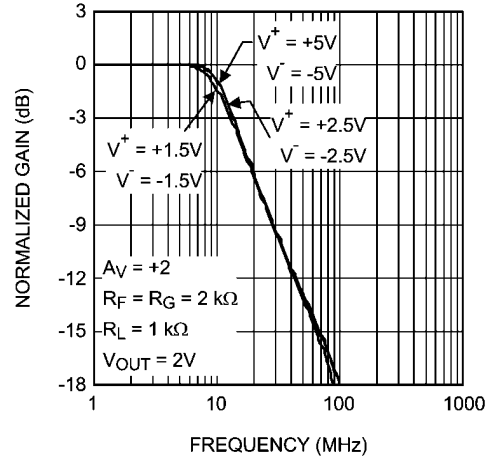
20195820

Closed Loop Gain vs. Frequency for Various Gains



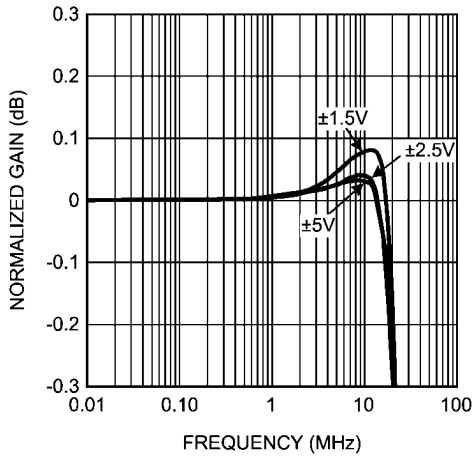
20195830

Large Signal Frequency Response



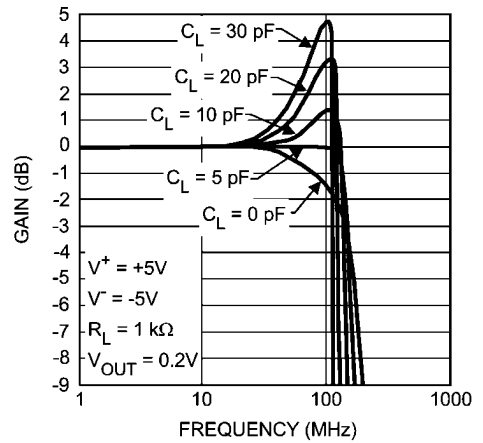
20195818

± 0.1 dB Gain Flatness for Various Supplies



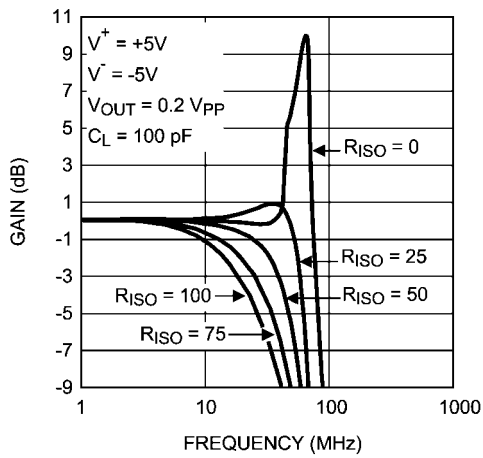
20195832

Small Signal Frequency Response with Various Capacitive Load



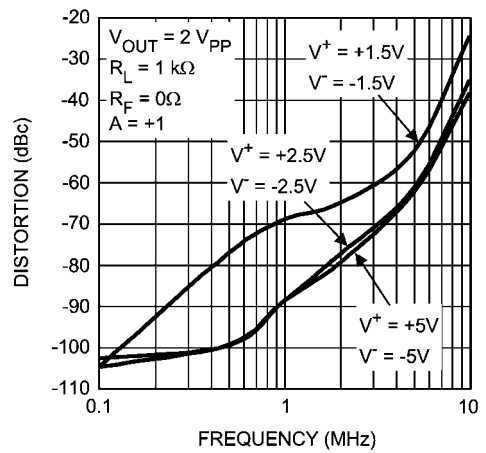
20195826

Small Signal Frequency Response with Capacitive Load and Various R_{ISO}



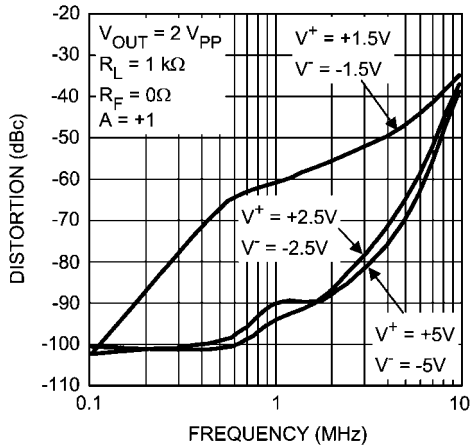
20195827

HD2 vs. Frequency and Supply Voltage



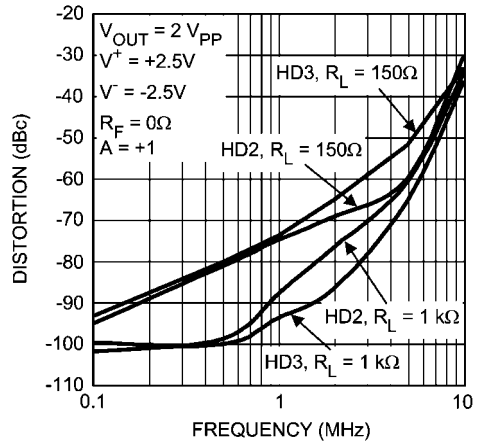
20195835

HD3 vs. Frequency and Supply Voltage



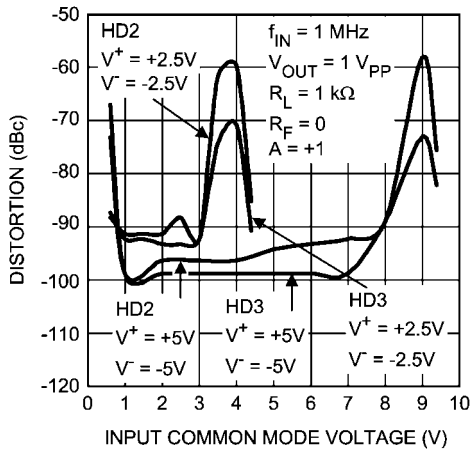
20195836

HD2 and HD3 vs. Frequency and Load



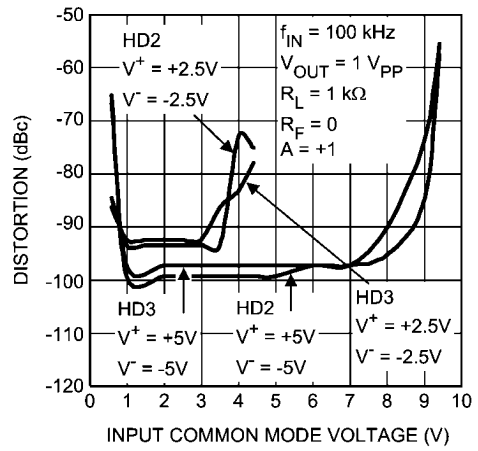
20195871

HD2 and HD3 vs. Common Mode Voltage



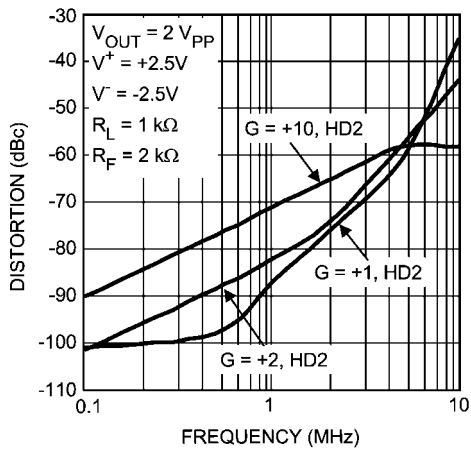
20195872

HD2 and HD3 vs. Common Mode Voltage



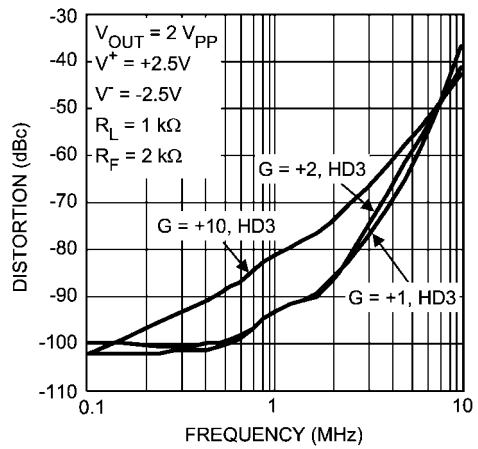
20195873

HD2 vs. Frequency and Gain

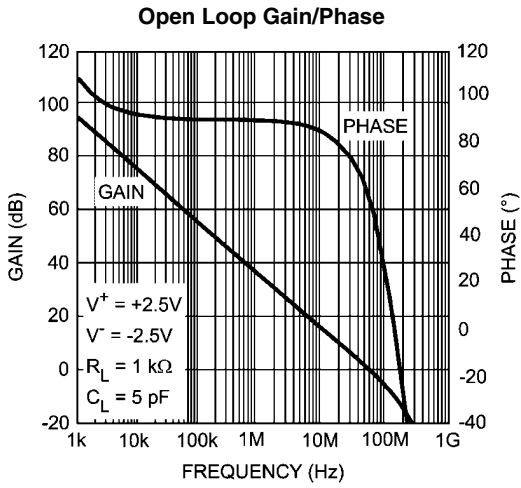


20195874

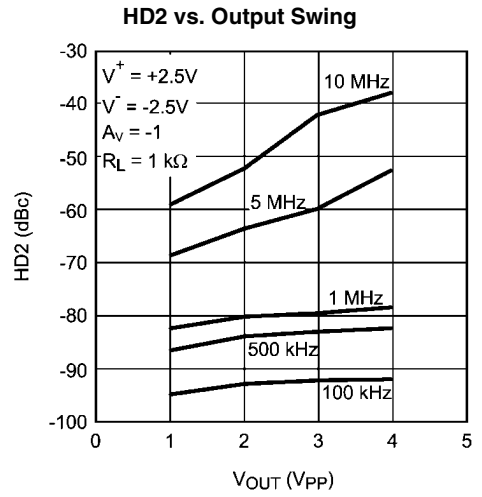
HD3 vs. Frequency and Gain



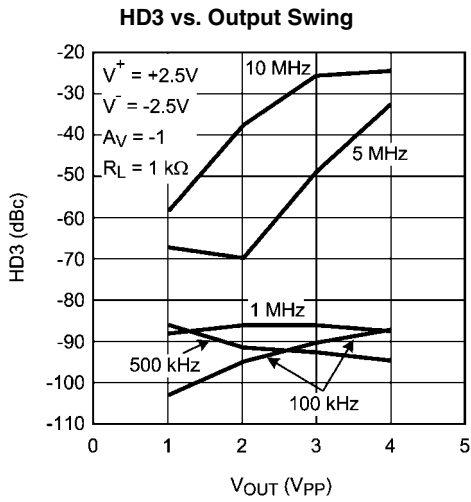
20195875



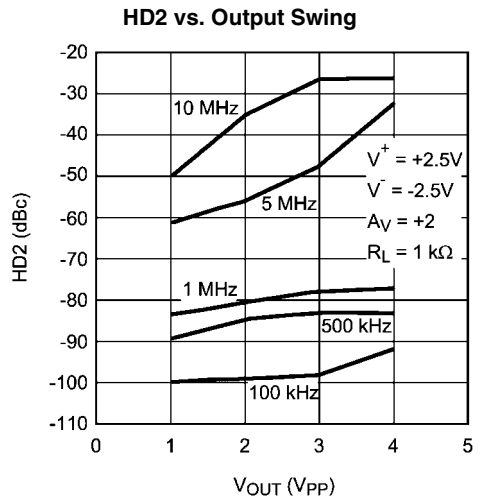
20195833



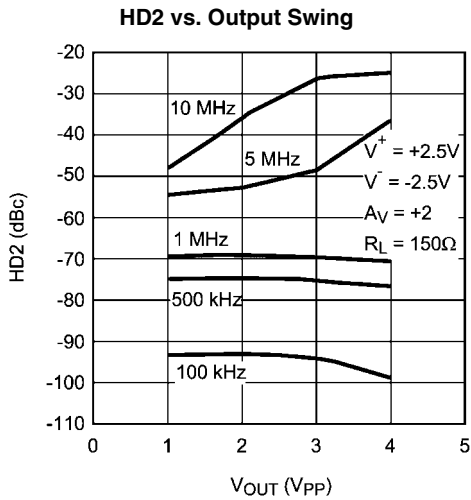
20195843



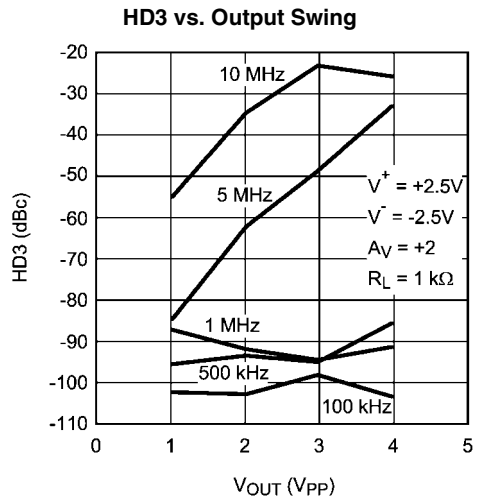
20195844



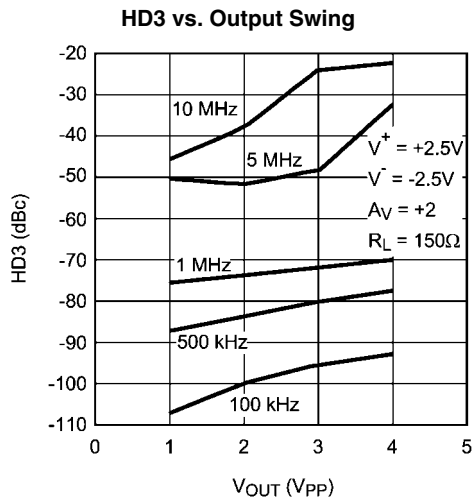
20195845



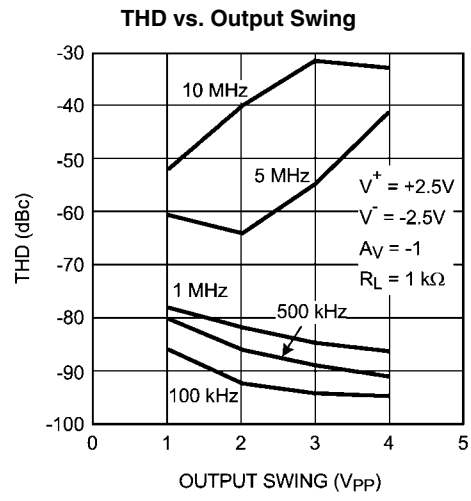
20195869



20195846

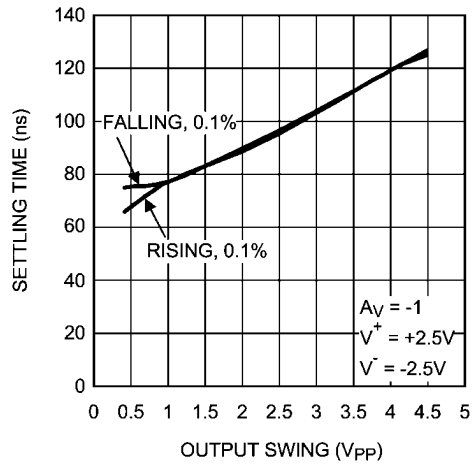


20195870

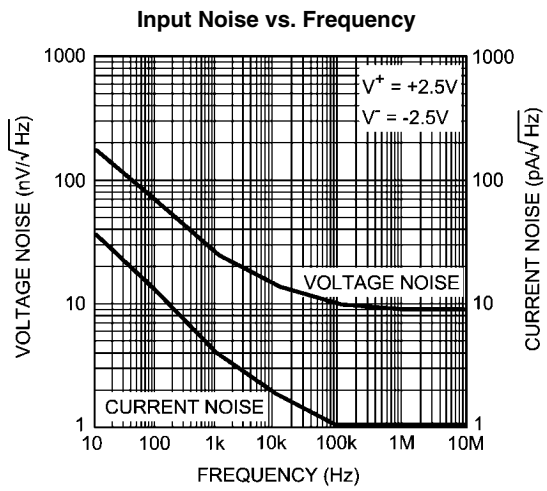


20195847

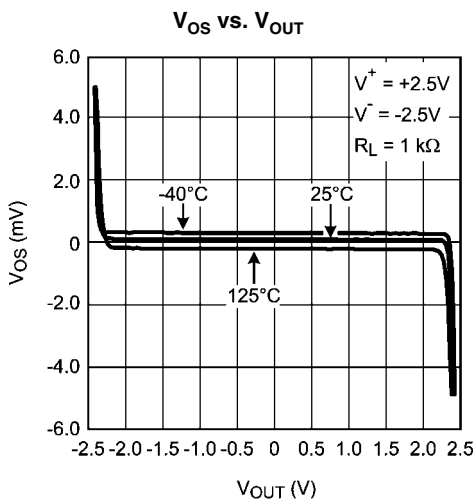
Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)



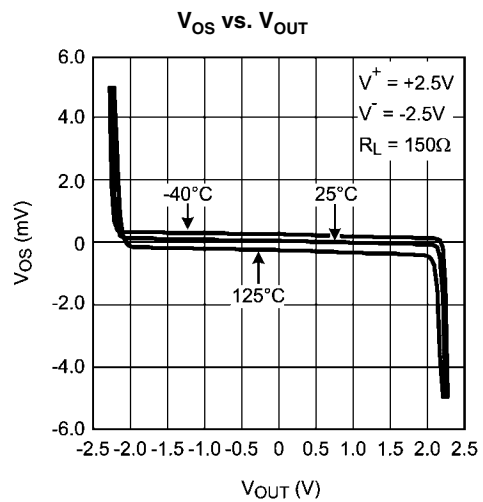
20195821



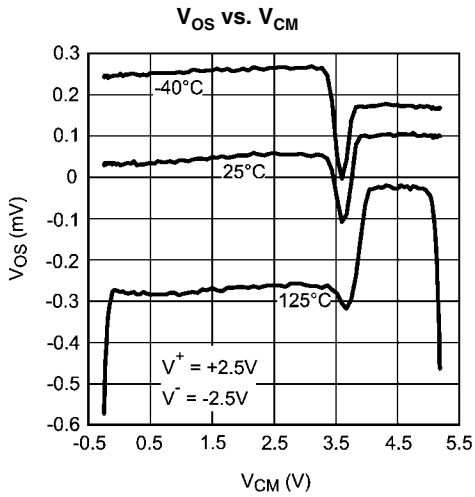
20195876



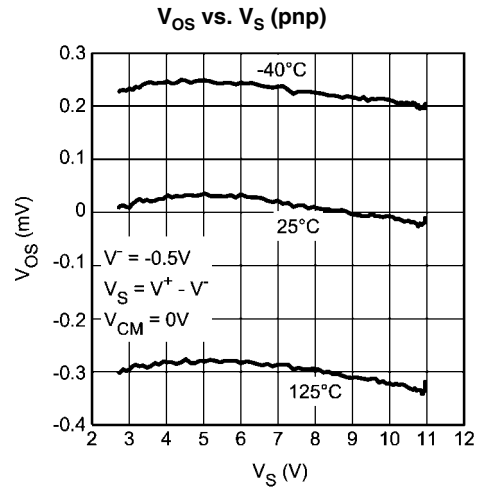
20195849



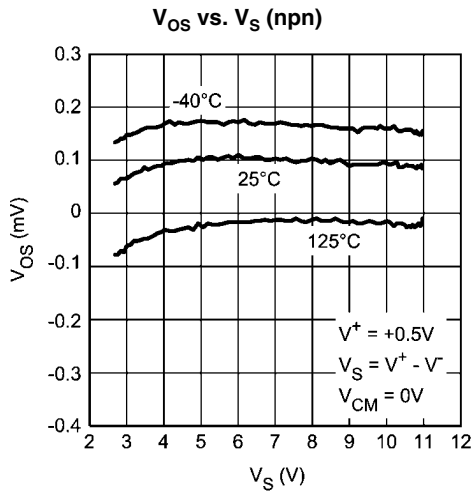
20195850



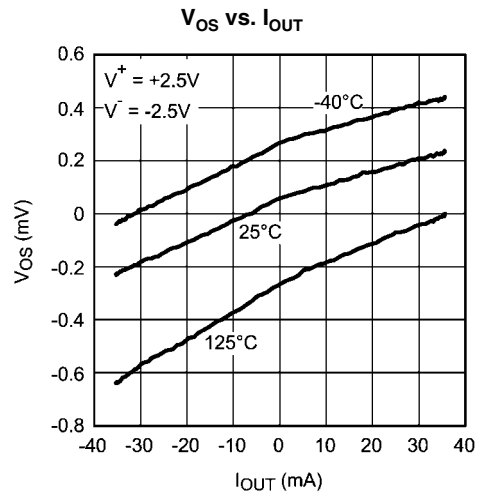
20195851



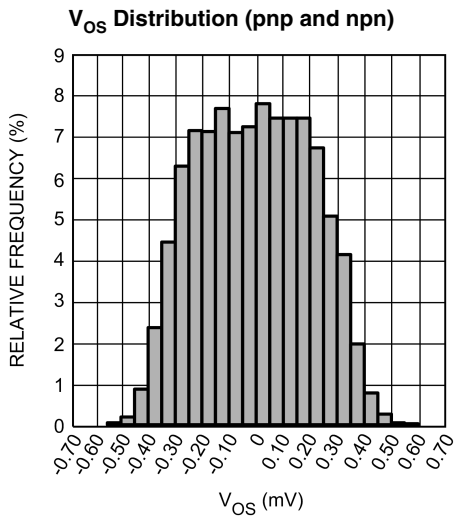
20195852



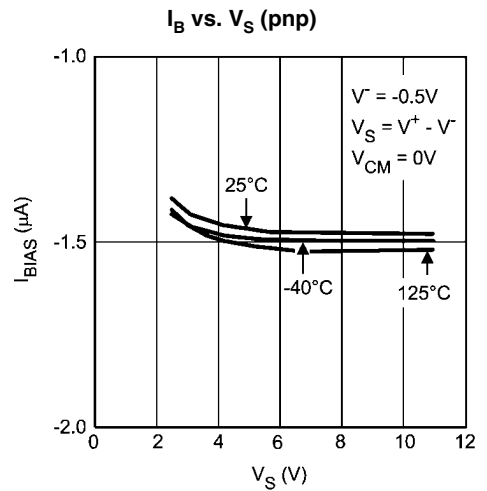
20195853



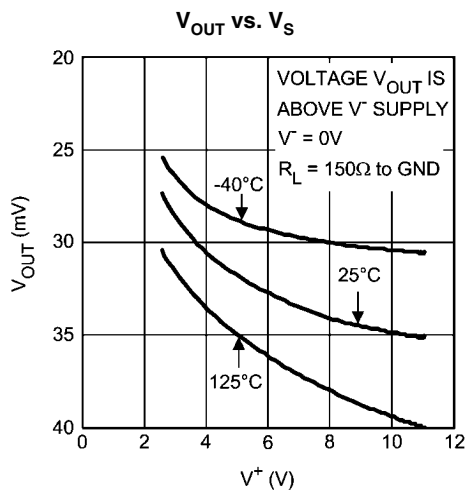
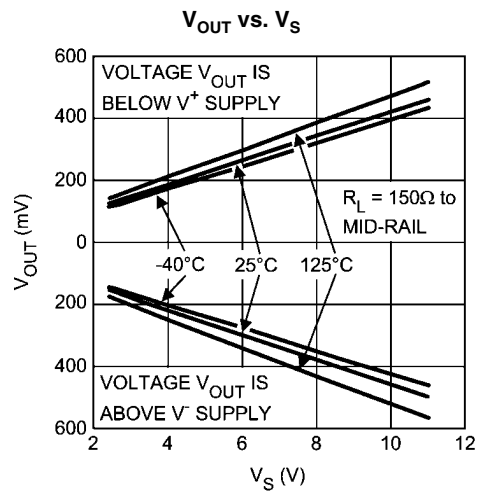
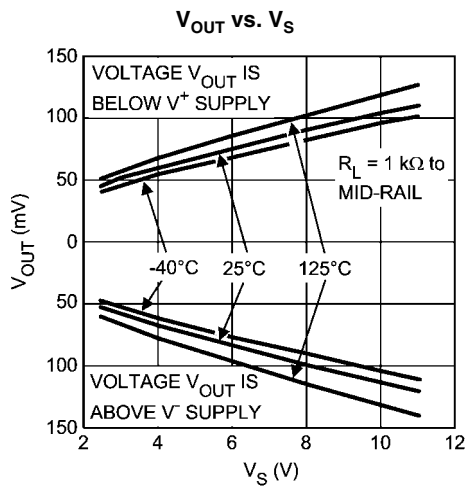
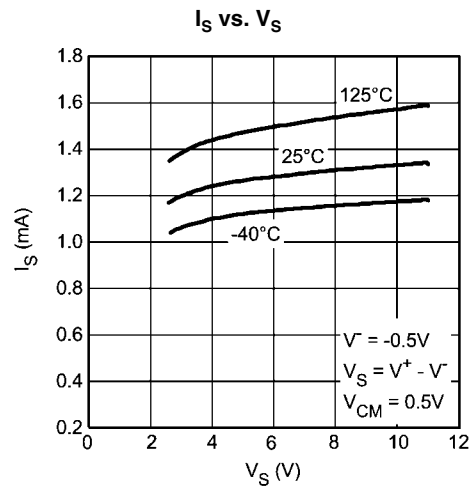
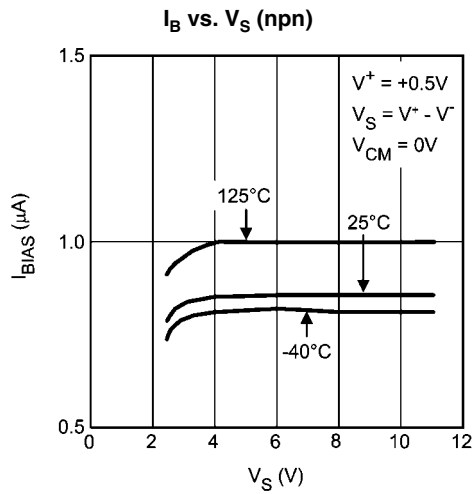
20195854



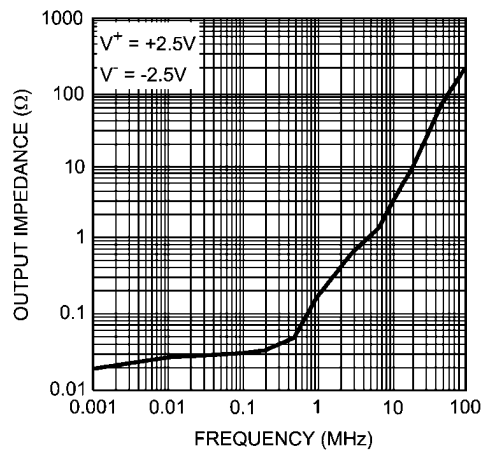
20195877

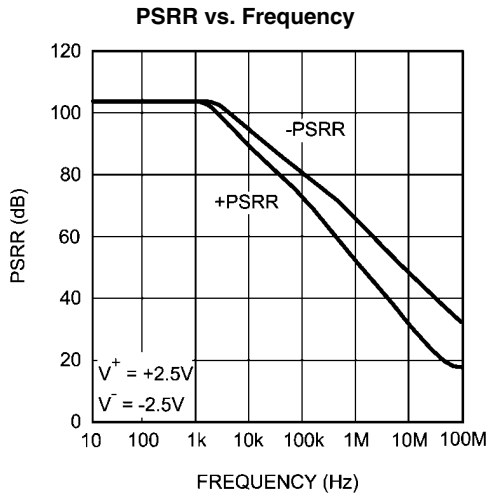


20195855

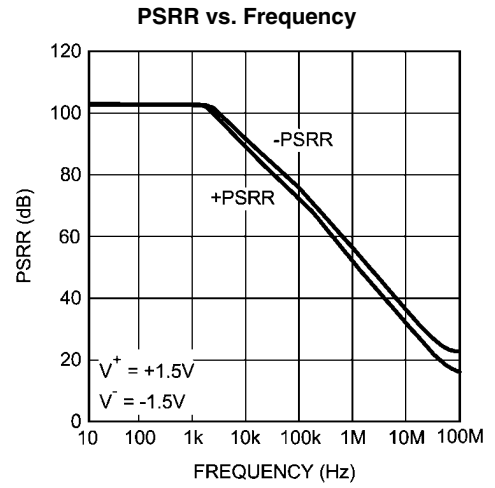


Closed Loop Output Impedance vs. Frequency $A_V = +1$

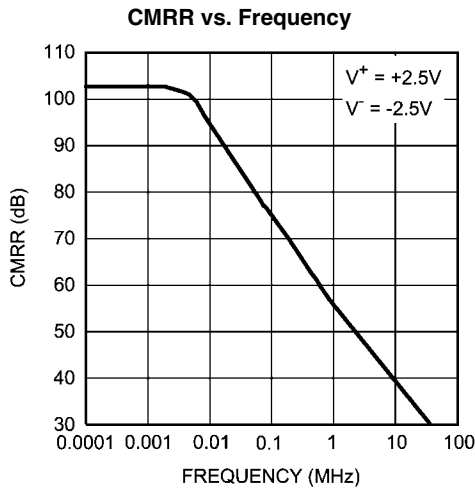




20195837

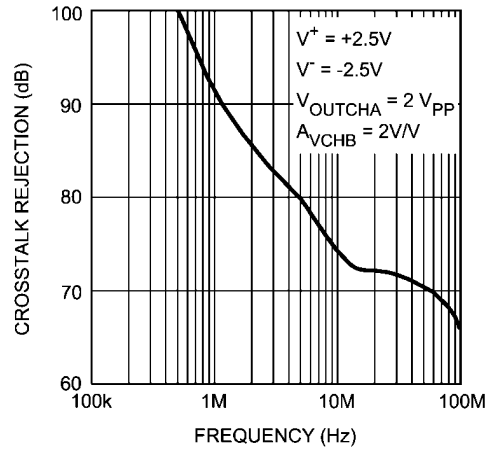


20195838

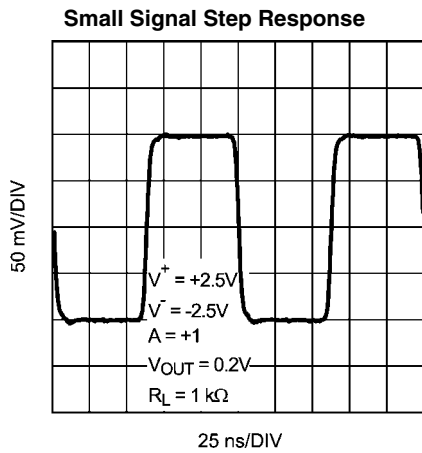


20195823

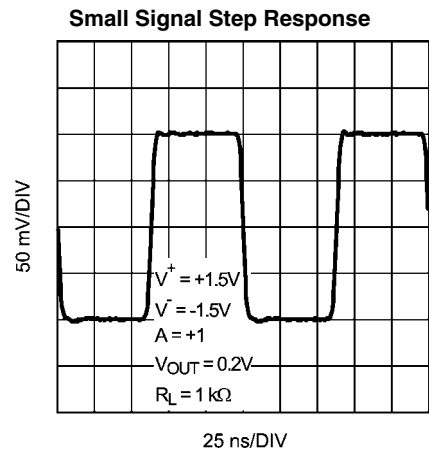
Crosstalk Rejection vs. Frequency (Output to Output)



20195879

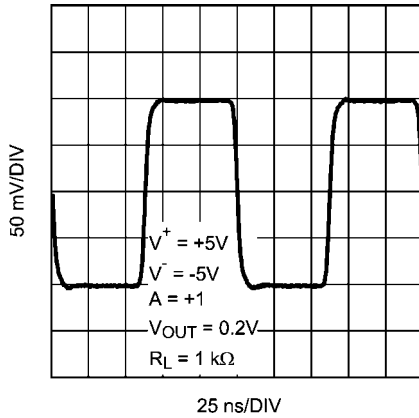


20195805



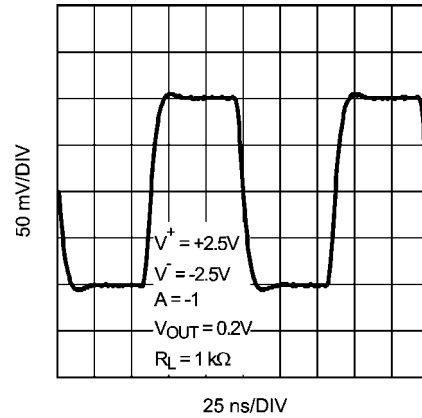
20195806

Small Signal Step Response



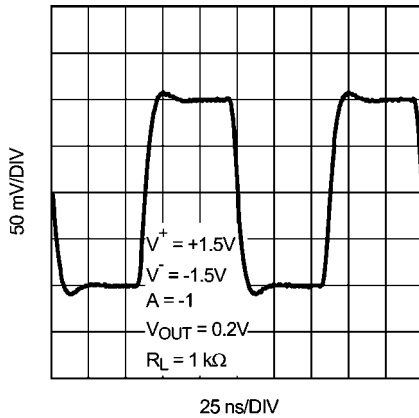
20195804

Small Signal Step Response



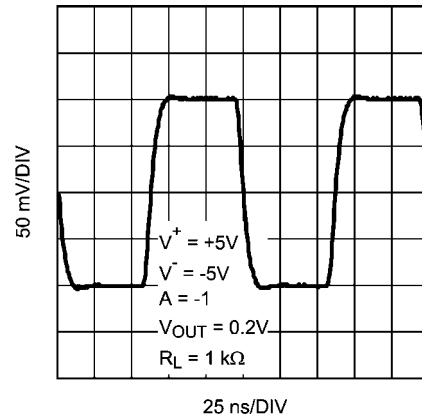
20195808

Small Signal Step Response



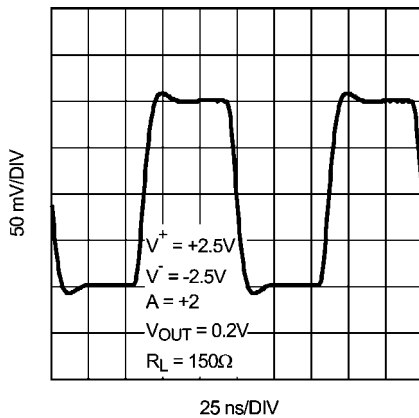
20195809

Small Signal Step Response



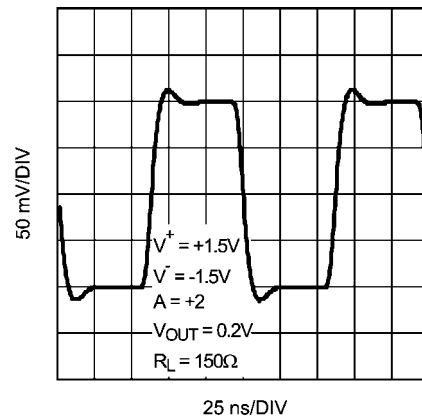
20195807

Small Signal Step Response



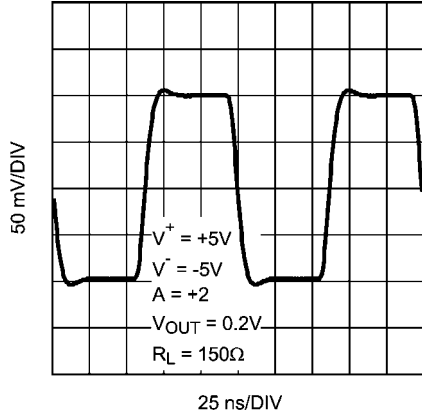
20195811

Small Signal Step Response



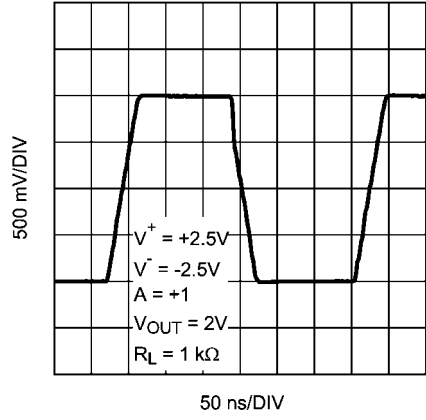
20195812

Small Signal Step Response



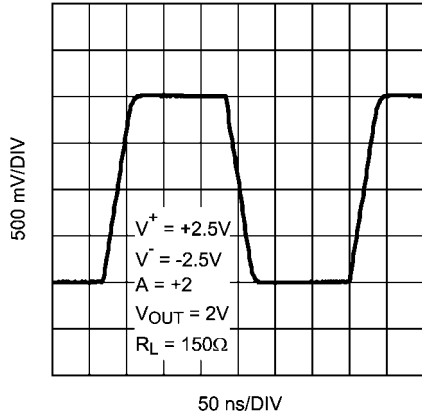
20195810

Large Signal Step Response



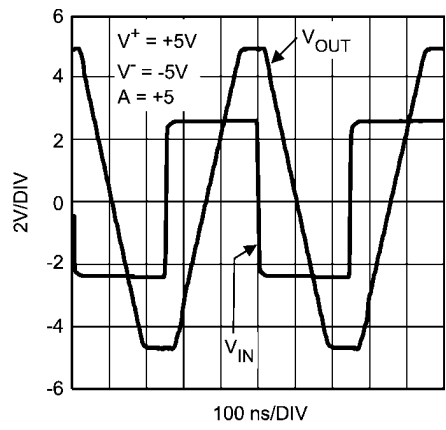
20195813

Large Signal Step Response



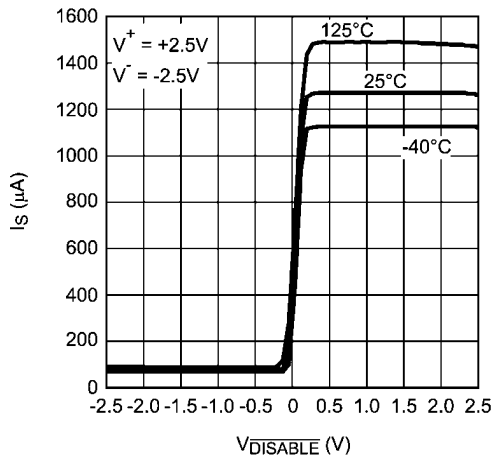
20195814

Overload Recovery Waveform



20195824

I_S vs. $V_{DISABLE}$



20195861

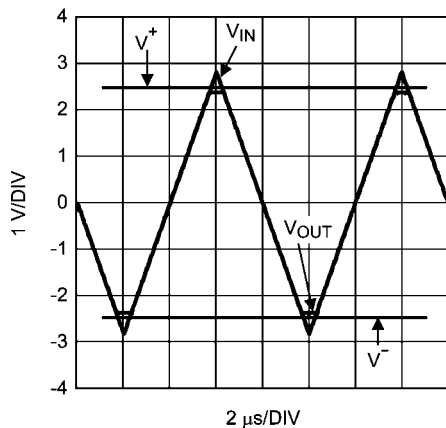
Application Information

The LMH6618 and LMH6619 are based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8 GHz) even under low supply voltage (2.7V) and low bias current.
- Common emitter push-push output stage. This architecture allows the output to reach within millivolts of either supply rail.
- Consistent performance from any supply voltage (2.7V - 11V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I_{OUT} .)
- Significant power saving compared to competitive devices on the market with similar performance.

With 3V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6618 and LMH6619 are well suited to many low voltage/low power applications. Even with 3V supplies, the -3 dB BW (at $A_V = +1$) is typically 120 MHz.

The LMH6618 and LMH6619 are designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). *Figure 1* shows the input and output voltage when the input voltage significantly exceeds the supply voltages.



20195825

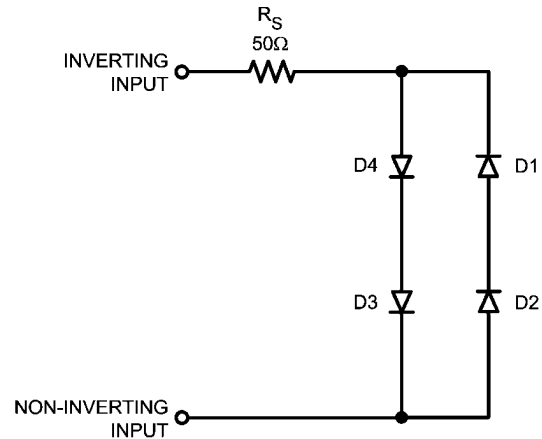
FIGURE 1. Input and Output Shown with CMVR Exceeded

If the input voltage range is exceeded by more than a diode drop beyond either rail, the internal ESD protection diodes will start to conduct. The current flow in these ESD diodes should be externally limited.

The LMH6618 can be shutdown by connecting the $\overline{\text{DISABLE}}$ pin to a voltage 0.5V below the supply midpoint which will reduce the supply current to typically less than

100 μA . The $\overline{\text{DISABLE}}$ pin is "active low" and should be connected through a resistor to V^+ for normal operation. Shutdown is guaranteed when the $\overline{\text{DISABLE}}$ pin is 0.5V below the supply midpoint at any operating supply voltage and temperature.

In the shutdown mode, essentially all internal device biasing is turned off in order to minimize supply current flow and the output goes into high impedance mode. During shutdown, the input stage has an equivalent circuit as shown in *Figure 2*.



20195839

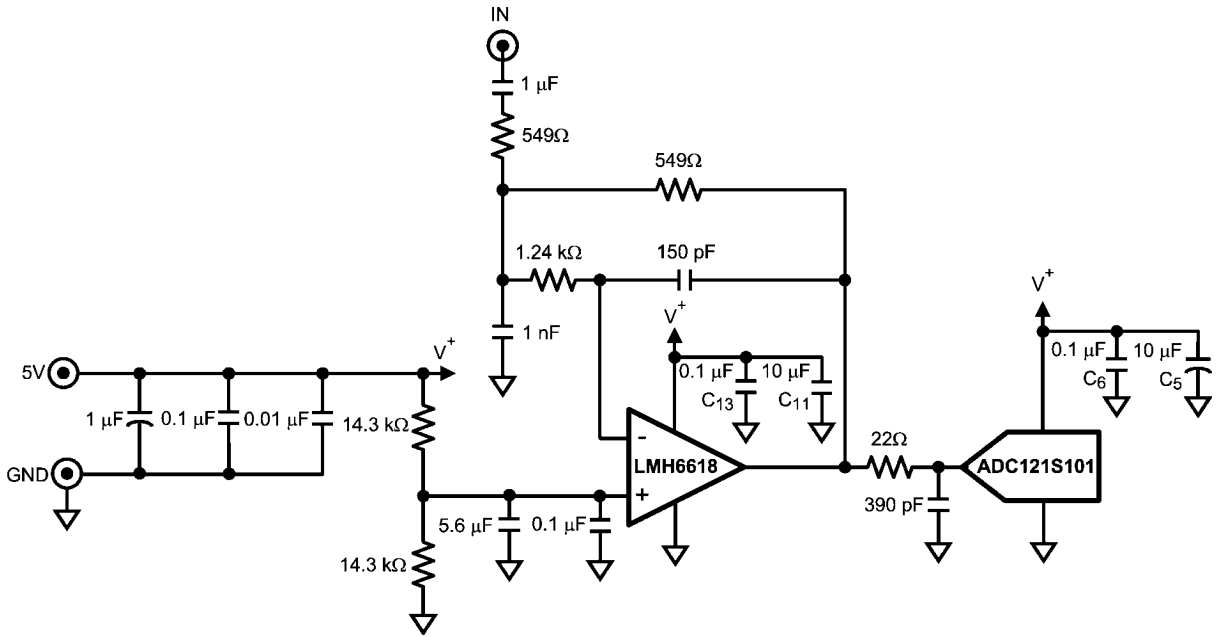
FIGURE 2. Input Equivalent Circuit During Shutdown

When the LMH6618 is shutdown, there may be current flow through the internal diodes shown, caused by input potential, if present. This current may flow through the external feedback resistor and result in an apparent output signal. In most shutdown applications the presence of this output is inconsequential. However, if the output is "forced" by another device, the other device will need to conduct the current described in order to maintain the output potential.

To keep the output at or near ground during shutdown when there is no other device to hold the output low, a switch using a transistor can be used to shunt the output to ground.

SINGLE CHANNEL ADC DRIVER

The low noise and wide bandwidth make the LMH6618 an excellent choice for driving a 12-bit ADC. *Figure 3* shows the schematic of the LMH6618 driving an ADC121S101. The ADC121S101 is a single channel 12-bit ADC. The LMH6618 is set up in a 2nd order multiple-feedback configuration with a gain of -1. The -3 dB point is at 500 kHz and the -0.01 dB point is at 100 kHz. The 22 Ω resistor and 390 pF capacitor form an antialiasing filter for the ADC121S101. The capacitor also stores and delivers charge to the switched capacitor input of the ADC. The capacitive load on the LMH6618 created by the 390 pF capacitor is decreased by the 22 Ω resistor. *Table 1* shows the performance data of the LMH6618 and the ADC121S101.



20195829

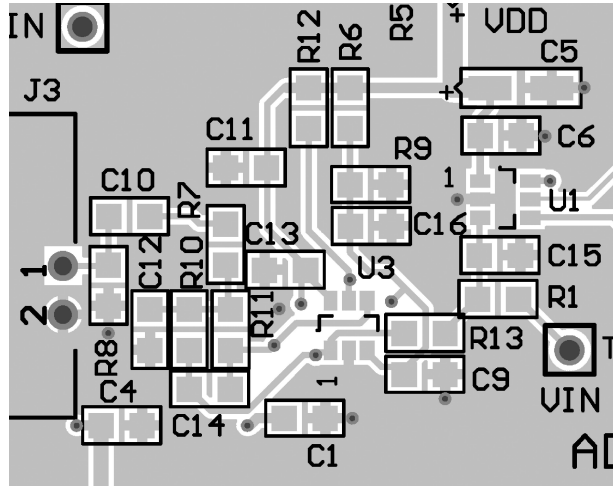
FIGURE 3. LMH6618 Driving an ADC121S101

TABLE 1. Performance Data for the LMH6618 Driving an ADC121S101

Parameter	Measured Value
Signal Frequency	100 kHz
Signal Amplitude	4.5V
SINAD	71.5 dB
SNR	71.87 dB
THD	-82.4 dB
SFDR	90.97 dB
ENOB	11.6 bits

When the op amp and the ADC are using the same supply, it is important that both devices are well bypassed. A 0.1 μF ceramic capacitor and a 10 μF tantalum capacitor should be located as close as possible to each supply pin.

A sample layout is shown in *Figure 4*. The 0.1 μF capacitors (C13 and C6) and the 10 μF capacitors (C11 and C5) are located very close to the supply pins of the LMH6618 and the ADC121S101.



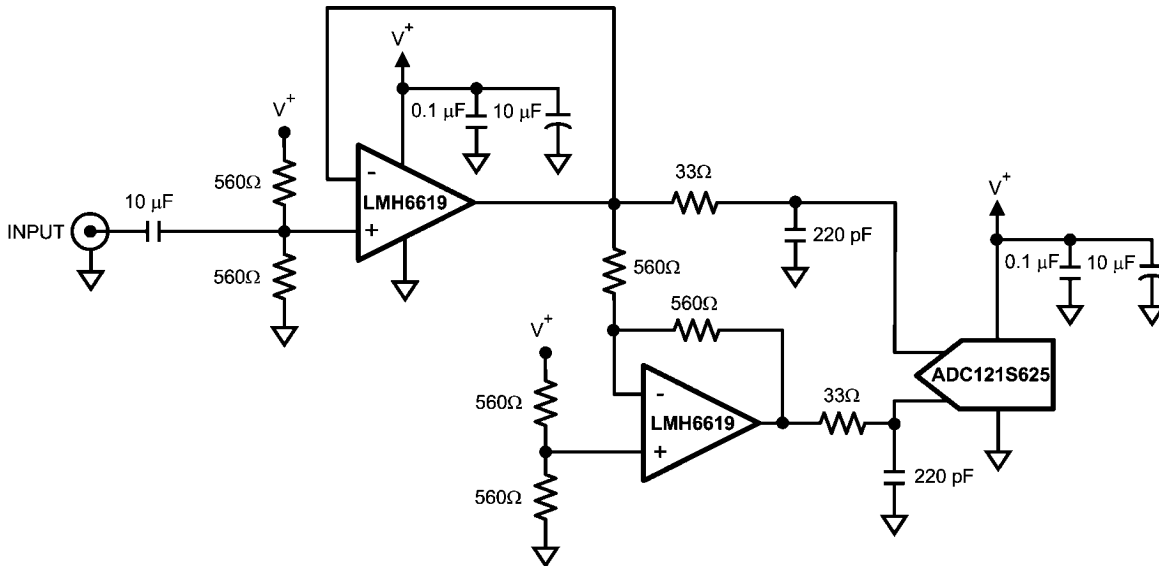
20195840

FIGURE 4. LMH6618 and ADC121S101 Layout

SINGLE TO DIFFERENTIAL ADC DRIVER

Figure 5 shows the LMH6619 used to drive a differential ADC with a single-ended input. The ADC121S625 is a fully differ-

ential 12-bit ADC. *Table 2* shows the performance data of the LMH6619 and the ADC121S625.



20195880

FIGURE 5. LMH6619 Driving an ADC121S625

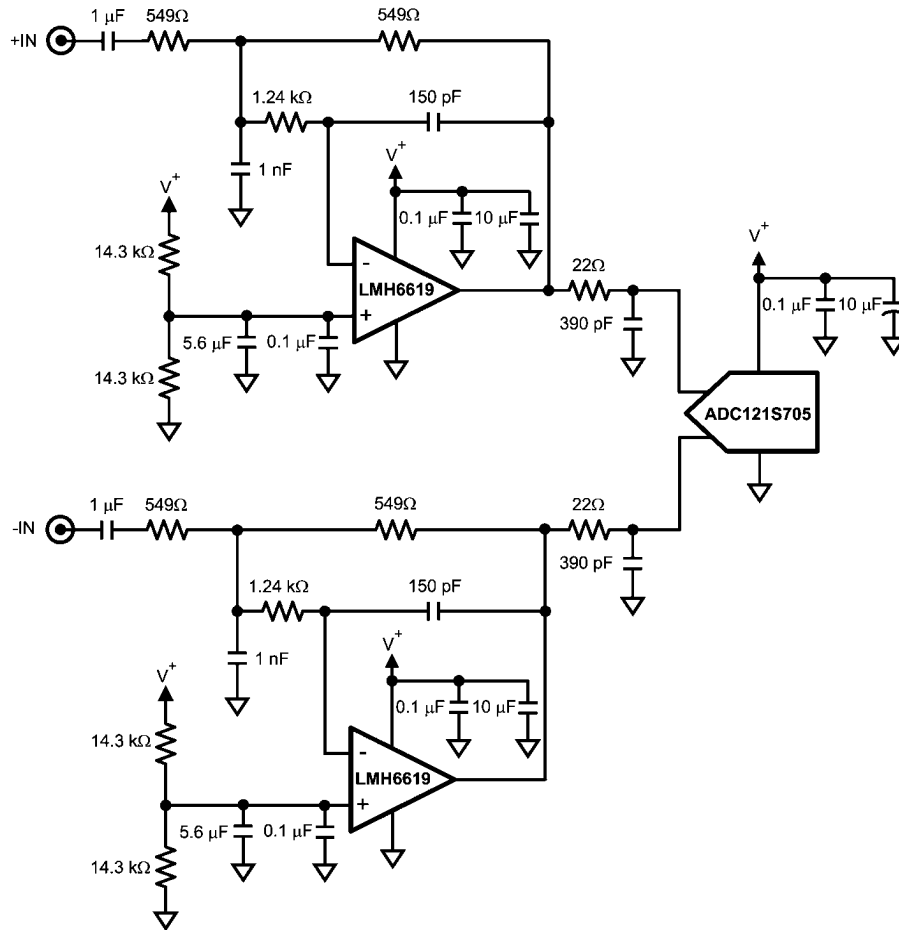
TABLE 2. Performance Data for the LMH6619 Driving an ADC121S625

Parameter	Measured Value
Signal Frequency	10 kHz
Signal Amplitude	2.5V
SINAD	67.9 dB
SNR	68.29 dB
THD	-78.6 dB
SFDR	75.0 dB
ENOB	11.0 bits

DIFFERENTIAL ADC DRIVER

The circuit in *Figure 3* can be used to drive both inputs of a differential ADC. *Figure 6* shows the LMH6619 driving an AD-

C121S705. The ADC121S705 is a fully differential 12-bit ADC. Performance with this circuit is similar to the circuit in *Figure 3*.



20195842

FIGURE 6. LMH6619 Driving an ADC121S705

DC LEVEL SHIFTING

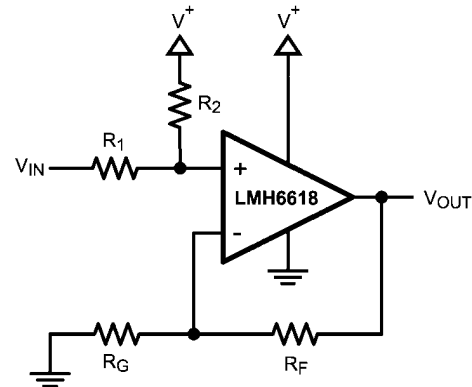
Often a signal must be both amplified and level shifted while using a single supply for the op amp. The circuit in *Figure 7* can do both of these tasks. The procedure for specifying the resistor values is as follows.

1. Determine the input voltage.
2. Calculate the input voltage midpoint, $V_{INMID} = V_{INMIN} + (V_{INMAX} - V_{INMIN})/2$.
3. Determine the output voltage needed.
4. Calculate the output voltage midpoint, $V_{OUTMID} = V_{OUTMIN} + (V_{OUTMAX} - V_{OUTMIN})/2$.
5. Calculate the gain needed, $gain = (V_{OUTMAX} - V_{OUTMIN}) / (V_{INMAX} - V_{INMIN})$.
6. Calculate the amount the voltage needs to be shifted from input to output, $\Delta V_{OUT} = V_{OUTMID} - gain \times V_{INMID}$.
7. Set the supply voltage to be used.
8. Calculate the noise gain, $noise\ gain = gain + \Delta V_{OUT}/V_S$.
9. Set R_F .
10. Calculate R_1 , $R_1 = R_F/gain$.
11. Calculate R_2 , $R_2 = R_F/(noise\ gain - gain)$.
12. Calculate R_G , $R_G = R_F/(noise\ gain - 1)$.

Check that both the V_{IN} and V_{OUT} are within the voltage ranges of the LMH6618.

The following example is for a V_{IN} of 0V to 1V with a V_{OUT} of 2V to 4V.

1. $V_{IN} = 0V$ to $1V$
2. $V_{INMID} = 0V + (1V - 0V)/2 = 0.5V$
3. $V_{OUT} = 2V$ to $4V$
4. $V_{OUTMID} = 2V + (4V - 2V)/2 = 3V$
5. $Gain = (4V - 2V)/(1V - 0V) = 2$
6. $\Delta V_{OUT} = 3V - 2 \times 0.5V = 2$
7. For the example the supply voltage will be $+5V$.
8. $Noise\ gain = 2 + 2/5V = 2.4$
9. $R_F = 2\ k\Omega$
10. $R_1 = 2\ k\Omega/2 = 1\ k\Omega$
11. $R_2 = 2\ k\Omega/(2.4-2) = 5\ k\Omega$
12. $R_G = 2\ k\Omega/(2.4 - 1) = 1.43\ k\Omega$



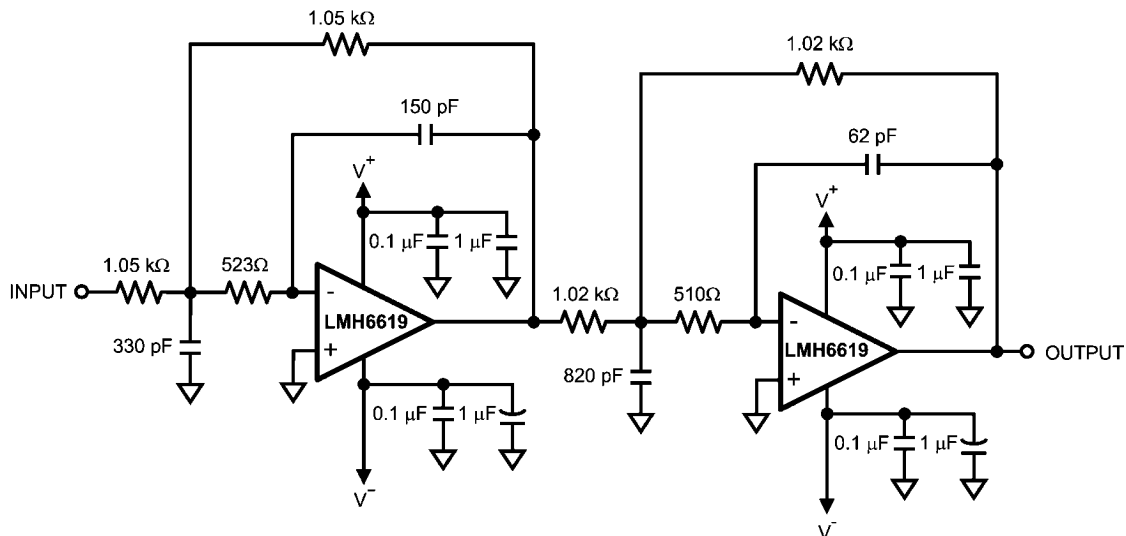
20195848

FIGURE 7. DC Level Shifting

4th ORDER MULTIPLE FEEDBACK LOW-PASS FILTER

Figure 8 shows the LMH6619 used as the amplifier in a multiple feedback low pass filter. This filter is set up to have a gain of +1 and a -3 dB point of 1 MHz. Values can be determined

by using the WEBENCH® Active Filter Designer found at amplifiers.national.com.

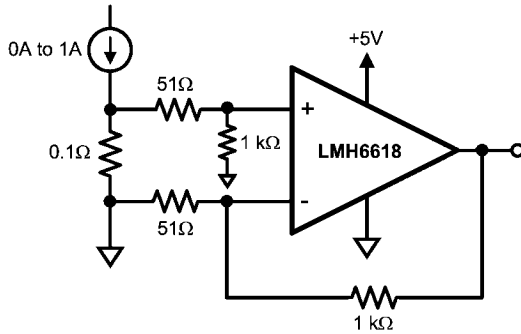


20195828

FIGURE 8. 4th Order Multiple Feedback Low-Pass Filter

CURRENT SENSE AMPLIFIER

With its rail-to-rail input and output capability, low V_{OS} , and low I_B the LMH6618 is an ideal choice for a current sense amplifier application. *Figure 9* shows the schematic of the LMH6618 set up in a low-side sense configuration which provides a conversion gain of 2V/A. Voltage error due to V_{OS} can be calculated to be $V_{OS} \times (1 + R_F/R_G)$ or $0.6 \text{ mV} \times 21 = 12.6 \text{ mV}$. Voltage error due to I_O is $I_O \times R_F$ or $0.26 \mu\text{A} \times 1 \text{ k}\Omega = 0.26 \text{ mV}$. Hence total voltage error is $12.6 \text{ mV} + 0.26 \text{ mV}$ or 12.86 mV which translates into a current error of $12.86 \text{ mV}/(2 \text{ V/A}) = 6.43 \text{ mA}$.

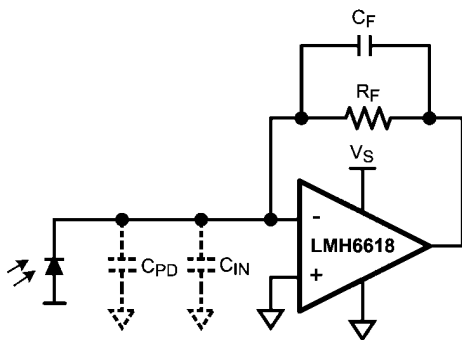


20195841

FIGURE 9. Current Sense Amplifier

TRANSIMPEDANCE AMPLIFIER

By definition, a photodiode produces either a current or voltage output from exposure to a light source. A Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal. The TIA often will need to be compensated to insure proper operation.



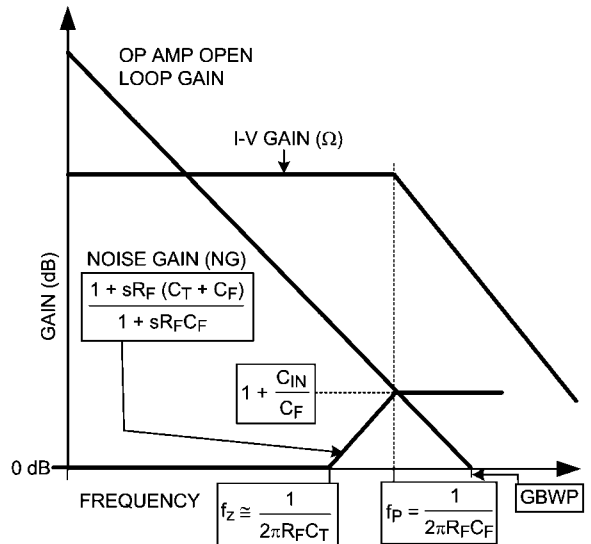
20195862

FIGURE 10. Photodiode Modeled with Capacitance Elements

Figure 10 shows the LMH6618 modeled with photodiode and the internal op amp capacitances. The LMH6618 allows circuit operation of a low intensity light due to its low input bias current by using larger values of gain (R_F). The total capacitance (C_T) on the inverting terminal of the op amp includes the photodiode capacitance (C_{PD}) and the input capacitance of the op amp (C_{IN}). This total capacitance (C_T) plays an important role in the stability of the circuit. The noise gain of this circuit determines the stability and is defined by:

$$NG = \frac{1 + sR_F (C_T + C_F)}{1 + sC_F R_F} \tag{1}$$

Where, $f_z \cong \frac{1}{2\pi R_F C_T}$ and $f_p = \frac{1}{2\pi R_F C_F}$ (2)



20195865

FIGURE 11. Bode Plot of Noise Gain Intersecting with Op Amp Open-Loop Gain

Figure 11 shows the bode plot of the noise gain intersecting the op amp open loop gain. With larger values of gain, C_T and R_F create a zero in the transfer function. At higher frequencies the circuit can become unstable due to excess phase shift around the loop.

A pole at f_p in the noise gain function is created by placing a feedback capacitor (C_F) across R_F . The noise gain slope is flattened by choosing an appropriate value of C_F for optimum performance.

Theoretical expressions for calculating the optimum value of C_F and the expected -3 dB bandwidth are:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F (GBWP)}} \tag{3}$$

$$f_{-3 \text{ dB}} = \sqrt{\frac{GBWP}{2\pi R_F C_T}} \tag{4}$$

Equation 4 indicates that the -3 dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

Table 3 shows the measurement results of the LMH6618 with different photodiodes having various capacitances (C_{PD}) and a feedback resistance (R_F) of $1 \text{ k}\Omega$.

TABLE 3. TIA (Figure 1) Compensation and Performance Results

C_{PD} (pF)	C_T (pF)	$C_{F\text{ CAL}}$ (pF)	$C_{F\text{ USED}}$ (pF)	$f_{-3\text{ dB CAL}}$ (MHz)	$f_{-3\text{ dB MEAS}}$ (MHz)	Peaking (dB)
22	24	7.7	5.6	23.7	20	0.9
47	49	10.9	10	16.6	15.2	0.8
100	102	15.8	15	11.5	10.8	0.9
222	224	23.4	18	7.81	8	2.9

Note:
 GBWP = 65 MHz
 $C_T = C_{PD} + C_{IN}$
 $C_{IN} = 2\text{ pF}$
 $V_S = \pm 2.5\text{ V}$

Figure 12 shows the frequency response for the various photodiodes in Table 3.

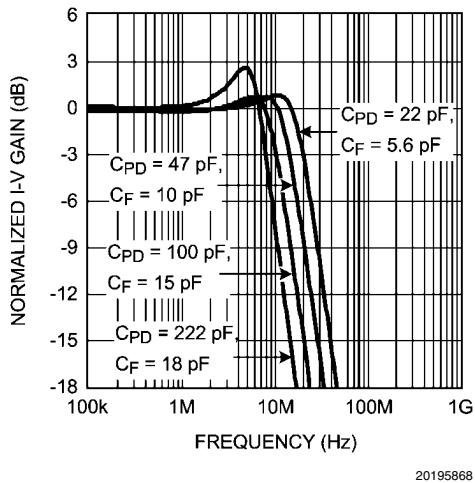


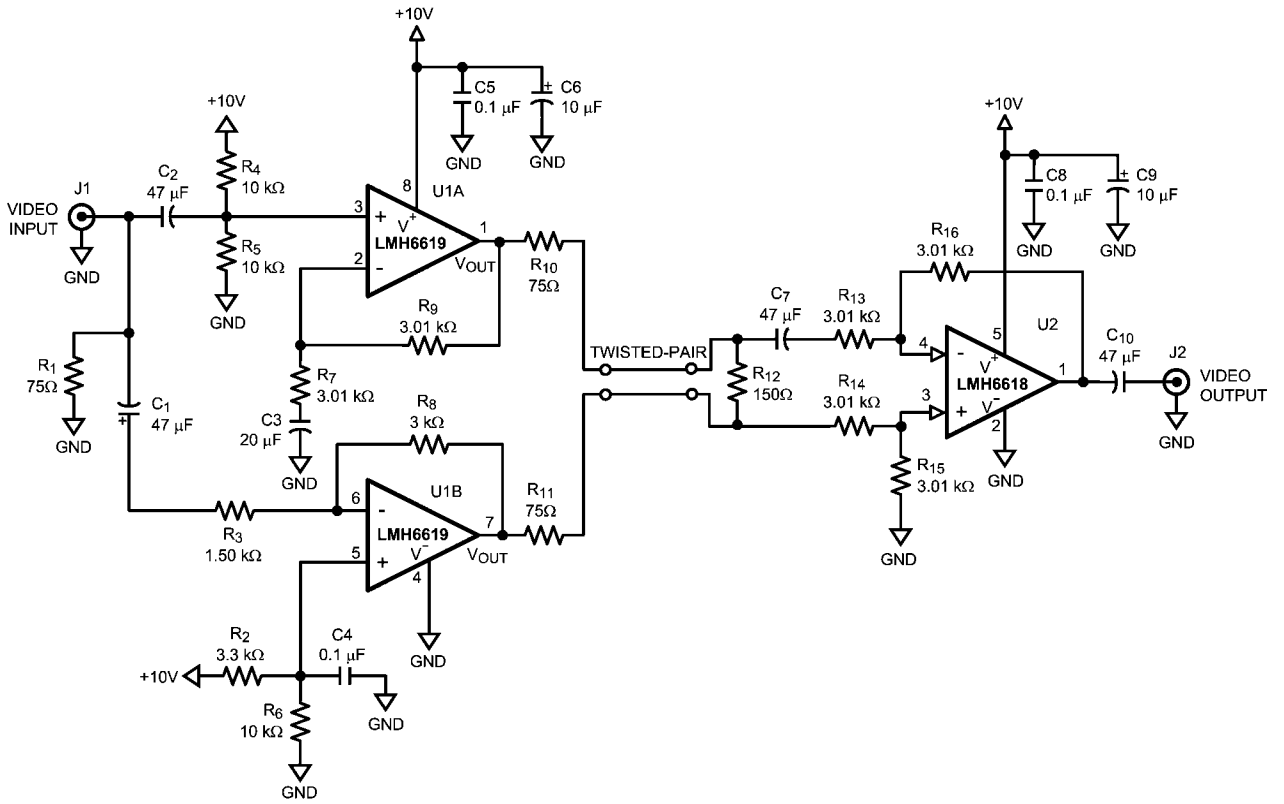
FIGURE 12. Frequency Response for Various Photodiode and Feedback Capacitors

When analyzing the noise at the output of the TIA, it is important to note that the various noise sources (i.e. op amp

noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. The op amp noise voltage will be gained up in the region between the noise gain's zero and pole (f_z and f_p in Figure 11). The higher the values of R_F and C_T , the sooner the noise gain peaking starts and therefore its contribution to the total output noise will be larger. It is obvious to note that it is advantageous to minimize C_{IN} by proper choice of op amp or by applying a reverse bias across the diode at the expense of excess dark current and noise.

DIFFERENTIAL CABLE DRIVER FOR NTSC VIDEO

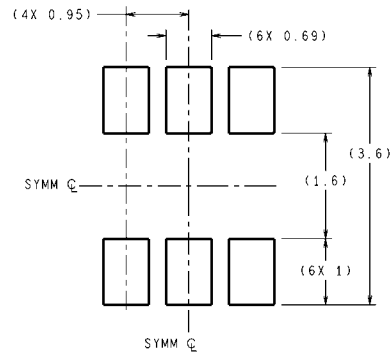
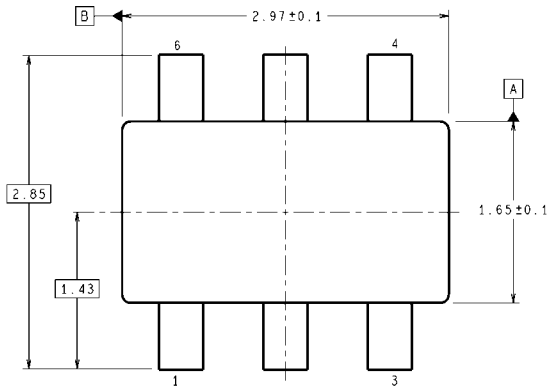
The LMH6618 and LMH6619 can be used to drive an NTSC video signal on a twisted-pair cable. Figure 13 shows the schematic of a differential cable driver for NTSC video. This circuit can be used to transmit the signal from a camera over a twisted pair to a monitor or display located a distance. C_1 and C_2 are used to AC couple the video signal into the LMH6619. The two amplifiers of the LMH6619 are set to a gain of 2 to compensate for the 75Ω back termination resistors on the outputs. The LMH6618 is set to a gain of 1. Because of the DC bias the output of the LMH6618 is AC coupled. Most monitors and displays will accept AC coupled inputs.



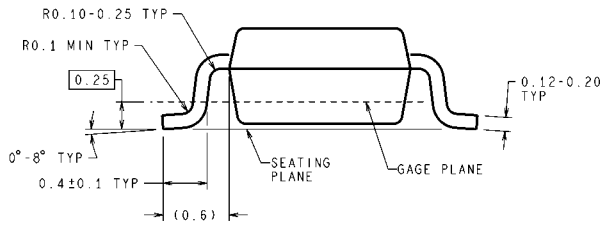
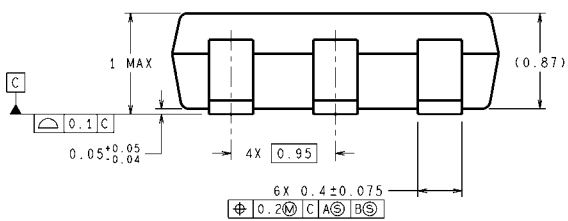
20195881

FIGURE 13. Differential Cable Driver

Physical Dimensions inches (millimeters) unless otherwise noted



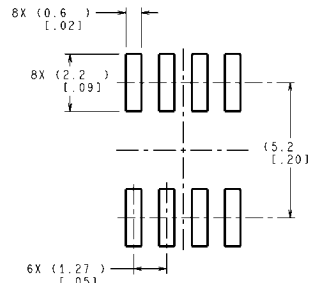
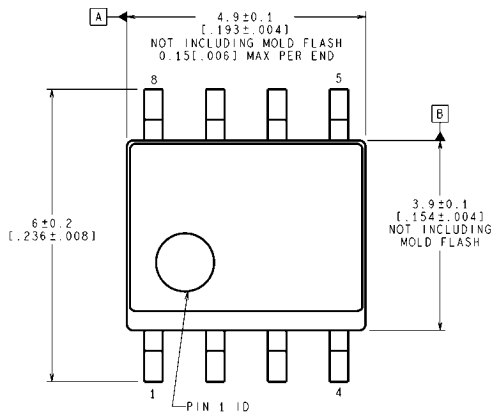
RECOMMENDED LAND PATTERN



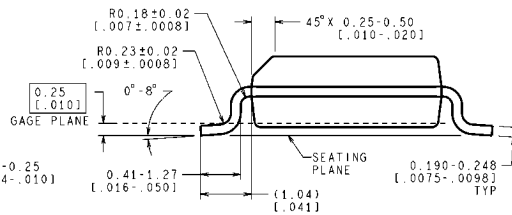
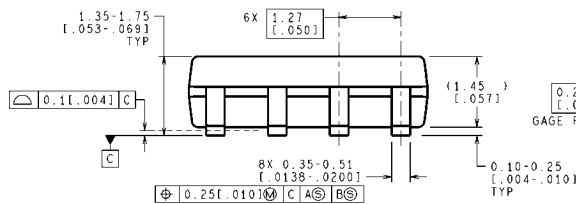
DIMENSIONS ARE IN MILLIMETERS

MK06A (Rev D)

**6-Pin TSOT23
NS Package Number MK06A**



RECOMMENDED LAND PATTERN



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [] ARE INCHES
DIMENSIONS IN () FOR REFERENCE ONLY

M08A (Rev L)

**8-Pin SOIC
NS Package Number M08A**

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/lido		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation
 For the most current product information visit us at www.national.com



National Semiconductor Americas Technical Support Center
 Email: support@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
 Email: europe.support@nsc.com
 German Tel: +49 (0) 180 5010 771
 English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
 Email: jpn.feedback@nsc.com