

FDD770N15A

N-Channel PowerTrench® MOSFET

150V, 18A, 77mΩ

Features

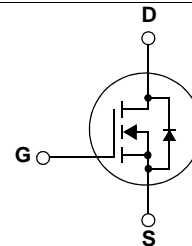
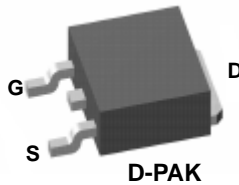
- $R_{DS(on)} = 61m\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 12A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Application

- DC to DC Converters
- Synchronous Rectification for Server / Telecom PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



MOSFET Maximum Ratings

Symbol	Parameter	FDD770N15A	Units
V_{DSS}	Drain to Source Voltage	150	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ C$, Silicon Limited)	18
		- Continuous ($T_C = 100^\circ C$, Silicon Limited)	11.4
I_{DM}	Drain Current	- Pulsed (Note 1)	36
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	31.7
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.0
P_D	Power Dissipation	($T_C = 25^\circ C$)	56.8
		- Derate above $25^\circ C$	0.46
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	FDD770N15A	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	2.2	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	87	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD770N15A	FDD770N15A	D-PAK	380MM	16MM	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.0824	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 120\text{V}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	1 500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 12\text{A}$	-	61	77	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 12\text{A}$	-	20	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	575	765	pF	
C_{oss}	Output Capacitance		-	64	85	pF	
C_{rss}	Reverse Transfer Capacitance		-	3.9	6	pF	
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$	-	113	-	pF	
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 75\text{V}, I_D = 12\text{A}$ $V_{GS} = 10\text{V}$	-	8.4	11	nC	
Q_{gs}	Gate to Source Gate Charge		-	2.7	-	nC	
Q_{gd}	Gate to Drain "Miller" Charge		-	1.8	-	nC	
$V_{plateau}$	Gate Plateau Voltage		(Note 4)	-	5.7	-	V
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0\text{V}, I_D = 6\text{A}$	(Note 5)	-	6.9	-	nC
Q_{oss}	Output Charge	$V_{DS} = 37.5\text{V}, V_{GS} = 0\text{V}$	-	14	-	nC	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{V}, I_D = 12\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 4.7\Omega$	-	10.3	30.6	ns
t_r	Turn-On Rise Time		-	3.1	16.2	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15.8	41.6	ns
t_f	Turn-Off Fall Time		(Note 4)	-	2.8	15.6
ESR	Equivalent Series Resistance (G-S)	$f = 1\text{MHz}$	-	0.5	-	Ω

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	18	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	36	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 12\text{A}$	-	-	1.25	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, V_{DD} = 75\text{V}, I_{SD} = 12\text{A}$	-	56.4	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	109	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 3\text{mH}, I_{AS} = 4.6\text{A}$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 12\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics
5. See the test circuit in page 8

Typical Performance Characteristics

Figure 1. On-Region Characteristics

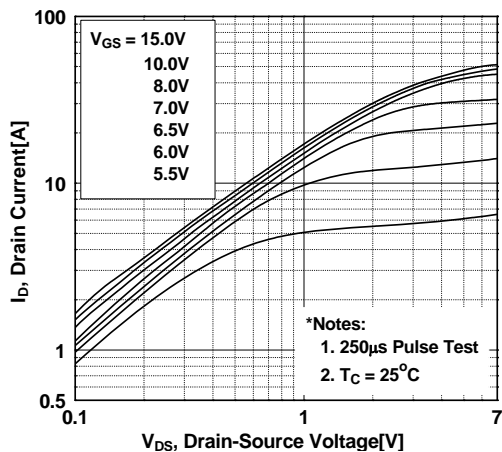


Figure 2. Transfer Characteristics

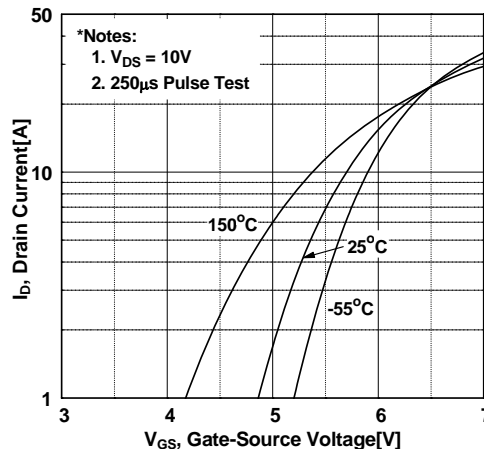


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

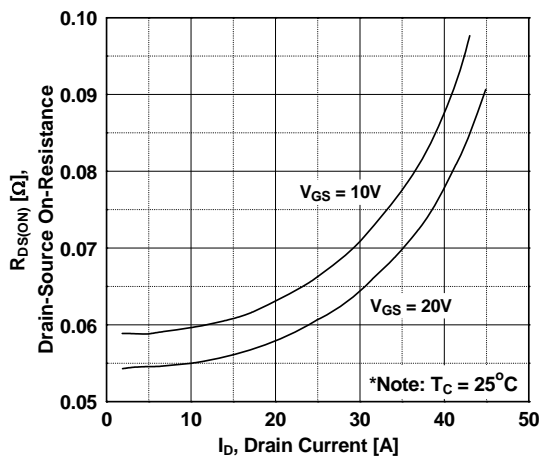


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

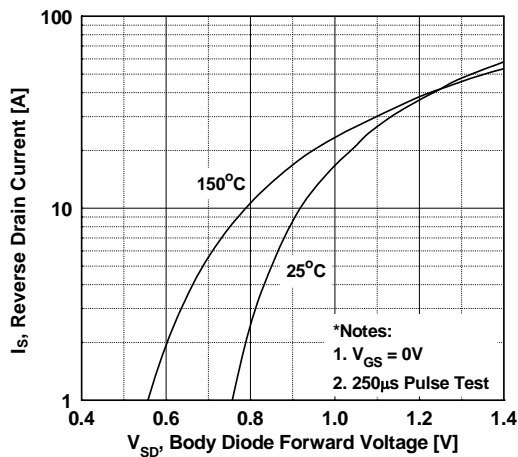


Figure 5. Capacitance Characteristics

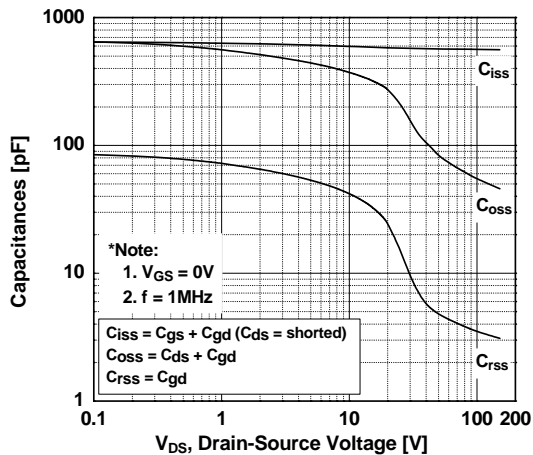
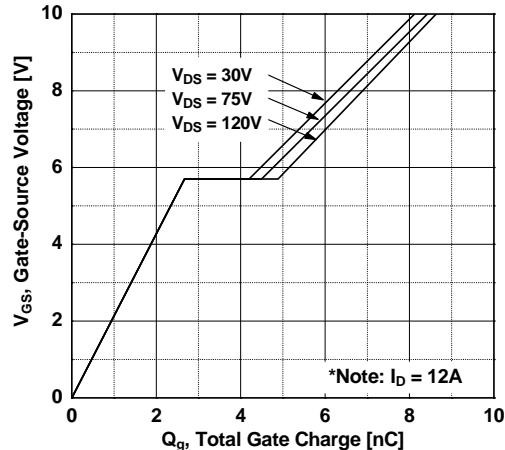


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

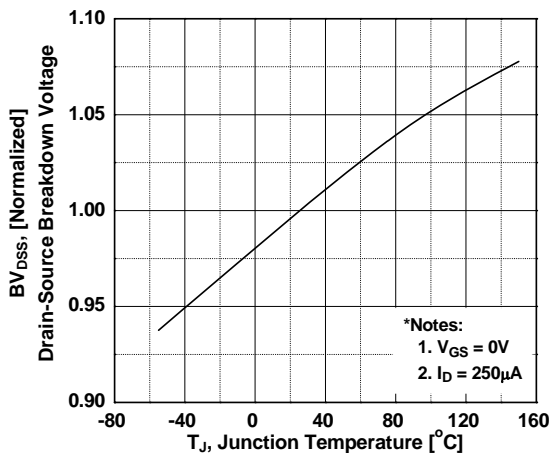


Figure 8. On-Resistance Variation vs. Temperature

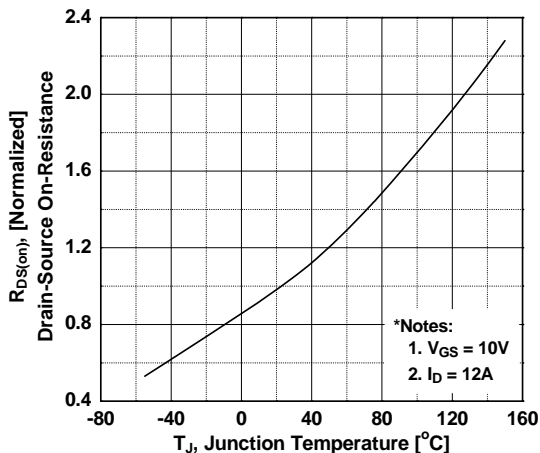


Figure 9. Maximum Safe Operating Area vs. Case Temperature

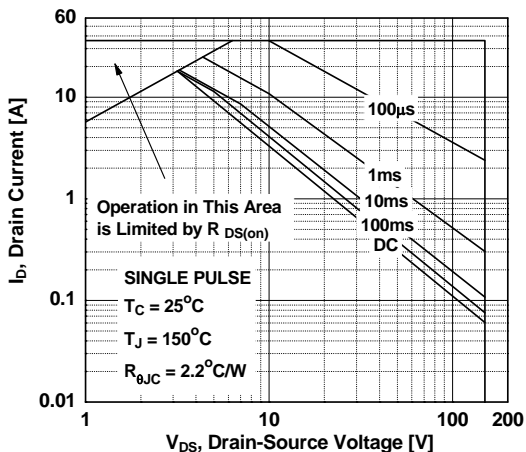


Figure 10. Maximum Drain Current

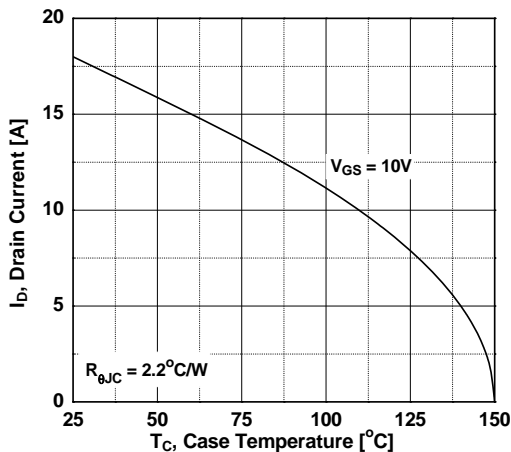


Figure 11. E_oss vs. Drain to Source Voltage

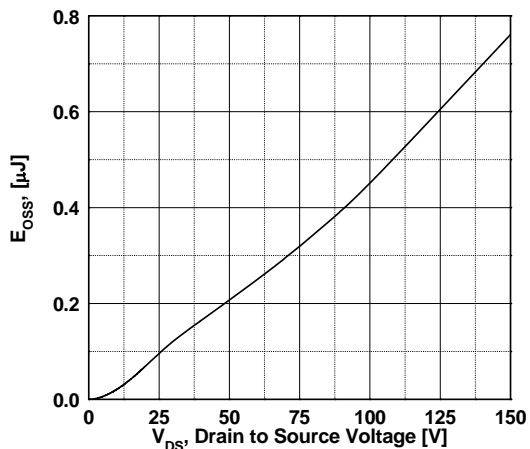
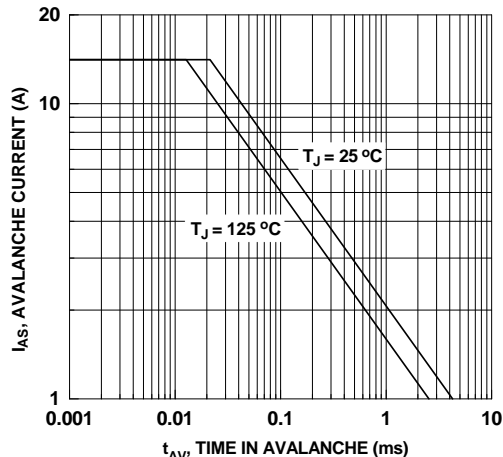
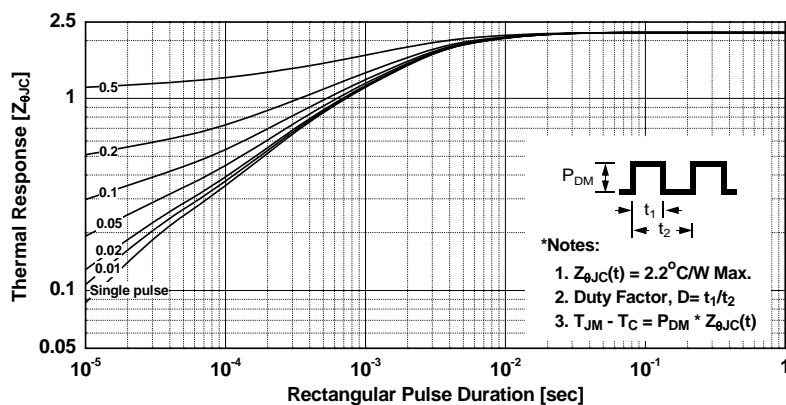


Figure 12. Unclamped Inductive Switching Capability

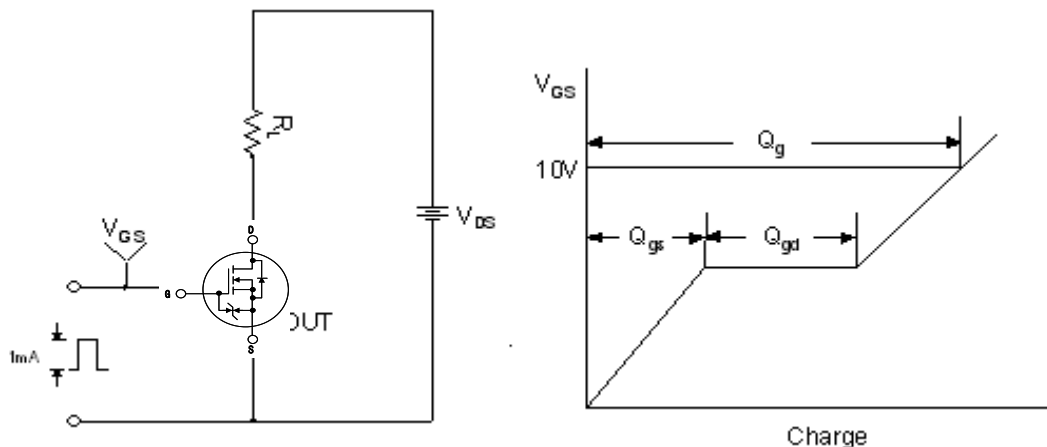


Typical Performance Characteristics (Continued)

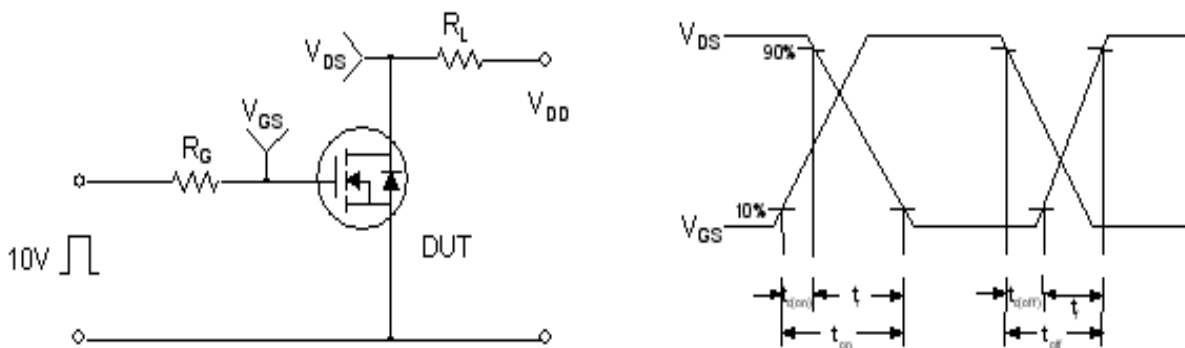
Figure 13. Transient Thermal Response Curve



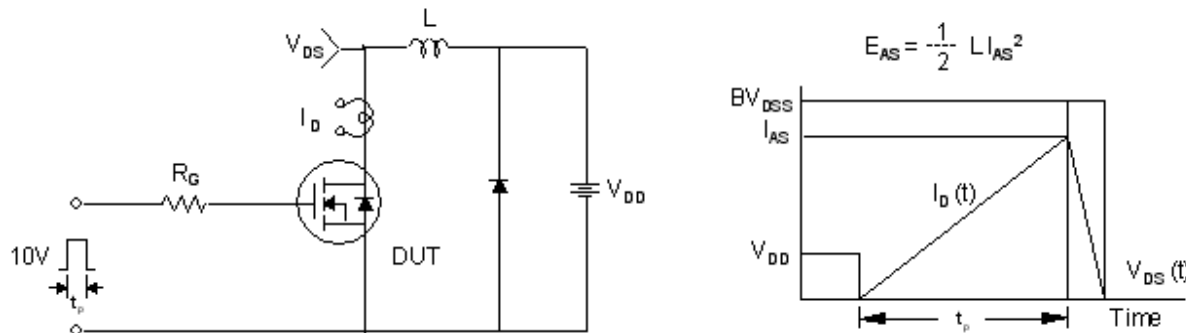
Gate Charge Test Circuit & Waveform



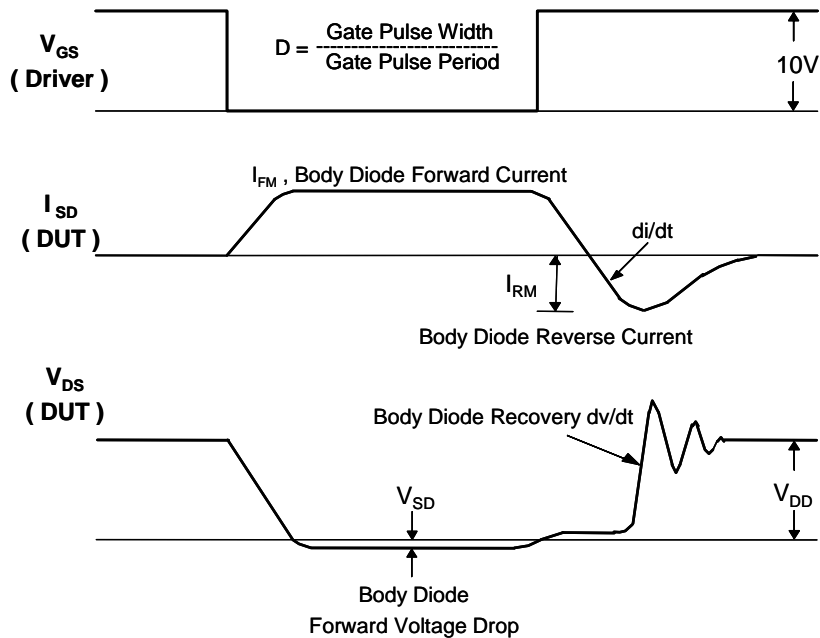
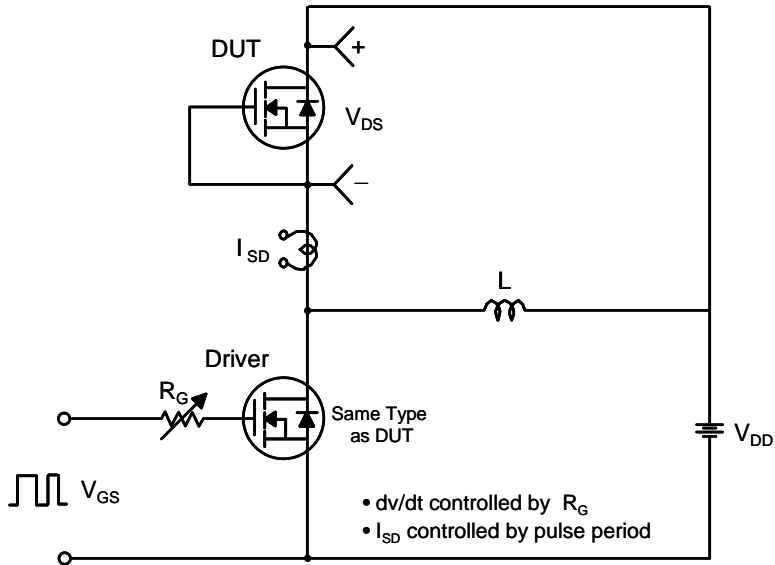
Resistive Switching Test Circuit & Waveforms



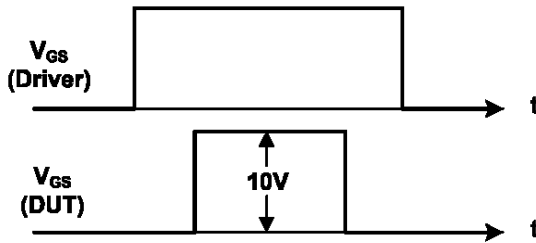
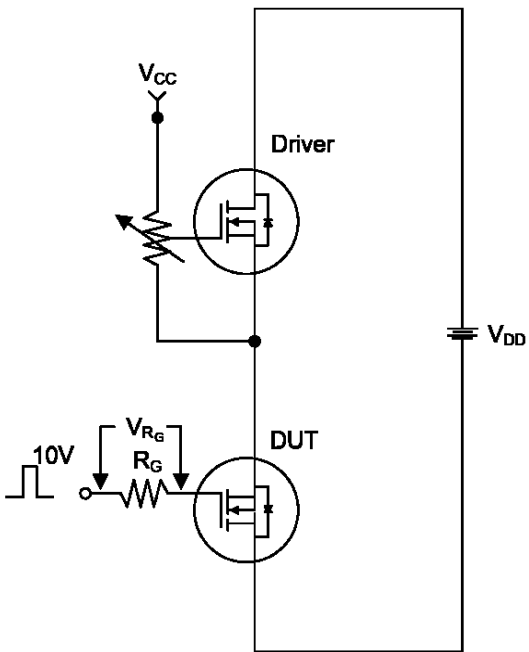
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



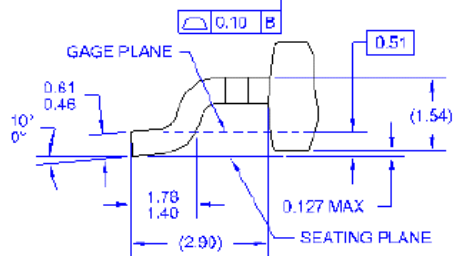
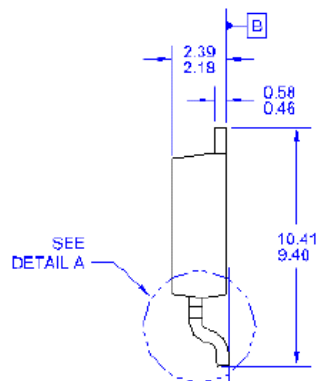
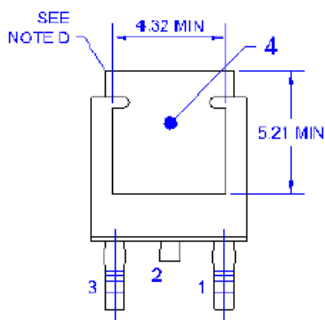
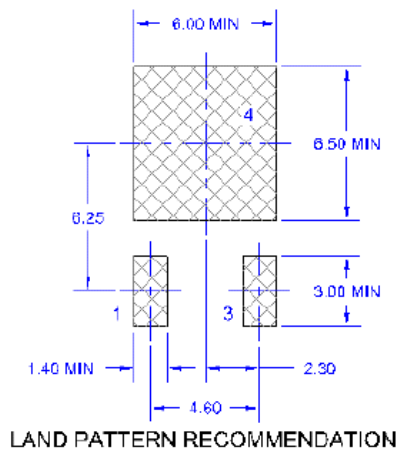
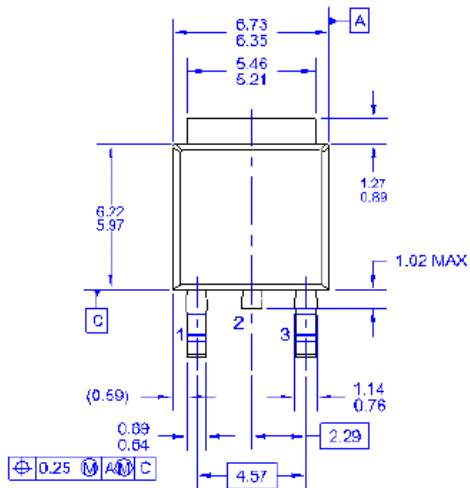
Total Gate Charge Q_{sync}. Test Circuit & Waveforms



$$Q_{sync} = \frac{1}{R_G} \cdot \int V_{R_G}(t) dt$$

Mechanical Dimensions

D-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252 ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A, STD TO220P1003X236-3N.
 H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

Dimensions in Millimeters



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|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
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| AX-CAP™* | Global Power ResourceSM | Programmable Active Droop™ | franchise™ |
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| Build it Now™ | Green FPS™ | QS™ | TinyBuck™ |
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| CTL™ | IntelliMAX™ |  | TinyPower™ |
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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