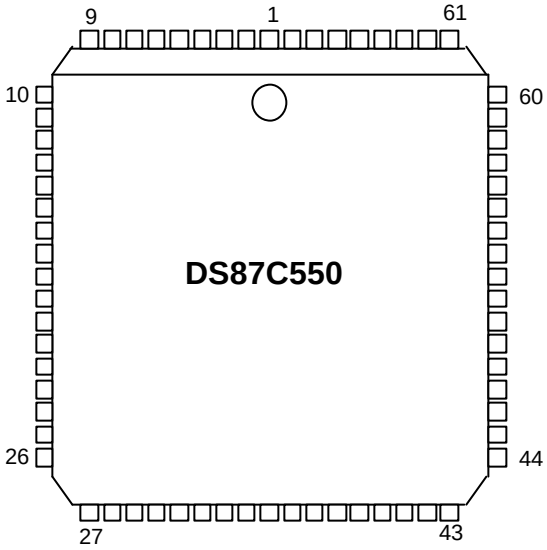
DS87C550

EPROM High-Speed Micro with ADC and PWM

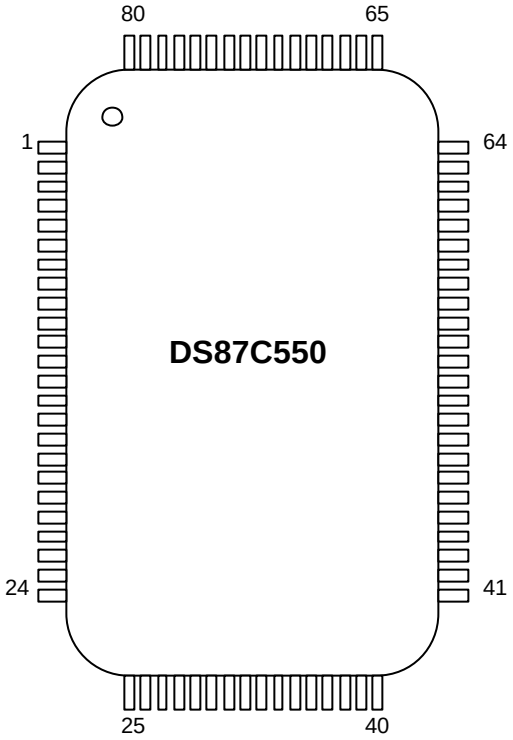
FEATURES

- 87C52-Compatible
  - 8051 pin- and instruction set-compatible
  - Three 16-bit timer/counters
  - 256 bytes scratchpad RAM
- On-chip Memory
  - 8 kB EPROM (OTP & Windowed Packages)
  - 1 kB extra on-chip SRAM for MOVX access
- On-chip Analog to Digital Converter
  - Eight channels of analog input, 10-bit resolution
  - Fast conversion time
  - Selectable internal or external reference voltage
- Pulse-Width Modulator Outputs
  - Four channels of 8-bit PWM
  - Channels cascadable to 16-bit PWM
- Four capture plus three compare registers
- 55 I/O Port Pins
- New Dual Data Pointer Operation
  - Either data pointer can be incremented or decremented
- ROMSIZE Feature
  - Selects effective on-chip ROM size from 0 to 8k
  - Allows access to entire external memory map
  - Dynamically adjustable by software
- High-Speed Architecture
  - 4 clocks/machine cycle (8051 = 12)
  - Runs DC to 33 MHz clock rates
  - Single-cycle instruction in 121 ns
  - New Stretch Cycle feature allows access to fast/slow memory or peripherals
- Unique Power Savings Modes
- EMI Reduction Mode disables ALE when not needed
- High integration controller includes:
  - Power-fail reset
  - Early-warning power-fail interrupt
  - Two full-duplex hardware serial ports
  - Programmable watchdog timer
- 16 total interrupt sources with six external
- Available in 68-pin PLCC, 80-pin PQFP, and 68-pin windowed CLCC

PIN ASSIGNMENT



68-Pin PLCC
68-Pin Windowed CLCC



80-Pin PQFP

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: http://www.maxim-ic.com/errata.

DESCRIPTION

The DS87C550 EPROM High-Speed Micro with ADC and PWM is a member of the fastest 100% 8051-compatible microcontroller family available. It features a redesigned processor core that removes wasted clock and memory cycles. As a result, it executes 8051 instructions up to three times faster than the original architecture for the same crystal speed. The DS87C550 also offers a maximum crystal speed of 33 MHz, resulting in apparent execution speeds of up to 99 MHz.

The DS87C550 uses an industry standard 8051 pin-out and includes standard resources such as three timer/counters, and 256 bytes of scratchpad RAM. This device also features 8 kbytes of EPROM with an extra 1 kbyte of data RAM (in addition to the 256 bytes of scratchpad RAM), and 55 I/O ports pins. Both One-Time-Programmable (OTP) and windowed packages are available.

Besides greater speed, the DS87C550 includes a second full hardware serial port, seven additional interrupts, a programmable watchdog timer, brownout monitor, and power-fail reset.

The DS87C550 also provides dual data pointers (DPTRs) to speed block data memory moves. The user can also dynamically adjust the speed of external accesses between two and 12 machine cycles for flexibility in selecting memory and peripherals.

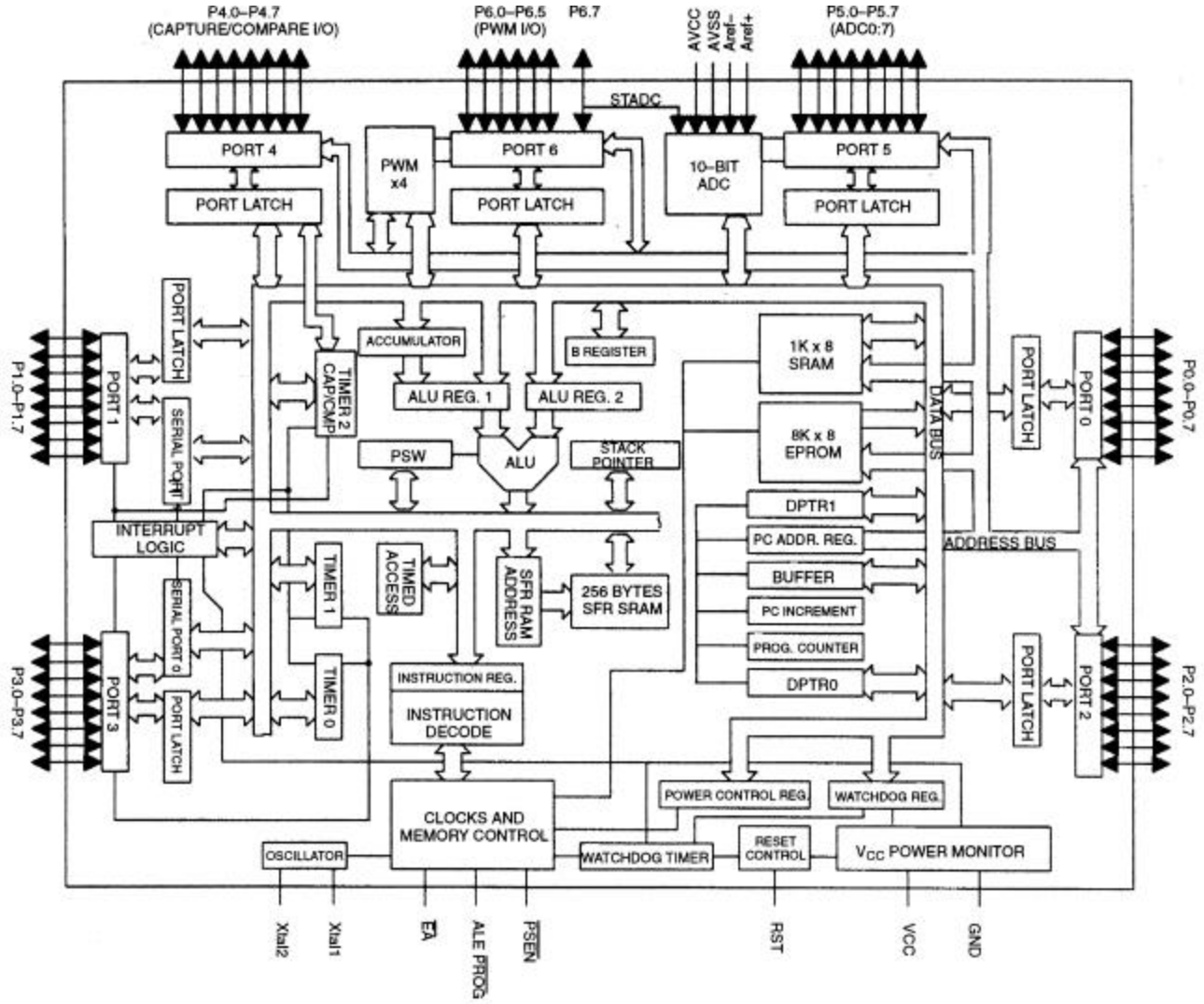
Power Management Mode (PMM) is useful for portable or battery-powered applications. This feature allows software to select a lower speed clock as the main time base. While normal operation has a machine cycle rate of 4 clocks per cycle, the PMM allows the processor to run at 1024 clocks per cycle. For example, at 12 MHz, standard operation has a machine cycle rate of 3 MHz. In Power Management Mode, software can select an 11.7 kHz (12 MHz/1024) machine cycle rate. There is a corresponding reduction in power consumption due to the processor running slower.

The DS87C550 also offers two features that can significantly reduce electromagnetic interference (EMI). One EMI reduction feature allows software to select a reduced emission mode that disables the ALE signal when it is unneeded. The other EMI reduction feature controls the current to the address and data pins interfacing to external devices producing a controlled transition of these signals.

ORDERING INFORMATION

PART NUMBER	PACKAGE	MAX. CLOCK SPEED	TEMPERATURE RANGE
DS87C550-QCL	68-pin PLCC	33 MHz	0°C to +70°C
DS87C550-FCL	80-pin PQFP	33 MHz	0°C to +70°C
DS87C550-QNL	68-pin PLCC	33 MHz	-40°C to +85°C
DS87C550-FNL	80-pin PQFP	33 MHz	-40°C to +85°C
DS87C550-KCL	68-pin windowed CLCC	33 MHz	0°C to 70°C

DS87C550 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION Table 1

PLCC/ CLCC	QFP	SIGNAL NAME	DESCRIPTION
2	72	V_{CC}	**V_{CC} -** Digital +5V power input.
36 37	34 35	GND	**GND –** Digital ground.
15	9	RST	**RST - I/O.** The RST input pin contains a Schmitt voltage input to recognize external active high Reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external Reset sources. An RC is not required for power-up, as the DS87C550 provides this function internally. This pin also acts as an output when the source of the reset is internal to the device (i.e., watchdog timer, power-fail, or crystal-fail detect). In this case, the RST pin will be held high while the processor is in a Reset state, and will return to low as the processor exits this state. When this output capability is used, the RST pin should not be connected to an RC network or a logic output driver.
35 34	32 31	XTAL1 XTAL2	**Input** - The crystal oscillator pins XTAL1 and XTAL2 provide support for fundamental mode, parallel resonant, AT cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 serves as the output of the crystal amplifier. Note that this output cannot be used to drive any additional load when a crystal is attached as this can disturb the oscillator circuit.
47	48	$\overline{\text{PSEN}}$	**$\overline{\text{PSEN}}$ - Output.** The Program Store Enable output. This signal is commonly connected to optional external ROM memory as a chip enable. $\overline{\text{PSEN}}$ will provide an active low pulse during a program byte access, and is driven high when not accessing external program memory.
48	49	ALE	**ALE - Output.** The Address Latch Enable output functions as a clock to latch the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE is driven high when the DS87C550 is in a Reset condition. ALE can also be disabled and forced high using the EMI reduction mode ALEOFF.
49	50	$\overline{\text{EA}}$	**$\overline{\text{EA}}$ - Input.** An active low input pin that when connected to ground will force the DS87C550 to use an external program memory. The internal RAM is still accessible as determined by register settings. $\overline{\text{EA}}$ should be connected to V_{CC} to use internal program memory. The input level on this pin is latched at reset.
16-23	10-17	P1.0-P1.7	**Port 1 - I/O.** Port 1 functions as both an 8-bit, bi-directional I/O port and an alternate functional interface for several internal resources. The reset condition of Port 1 is all bits at logic 1. In this state, a weak pullup holds the port high. This condition allows the pins to serve as both input and output. Input is possible since any external circuit whose output drives the port will overcome the weak pullup. When software writes a 0 to any Port 1 pin, the DS87C550 will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again returns to a weakly held high output (and input) state. The alternate functions of Port 1 pins are detailed below. Note that when the Capture/Compare functions of timer 2 are used, the interrupt input pins become capture trigger inputs.

		Port	**Alternate Function**
16	10	P1.0	INT2/CT0 External Interrupt 2/Capture Trigger 0
17	11	P1.1	INT3/CT1 External Interrupt 3/Capture Trigger 1
18	12	P1.2	INT4/CT2 External Interrupt 4/Capture Trigger 2
19	13	P1.3	INT5/CT3 External Interrupt 5/Capture Trigger 3
20	14	P1.4	T2 External I/O for Timer/Counter 2
21	15	P1.5	T2EX Timer/Counter 2 Capture/Reload Trigger
22	16	P1.6	RXD1 Serial Port 1 Input
23	17	P1.7	TXD1 Serial Port 1 Output

PLCC/ CLCC	QFP	SIGNAL NAME	DESCRIPTION
50-57	51-58		
57	58	P0.0 (AD0)	**Port 0-I/O - AD0-7.** Port 0 is an open-drain 8-bit, bi-directional general-purpose I/O port. When used in this mode pullup resistors are required to provide a logic 1 output. As an alternate function, Port 0 operates as a multiplexed address/data bus to access off-chip memory or peripherals. In this mode, the LSB of the memory address is output on the bus during the time that ALE is high. When ALE falls to a logic 0, the port transitions to a bi-directional data bus. In this mode, the port provides active high drivers for logic 1 output. The reset condition of Port 0 is tri-state (i.e., the open drain devices are off).
56	57	P0.1 (AD1)	
55	56	P0.2 (AD2)	
54	55	P0.3 (AD3)	
53	54	P0.4 (AD4)	
52	53	P0.5 (AD5)	
51	52	P0.6 (AD6)	
50	51	P0.7 (AD7)	
	38-42		
39-46	45-47		
39	38	P2.0 (A8)	**Port 2-I/O Address A15:A8.** Port 2 functions as an 8-bit bi-directional I/O port or alternately as an external address bus (A15-A8). The reset condition of Port 2 is logic high I/O state. In this state, weak pullups hold the port high allowing the pins to be used as an input or output as described above for Port 1. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external memory or peripherals.
40	39	P2.1 (A9)	
41	40	P2.2 (A10)	
42	41	P2.3 (A11)	
43	42	P2.4 (A12)	
44	45	P2.5 (A13)	
45	46	P2.6 (A14)	
46	47	P2.7 (A15)	
24-31	18-20 23-27	P3.0-P3.7	**Port 3 - I/O.** Port 3 functions as an 8-bit bi-directional I/O port or alternately as an interface for External Interrupts, Serial Port 0, Timer 0 & 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. When functioning as an I/O port, these pins operate as indicated above for Port 1. The alternate modes of Port 3 are detailed below. **Port Alternate Mode** P3.0 RXD0 Serial Port 0 Input P3.1 TXD0 Serial Port 0 Output P3.2 $\overline{INT0}$ External Interrupt 0 P3.3 $\overline{INT1}$ External Interrupt 1 P3.4 T0 Timer 0 External Input P3.5 T1 Timer 1 External Input P3.6 $\overline{WR}$ External Data Memory Write Strobe P3.7 $\overline{RD}$ External Data Memory Read Strobe
24	18		
25	19		
26	20		
27	23		
28	24		
29	25		
30	26		
31	27		
7-14	80 1-2 4-8	P4.0-P4.7	**Port 4 - I/O.** Port 4 functions as an 8-bit bi-directional I/O port or alternately as an interface to Timer 2's Capture Compare functions. When functioning as an I/O port, these pins operate as indicated in the Port 1 description. The alternate modes of Port 4 are detailed below. **Port 4 Alternate Mode** P4.0 CMSR0 Timer 2 compare match set/reset output 0 P4.1 CMSR1 Timer 2 compare match set/reset output 1 P4.2 CMSR2 Timer 2 compare match set/reset output 2 P4.3 CMSR3 Timer 2 compare match set/reset output 3 P4.4 CMSR4 Timer 2 compare match set/reset output 4 P4.5 CMSR5 Timer 2 compare match set/reset output 5 P4.6 CMT0 Timer 2 compare match toggle output 0 P4.7 CMT1 Timer 2 compare match toggle output 1
7	80		
8	1		
9	2		
10	4		
11	5		
12	6		
13	7		
14	8		

PLCC/ CLCC	QFP	SIGNAL NAME	DESCRIPTION
1, 62-68	64-71	P5.0-P5.7	**Port 5 - I/O.** Port 5 functions as an open-drain 8-bit bi-directional I/O port or alternately as an interface to the A/D converter. When used for general purpose I/O, these pins operate in a quasi-bi-directional mode. Writing a logic 1 to these pins (reset condition) will cause them to tri-state. This allows the pins to serve as inputs since the tri-state condition can be driven by an external device. If a logic 0 is written to a pin, it is pulled down internally and therefore serves as an output pin containing a logic 0. Because these pins are open-drain, external pullup resistors are required to create a logic 1 level when they are used as outputs. As an alternate function Port 5 pins operate as the analog inputs for the A/D converter as described below. **Port Alternate Mode**
1	71		P5.0 ADC0 Analog to Digital Converter input channel 0
68	70		P5.1 ADC1 Analog to Digital Converter input channel 1
67	69		P5.2 ADC2 Analog to Digital Converter input channel 2
66	68		P5.3 ADC3 Analog to Digital Converter input channel 3
65	67		P5.4 ADC4 Analog to Digital Converter input channel 4
64	66		P5.5 ADC5 Analog to Digital Converter input channel 5
63	65		P5.6 ADC6 Analog to Digital Converter input channel 6
62	64		P5.7 ADC7 Analog to Digital Converter input channel 7
3-6, 32 33, 38	28, 29 37 74-77	P6.0-P6.5 P6.7	**Port 6 - I/O.** Port 6 functions as an 6-bit bi-directional I/O port or alternately as an interface to the PWM and A/D on-board peripherals. As an I/O port, these pins operate as described in Port 1. The alternate modes of Port 6 are detailed below. **Port Alternate Function**
4	75		P6.0 PWMO0 PWM channel 0 output
5	76		P6.1 PWMO1 PWM channel 1 output
32	28		P6.2 PWMO2 PWM channel 2 output
33	29		P6.3 PWMO3 PWM channel 3 output
6	77		P6.4 PWMC0 PWM0 clock input
38	37		P6.5 PWMC1 PWM1 clock input
3	74		P6.7 STADC External A/D conversion start signal (active low)
59	60	A_{vref+}	**A/D +Reference** - Input. When selected, supplies the positive reference voltage for the A/D converter. This signal should be isolated from digital V_{CC} to prevent noise from affecting A/D measurements.
58	59	A_{vref-}	**A/D -Reference** - Input. When selected, supplies the negative reference voltage for the A/D converter. This signal should be isolated from digital GND to prevent noise from affecting A/D measurements.
61	63	A_{VCC}	**Analog V_{CC}**
60	61	A_{VSS}	**Analog Ground**
	3, 21 22, 30 33, 36 43, 44 62, 73 78, 79	NC	**NC-Reserved.** These pins should not be connected. They are reserved for use with future devices in this family.

COMPATIBILITY

The DS87C550 is a fully static, CMOS 8051-compatible microcontroller designed for high performance. While remaining familiar to 8051 family users, it has many new features. With very few exceptions, software written for existing 8051-based systems works without modification on the DS87C550. The exception is critical timing since the High Speed Micro performs its instructions much faster than the original for any given crystal selection. The DS87C550 runs the standard 8051 family instruction set and is pin-compatible with existing devices with similar features in PLCC or QFP packages.

The DS87C550 provides three 16-bit timer/counters, two full-duplex serial ports, 256 bytes of direct RAM plus 1 kbyte of extra MOVX RAM. I/O ports have the same operation as a standard 8051 product. Timers will default to a 12 clock per cycle operation to keep their timing compatible with original 8051 family systems. However, timers are individually programmable to run at the new 4 clocks per cycle if desired.

The DS87C550 provides several new hardware features implemented by new Special Function Registers. A summary of all SFRs is provided in Table 2.

PERFORMANCE OVERVIEW

The DS87C550 features a high-speed, 8051-compatible core. Higher speed comes not just from increasing the clock frequency, but from a newer, more efficient design.

This updated core does not have the dummy memory cycles that are present in a standard 8051. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the DS87C550, the same machine cycle takes 4 clocks. Thus the fastest instruction, 1 machine cycle, executes three times faster for the same crystal frequency. Note that these are identical instructions. The majority of instructions on the DS87C550 will see the full 3 to 1 speed improvement. However, some instructions will achieve between 1.5 and 2.4 to 1 improvement. Regardless of specific performance improvements, all instructions are faster than the original 8051.

The numerical average of all opcodes gives approximately a 2.5 to 1 speed improvement. Improvement of individual programs will depend on the actual mix of instructions used. Speed sensitive applications would make the most use of instructions that are 3 times faster. However, the sheer number of 3 to 1 improved opcodes makes dramatic speed improvements likely for any arbitrary combination of instructions. These architecture improvements and the sub-micron CMOS design produce a peak instruction cycle in 121 ns (8.25 MIPs). The Dual Data Pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory.

INSTRUCTION SET SUMMARY

All instructions in the DS87C550 perform exactly the same functions as their 8051 counterparts. Their effect on bits, flags, and other status functions is identical. However, the timing of each instruction is different. This applies both in absolute and relative number of clocks.

For absolute timing of real-time events, the timing of software loops can be calculated using a table in the High Speed Micro User's Guide. However, counter/timers default to run at the old 12 clocks per increment. In this way, timer-based events occur at the standard intervals with software executing at higher speed. Timers optionally can run at 4 clocks per increment to take advantage of faster processor operation.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct"

instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C550, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles, but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C550 usually uses one instruction cycle for each instruction byte. Examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the High Speed Micro User's Guide for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C550. This allows the DS87C550 to have many new features but use the same instruction set as the 8051. When writing software to use a new feature, an equate statement defines the SFR to an assembler or compiler. This is the only change needed to access the new function. The DS87C550 duplicates the SFRs contained in the standard 80C52. Table 2 shows the register addresses and bit locations. Many are standard 80C52 registers. The High Speed Micro User's Guide describes all SFRs in full detail.

SPECIAL FUNCTION REGISTER LOCATION: Table 2

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
PORT0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	ID1	ID0	TSL	-	-	-	-	SEL	86h
PCON	SMOD_0	SMOD0	OFDF	OFDE	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh
PORT1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
RCON	-	-	-	-	CKRDY	RGMD	RGSL	BGS	91h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
PMR	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEOFF	DEM1	DME0	9Fh
PORT2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
SADDR0									A1h
SADDR1									A2h
IE	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	A8h
CMPL0									A9h
CMPL1									AAh
CMPL2									ABh
CPTL0									ACh
CPTL1									ADh
CPTL2									AEh
CPTL3									AFh
PORT3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
ADCON1	STRT/BSY	EOC	CONT/SS	ADEX	WCQ	WCM	ADON	WCIO	B2h

SPECIAL FUNCTION REGISTER LOCATION: Table 2 cont'd

REGISTER	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADDRESS
ADCON2	OUTCF	MUX2	MUX1	MUX0	APS3	APS2	APS1	APS0	B3h
ADMSB									B4h
ADLSB									B5h
WINHI									B6h
WINLO									B7h
IP	-	PAD	PS1	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	$\overline{RL2}$	BEh
T2MOD	-	-	-	-	-	-	T2OE	DCEN	BFh
PORT4	CMT1	CMT0	CMSR5	CMSR4	CMSR3	CMSR2	CMSR1	CMSR0	C0h
ROMSIZE	-	-	-	-	-	RMS2	RMS1	RMS0	C2h
PORT5	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	C4h
STATUS	PIP	HIP	LIP	-	SPTA1	SPRA1	SPTA0	SPRA0	C5h
TA									C7h
T2IR	-	CM2F	CM1F	CM0F	IE5/CF3	IE4/CF2	IE3/CF1	IE2/CF0	C8h
CMPH0									C9h
CMPH1									CAh
CMPH2									CBh
CPTH0									CCh
CPTH1									CDh
CPTH2									CEh
CPTH3									CFh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
PW0FG									D2h
PW1FG									D3h
PW2FG									D4h
PW3FG									D5h
PWMADR	ADRS	-	-	-	-	-	PWE1	PWE0	D6h
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	D8h
SBUF1									D9h
PWM0									DCh
PWM1									DDh
PWM2									DEh
PWM3									DFh
ACC									E0h
PW01CS	PW0S2	PW0S1	PW0S0	PW0EN	PW1S2	PW1S1	PW1S0	PW1EN	E1h
PW23CS	PW2S2	PW2S1	PW2S0	PW2EN	PW3S2	PW3S1	PW3S0	PW3EN	E2h
PW01CON	PW0F	PW0DC	PW0OE	PW0T/C	PW1F	PW1DC	PW1OE	PW1T/C	E3h
PW23CON	PW2F	PW2DC	PW2OE	PW2T/C	PW3F	PW3DC	PW3OE	PW3T/C	E4h
RLOADL									E6h
RLOADH									E7h
EIE	ET2	ECM2	ECM1	ECM0	EX5/EC3	EX4/EC2	EX3/EX1	EX2/EC0	E8h
T2SEL	TF2S	TF2BS	-	TF2B	-	-	T2P1	T2P0	EAh
CTCON	$\overline{CT3}$	CT3	$\overline{CT2}$	CT2	$\overline{CT1}$	CT1	$\overline{CT0}$	CT0	EBh
TL2									ECh
TH2									EDh
SETR	TGFF1	TGFF0	CMS5	CMS4	CMS3	CMS2	CMS1	CMS0	EEh
RSTR	CMTE1	CMTE0	CMR5	CMR4	CMR3	CMR2	CMR1	CMR0	EFh
B									F0h
PORT6	STADC	-	PWMC1	PWMC0	PWMO3	PWMO2	PWMO1	PWMO0	F1h
EIP	PT2	PCM2	PCM1	PCM0	PX5/PC3	PX4/PC2	PX3/PC1	PX2/PC0	F8h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	FFh

MEMORY RESOURCES

As is convention within the 8051 architecture, the DS87C550 uses three memory areas. The total memory configuration of the DS87C550 is 8 kbytes of EPROM, 1 kbyte of data SRAM and 256 bytes of scratchpad or direct RAM. The 1 kbyte of data space SRAM is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. The scratchpad area is 256 bytes of register mapped RAM and is identical to the RAM found on the 80C52. There is no conflict or overlap among the 256 bytes and the 1k as they use different addressing modes and separate instructions.

OPERATIONAL CONSIDERATION

The erasure window of the windowed CLCC package should be covered without regard to the programmed/unprogrammed state of the EPROM. Otherwise, the device may not meet the AC and DC parameters listed in the datasheet.

PROGRAM MEMORY

On-chip ROM begins at address 0000h and is contiguous through 1FFFh (8k). Exceeding the maximum address of on-chip ROM will cause the DS87C550 to access off-chip memory. However, the maximum on-chip decoded address is selectable by software using the ROMSIZE feature. Software can cause the DS87C550 to behave like a device with less on-chip memory. This is beneficial when overlapping external memory, such as Flash, is used.

With the ROMSIZE feature the maximum on-chip memory size is dynamically variable. Thus a portion of on-chip memory can be removed from the memory map to access off-chip memory, then restored to access on-chip memory. In fact, all of the on-chip memory can be removed from the memory map, allowing the full 64k memory space to be addressed as off-chip memory. ROM addresses that are larger than the selected maximum are automatically fetched from outside the part via Ports 0 & 2. A depiction of the ROM memory map is shown in Figure 2.

The ROMSIZE register is used to select the maximum on-chip decoded address for ROM. Bits RMS2, RMS1, RMS0 (ROMSIZE2:0) have the following effect.

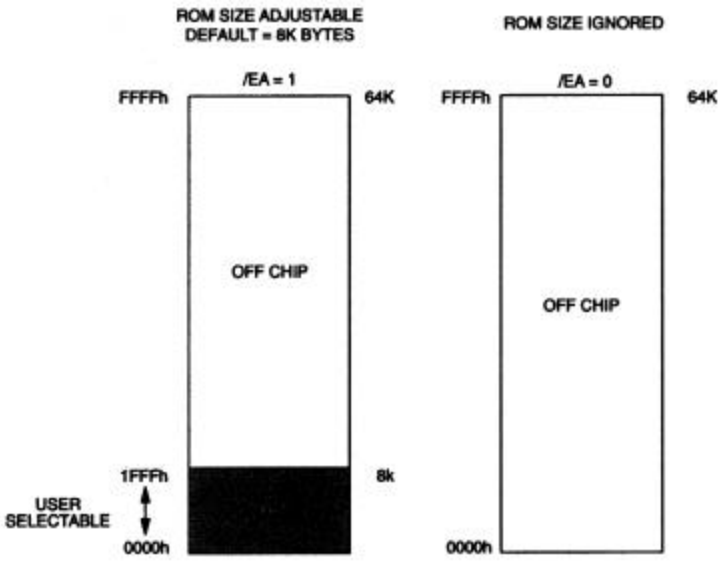
RMS2	RMS1	RMS0	Maximum on-chip ROM Address
0	0	0	0k
0	0	1	1k (0h - 03FFh)
0	1	0	2k (0h - 07FFh)
0	1	1	4k (0h - 0FFFh)
1	**0**	**0**	**8k (0h – 1FFFh) default**
1	0	1	invalid - reserved
1	1	0	invalid - reserved
1	1	1	invalid - reserved

The reset default condition is a maximum on-chip ROM address of 8 kbytes. Thus no action is required if this feature is not used. Therefore when accessing external program memory, the first 8 kbytes would be inaccessible. To select a smaller effective ROM size, software must alter bits RMS2-RMS0. Altering these bits requires a Timed Access procedure as explained below. The ROMSIZE register should be manipulated from a safe area in the program memory map. This is a program memory address that will not be affected by the change. For example, do not select a maximum ROM size of 4k from an internal ROM address of 5k. This would cause the current address to switch from internal to external and potentially cause invalid operation. Similarly, do not instantly switch from external to internal memory.

For example, do not select a maximum ROM address of 8k from an external ROM address of 7k (if ROMSIZE is set for 4k or less).

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not available as I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the EA pin is logic 0. EA overrides all bit settings. The PSEN signal will go active (low) to serve as a chip enable or output enable when Ports 0 & 2 fetch from external ROM.

ROM MEMORY MAP Figure 2



DATA MEMORY

Unlike many 8051 derivatives, the DS87C550 contains additional on-chip data memory. In addition to the standard 256 bytes of data RAM accessed by direct instructions, the DS87C550 contains another 1 kbyte of data memory that is accessed using the MOVX instruction. Although physically on-chip, software treats this area as though it was located off-chip. The 1 kbyte of SRAM is permanently located from address 0000h to 03FFh (when enabled).

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 1k automatically go to external memory through Ports 0 & 2.

When disabled, the 1k memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 & 2. This also is the default condition. This default allows the DS87C550 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using two bits in the Power Management Register (DME1, DME0). This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. These bits have the following operation:

DATA MEMORY ACCESS CONTROL Table 3

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h - FFFFh	External Data Memory *Default condition
0	1	0000h - 03FFh 0400h - FFFFh	Internal SRAM Data Memory External Data Memory
1	0	Reserved	Reserved
1	1	0000h - 03FFh 0400h – FFFBh FFFCh FFFDh - FFFFh	Internal SRAM Data Memory Reserved - no external access Read access to the status of lock bits Reserved

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: bits 2-0 reflect the programmed status of the security lock bits LB2-LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read only.

STRETCH MEMORY CYCLE

The DS87C550 allows software to adjust the speed of off-chip data memory and/or peripheral access by adjusting the number of machine cycles it takes to execute a MOVX instruction. The micro is capable of performing the MOVX in as little as two machine cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally always uses two cycles. However, the time for the instruction execution can be stretched for slower interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory mapped peripherals such as LCDs or UARTs that are slow and require more time to access.

The Stretch MOVX function is controlled by the MD2-MD0 SFR bits in the Clock Control Register (CKCON.2-0) as described below. They allow the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX instruction. A Stretch of 7 will result in a MOVX of 12 machine cycles. Software can dynamically change the stretch value depending on the particular memory or peripheral being accessed. The default stretch of one allows the use of commonly available SRAMs without dramatically lengthening the memory access times.

Note that the STRETCH MOVX function is slightly different in the DS87C550 than in earlier members of the high-speed microcontroller family. In all members of this family (including the DS87C550), increasing the stretch value from 0 to 1 causes setup and hold times to be increased by 1 crystal clock each. In older members of the family, there is no further change in setup and hold times regardless of the number of stretch cycles selected. In the DS87C550 however, when a stretch value of 4 or above is selected, the timing of the interface changes dramatically to allow for very slow peripherals. First, the ALE signal is increased by 1 machine cycle. This increases the address setup time into the peripheral by this amount. Next, the address is held on the bus for one additional machine cycle, increasing the address hold time by this amount. The Read or Write signal is then increased by a machine cycle. Finally, the data is held on the bus (for a write cycle) one additional machine cycle, thereby increasing the data hold time by this amount. For every Stretch value greater than 4, the setup and hold times remain constant, and only the width of the read or write signal is increased.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, the default off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the

Stretch setting. When maximum speed is desired, software should select a Stretch value of 0. When using very slow RAM or peripherals, the application software can select a larger Stretch value. Note that this affects data memory accesses only and that there is no way to slow the accesses to program memory other than to use a slower crystal (or external clock).

The specific timing of the variable speed Stretch MOVX is provided in the Electrical Specifications section of this data sheet. Table 4 shows the resulting MOVX instruction timing and the read or write strobe widths for each Stretch value.

DATA MEMORY CYCLE STRETCH VALUES Table 4

CKCON.2-0			MOVX MACHINE	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH
M2	M1	M0	CYCLES	IN MACHINE CYCLES
0	0	0	2 (forced internal)	0.5
0	0	1	3 (**default** external)	1
0	1	0	4	2
0	1	1	5	3
1	0	0	9	4
1	0	1	10	5
1	1	0	11	6
1	1	1	12	7

Dual Data Pointer With Inc/Dec

The DS87C550 contains several new, unique features that are associated with the Data Pointer register. In the original 8051 architecture, the DPTR was a 16-bit value that was used to address off-chip data RAM or peripherals. To improve the efficiency of data moves, the DS87C550 contains two Data Pointer registers (DPTR0 and DPTR1). By loading one DPTR with the source address and the other with the destination address, block data moves can be made much more efficient. Since DPTR0 is located at the same address as the single DPTR in the original 8051 architecture, code written for the original architecture will operate normally on the DS87C550 with no modification necessary.

The second data pointer, DPTR1 is located at the next two register locations (up from DPTR0) and is selected using the data pointer select bit SEL (DPS.0). If SEL = 0, then DPTR0 is the active data pointer. Conversely, if SEL = 1, then DPTR1 is the active data pointer. Any instruction that reference the DPTR (ex. MOVX A, @ DPTR) refers to the active data pointer as determined by the SEL bit. Since the bit adjacent to SEL in the DPS register is not used, the fastest means of changing the SEL (and thereby changing the active data pointer) is with an INC instruction. Each INC DPS Instruction will toggle the active data pointer.

Unlike the standard 8051, the DS87C550 has the ability to decrement as well as increment the data pointers without additional instructions. When the INC DPTR instruction is executed, the active DPTR is incremented or decremented according to the ID1, ID0 (DPS.7-6), and SEL (DPS.0) bits as shown. The inactive DPTR is not affected.

ID1	ID0	SEL	RESULT OF INC DPTR
X	0	0	INCREMENT DPTR0
X	1	0	DECREMENT DPTR0
0	X	1	INCREMENT DPTR1
1	X	1	DECREMENT DPTR1

Another useful feature of the device is its ability to automatically switch the active data pointer after a DPTR-based instruction is executed. This feature can greatly reduce the software overhead associated with data memory block moves, which toggle between the source and destination registers. When the Toggle Select bit (TSL;DPS.5) is set to 1, the SEL bit (DPS.0) is automatically toggled every time one of the following DPTR related instructions are executed:

- INC DPTR
- MOV DPTR, #data16
- MOVC A, @A+DPTR
- MOVX A, @DPTR
- MOVX @DPTR, A

As a brief example, if TSL is set to 1, then both data pointers can be updated with the two instruction series shown.

```
INC DPTR
INC DPTR
```

With TSL set, the first increment instruction increments the active data pointer, and then causes the SEL bit to toggle making the other DPTR active. The second increment instruction increments the newly active data pointer and then toggles SEL to make the original data pointer active again.

CLOCK CONTROL and POWER MANAGEMENT

The DS87C550 includes a number of unique features that allow flexibility in selecting system clock sources and operating frequencies. To support the use of inexpensive crystals while allowing full-speed operation, a clock multiplier is included in the processor's clock circuit. Also, along with the Idle and power-down (Stop) modes of the standard 80C52, the DS87C550 provides a new Power Management mode. This mode allows the processor to continue instruction execution at a very low speed to significantly reduce power consumption (below even idle mode). The DS87C550 also features several enhancements to Stop mode that make this extremely low power mode more useful. Each of these features is discussed in detail below.

SYSTEM CLOCK CONTROL

As mentioned previously, the DS87C550 contains special clock control circuitry that simultaneously provides maximum timing flexibility and maximum availability and economy in crystal selection. There are two basic functions to this circuitry: a frequency multiplier and a clock divider. By including a frequency multiplier circuit, full-speed operation of the processor may be achieved with a lower frequency crystal. This allows the user the ability to choose a more cost-effective and easily obtainable crystal than would be possible otherwise.

The logical operation of the system clock divide control function is shown in Figure 3. The clock signal from the crystal oscillator (or external clock source) is provided to the frequency multiplier module, to a divide-by-256 module, and to a 3-to-1 multiplexer. The output of this multiplexer is considered the **system clock**. The system clock provides the time base for timers and internal peripherals, and feeds the CPU State Clock Generation circuitry. This circuitry divides the system clock by 4, and it is the four phases of this clock that make up the instruction execution clock. The four phases of a single instruction execution clock are also called a single **machine cycle clock**. Instructions in the DS87C550 all use the machine cycle as the fundamental unit of measure and are executed in from one to five of these machine cycles. It is important to note the distinction between the system clock and the machine cycle clock as they are often confused, creating errors in timing calculations. In performing timing calculations, it is

important to remember that all timers and internal peripherals operate off of some version of the system clock while the instruction execution engine always operates off of the machine cycle clock.

When CD1 and CD0 (PMR.7-6) are both cleared to a logic 0, the multiplexer selects the frequency multiplier output. The frequency multiplier can supply a clock that is 2 times or 4 times the frequency of the incoming signal. If the times-4 multiplier is selected by setting the 4X/$\overline{2X}$ bit (PMR.3) to 1, for example, the incoming signal is multiplied by 4. This 4X clock is then passed through the multiplexer, and then output to the CPU State Clock Generation circuits. These CPU State Clock Generation circuits **always** divide the incoming clock by 4 to arrive at the four states (called a machine cycle) necessary for correct processor operation. In this example, since the clock multiplier multiplies by four and the CPU State Clock Generation circuit divides by 4, the apparent instruction execution speed is 1 external (or crystal oscillator) clock per instruction. If the 4X/$\overline{2X}$ bit is set to 0, then the apparent instruction execution speed is 2 clocks per instruction.

It is important to note that the clock multiplier function does not increase the maximum clock (system clock) rate of the device. The DS87C550 operates at a maximum system clock rate of 33 MHz. Therefore, the maximum crystal frequency is 8.25 MHz when a clock multiplier of 4 is used, and is 16.5 MHz when a clock multiplier of 2 is used. The purpose of the clock multiplier is to simplify crystal selection when maximum processor operation is desired. Specifically, an 8.25 MHz fundamental mode, AT cut, parallel resonant crystal is much easier to obtain than the same crystal at 33 MHz. Most crystals in that frequency range tend to be third overtone type.

As illustrated in Figure 3, the programmable Clock Divide control bits CD1-CD0 (PMR.7-6) provide the processor with the ability to adapt to different crystal (and external clock) frequencies and also to allow extreme division of the incoming clock providing lower power operation when desired. The effect of these bits is shown in Table 5.

CD1:CD0 OPERATION Table 5

CD1	CD0	Instruction Execution
0	0	Frequency multiplier (1 or 2 clocks per machine cycle)
0	1	Reserved
1	**0**	Clock divided by 4 (4 clocks per machine cycle) **Default**
1	1	Clock divided by 1024 (1024 clocks per machine cycle)

Besides the ability to use a multiplied clock signal, the normal mode of operation, i.e. the reset default condition (CD1 = 1, CD0 = 0) passes the incoming crystal or external oscillator clock signal straight through as the system clock. Because of the CPU State Clock generation circuitry's normal divide-by-4 function, the default execution speed of the DS87C550's basic instruction is one-fourth the clock frequency.

The selection of instruction cycle rate takes effect after a delay of one machine cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it may be difficult to conduct serial communication while in divide-by-1024 mode. This is simplified by the use of switchback mode (described later) included on the DS87C550.

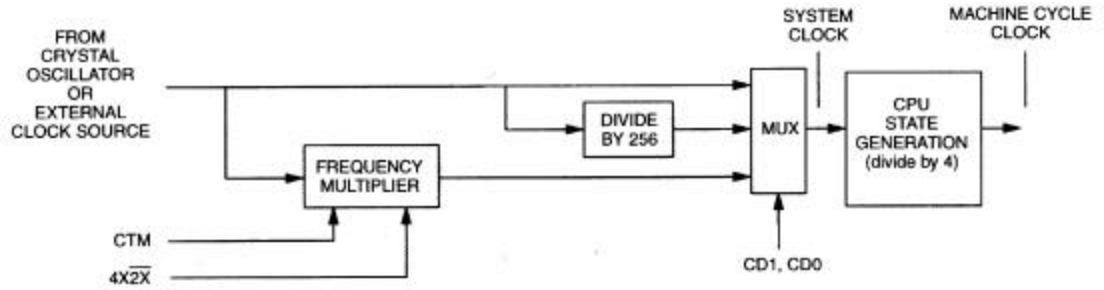
CLOCK SWITCHING RESTRICTIONS

To ensure clean "glitch-free" switching of the system clock and to ensure that all clocks are running and stable before they are used, there are minor restrictions on accessing the clock selection bits CD1:0 and the 4X/$\overline{2X}$ bit.

One restriction is that any change in the CD1 and CD0 bits from a condition other than a 1 0 state (i.e., clock divided by 4 mode) must pass through the divide-by-4 state before proceeding to the desired state. As a specific example, if the clock divisor bits are set to use the frequency multiplier in 4X mode, no other clock setting is possible until after the CD1:0 bits are set to divide-by-4 mode. After setting clock divided-by-4 mode, then clock divided by 1024 can be selected by setting CD1 and CD0 to "11b". Any attempt to change these bits to a disallowed state will be ignored by the hardware.

There are also some minor restrictions when changing from one clock multiplier to another. Changing the clock multiplier can only be performed when the Crystal Multiplier Enable bit CTM (PMR.4) is set to 0. This bit disables the clock multiplication function. However, the CTM bit can only be changed when CD1 and CD0 are set to divide-by-4 mode (i.e., "10b") and the ring mode (RNGMD = RCON.2) bit is 0 (discussed later). Changing the clock multiplication factor also requires that the new frequency be stable prior to effecting the change. The SFR bit CKRDY (RCON.3) indicates the state of the stabilization timeout. Setting the CTM bit to a 0 from a 1 disables the clock multiplier function, automatically clears the CKRDY bit, and starts the stabilization timeout.

SYSTEM CLOCK CONTROL Figure 3



During the stabilization period, CKRDY will remain low, and software will be unable to set the CD1:0 bits to select the frequency multiplier. After the stabilization delay, CKRDY will be set to a 1 by hardware. Note that this bit cannot be set to 1 by software. After hardware sets CKRDY bit, then the CD1:0 bits can be set to use the clock multiplier function. However, before changing CD1:0, the 4X/$\overline{2X}$ bit must be set to the desired state. Following this, the CTM bit must be set to 1 to enable the crystal multiplier. Finally the CD1:0 bits may be set to select the crystal multiplier function. By following this procedure, the processor is guaranteed to receive a stable, glitch-free clock.

OSCILLATOR-FAIL DETECT

The DS87C550 contains a unique safety mechanism called an on-chip Oscillator-Fail Detect circuit. When enabled, this circuit causes the processor to be reset if the oscillator frequency falls below TBD kHz. The processor is held in reset until the oscillator frequency rises above TBD kHz. In operation, this circuit can provide a backup for the watchdog timer. Normally, the watchdog timer is initialized so that it will timeout and will cause a processor reset in the event that the processor loses control. This works perfectly as long as there is a clock from the crystal or external oscillator, but if this clock fails, there is the potential for the processor to fail in an uncontrolled and possibly undesirable state. With the use of the oscillator-fail detect circuit, the processor will be forced to a known state (i.e., reset) even if the oscillator stops.

The oscillator-fail detect circuitry is enabled by software setting the enable bit OFDE (PCON.4) to a 1. Please note that software must use a "Timed Access" procedure (described later) to write to this bit. There is an oscillator-fail detect flag, OFDF (PCON.5), that is set to a 1 by the hardware when it detects an oscillator failure. The processor will be forced into a reset state when this occurs if enabled by OFDE. The oscillator-fail detect flag can only be cleared to a 0 by a power-up reset or by software. It should be noted that the oscillator-fail detect circuitry is not disabled by entering Stop mode. There fore, the user must ensure that this feature is disabled before entering Stop mode.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. Normally, during default operation, the DS87C550 uses 4 clocks per machine cycle. Thus the instruction cycle (machine cycle clock) rate is Clock/4. At 33 MHz crystal speed, the instruction cycle speed is 8.25 MHz. In PMM the microcontroller operates, but from an internally divided version of the clock source. This creates a lower power state without external components. As shown in Figure 3, the system clock may be selected to use the crystal (or external oscillator) frequency divided by 256. This produces a machine cycle that consists of the crystal frequency divided by 1024, which is considered Power Management Mode (PMM). With the processor executing instructions at this much lower rate, a significant amount of power is saved.

Software is the only mechanism to invoke the PMM. Table 6 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM runs very slowly and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 7.

MACHINE CYCLE RATE Table 6

Crystal Speed	Full Operation (4 clocks per machine cycle)	PMM (1024 clocks per machine cycle)
11.0592 MHz	2.765 MHz	10.8 kHz
16 MHz	4.0 MHz	15.6 kHz
25 MHz	6.25 MHz	24.4 kHz
33 Mhz	8.25 MHz	32.2 kHz

OPERATING CURRENT ESTIMATES IN PMM Table 7

Crystal Speed	Full Operation (4 clocks per machine cycle)	PMM (1024 clocks per machine cycle)
11.0592 MHz	13.1 mA	4.8 mA
16 MHz	17.2 mA	5.6 mA
25 MHz	25.7 mA	7.0 mA
33 Mhz	32.8 mA	8.2 mA

Note that PMM provides a lower power condition than Idle mode. This is because in Idle, all clocked functions such as timers run at a rate of crystal divided by 4. Since wakeup from PMM is as fast as or

faster than wakeup from Idle, and since PMM allows the CPU to continue to execute instructions (even if doing NOPs), there is little reason to use Idle in new designs.

Switchback

One of the other unique features included on the DS87C550 is Switchback. Simply, Switchback when enabled will allow serial ports and interrupts to automatically switch back from divide-by-1024 (PMM) to divide-by-4 (standard speed operation). This feature makes it very convenient to use the Power Management Mode in real time applications. Of course to return to a divide-by-4 clock rate from divide-by-1024 PMM, software can simply select the CD1 & CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C550 provides hardware alternatives for automatic Switchback to standard speed operation.

The Switchback feature is enabled by setting the SFR bit SWB (PMR.5) to a 1. Once it is enabled and when PMM is selected, there are two possible events that can cause an automatic switchback to divide-by-4 mode. First, if an interrupt occurs and is set so that it will be acknowledged, this event will cause the system clock to revert from PMM to divide-by-4 mode. For example, if $\overline{\text{INT0}}$ is enabled then Switchback will occur on $\overline{\text{INT0}}$. However, if $\overline{\text{INT0}}$ is not enabled, then activity on $\overline{\text{INT0}}$ will not cause switchback to occur.

A Switchback can also occur when an enabled UART detects the start bit indicating the beginning of an incoming serial character or when the SBUF register is loaded initiating a serial transmission. Note that a serial character's start bit does not generate an interrupt. This occurs only on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception or transmission. So with Switchback enabled and a serial port enabled, the automatic switch to normal speed operation occurs automatically in time to receive or transmit a complete serial character as if nothing special had happened.

Once Switchback causes the processor to make the transition back to divide-by-4 mode, software must modify SFR bits CD1 & CD0 to re-enter Power Management Mode. However, if a serial port is in the process of transmitting or receiving a character, then this change back to PMM will not be allowed as the hardware prevents a write to CD1 & CD0 during any serial port activity.

Since the reception of a serial start bit or an interrupt priority lockout is normally undetectable by software in an 8051, the Status register features several new flags that are useful. These are described below.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C550 supports three levels of interrupt priority. These levels are Power-fail, High, and Low. Status bits STAT.7-5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS.7) is a 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port Zero Receive Activity (SPRA0; STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port Zero Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 (SPRA1) and STATUS.3 (SPTA1) provide the same information for Serial Port 1, respectively. While one of these bits is set, hardware prohibits software from entering PMM (CD1 & CD0 are write-protected) since this would corrupt the corresponding serial transmissions.

IDLE MODE

Setting the LSB of the Power Control register (PCON.0) invokes the Idle mode. Idle will leave internal clocks, serial ports and timers running. Power consumption drops because memory is not being accessed and instructions are not being executed. Since clocks are running, the Idle power consumption is a function of crystal frequency. It should be approximately ½ of the operational power at a given frequency. The CPU can exit the Idle state with any interrupt or a reset. Idle is available for backward software compatibility. However, due to improvements over the original architecture, the processor's power consumption can be reduced to below Idle levels by invoking Power Management Mode (PMM) and running NOPs.

STOP MODE

Setting bit 1 of the Power Control register (PCON.1) invokes the Stop mode. Stop mode is the lowest power state (besides power-off) since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 uA (but is specified in the Electrical Specifications). All processor operation ceases at the end of the instruction that sets PCON.1. The CPU can exit Stop mode from an external interrupt or a reset condition. Internally generated interrupts (timer, serial port, etc.) are not useful since they require clocking activity.

BAND-GAP SELECT

The DS87C550 provides two enhancements to the Stop mode. As described below, the DS87C550 provides a band-gap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the band-gap reference is off while in Stop mode. This mode allows the extremely low-power state mentioned above. A user can optionally choose to have the band-gap enabled during Stop mode. With the band-gap reference enabled, PFI and Power-fail Reset are functional and are valid means for leaving Stop mode. This allows software to detect and compensate for a brownout or power supply sag, even when in Stop mode.

In Stop mode with the band-gap enabled, I_{CC} will be approximately 100 uA compared with 1 uA with the band-gap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the band-gap can remain disabled. Only the most power-sensitive applications should turn off the band-gap, as this results in an uncontrolled power-down condition.

The control of the band-gap reference is located in the Ring Oscillator Control Register (RCON). Setting BGS (RCON.0) to a 1 will keep the band-gap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the band-gap being off during Stop mode. Note that this bit has no control of the reference during full power, PMM, or Idle modes.

RING OSCILLATOR

The second enhancement to Stop mode on the DS87C550 allows an additional power saving option while also making Stop easier to use. This is the ability to start instantly when exiting Stop mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Entering Stop mode turns off the crystal oscillator and all internal clocks to save power. When exiting Stop mode, the external crystal may require up to 10 ms to begin oscillating again. The DS87C550 can eliminate that delay through the use of the internal ring oscillator, resuming operation in less than 100 ns when exiting Stop mode. If a user selects the ring to provide the start-up clock and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65536 crystal clocks) has expired.

The ring oscillator runs at approximately 4 MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. The default state is to exit Stop mode without using the ring oscillator, so action to enable the ring must be taken before entering stop mode.

The Ring Select (RGSL) bit in the RCON register (RCON.1) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57 MHz crystal, this is approximately 18 ms. The processor sets a flag called Ring Mode (RGMD = RCON.2) that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use.

TIMED ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect them against an accidental write operation. The Timed Access procedure prevents an errant processor from accidentally altering a bit that would seriously affect processor operation. The Timed Access procedure requires that the write of a protected bit be preceded by the following instructions:

```
MOV 0C7h, #0AAh
MOV 0C7h, #55h
```

By writing an AAh followed by a 55h to the Timed Access register (location C7h), the hardware opens a three-cycle window that allows software to modify one of the protected bits. If the instruction that seeks to modify the protected bit is not immediately preceded by these instructions, the write will not take effect. The protected bits are:

WDCON.6	POR	Power-On Reset Flag
WDCON.3	WDIF	Watchdog Interrupt Flag
WDCON.1	EWT	Watchdog Reset Enable
WDCON.0	RWT	Reset Watchdog Timer
RCON.0	BGS	Band-Gap Select
ROMSIZE.2	RMS2	Program Memory Select Bit 2

ROMSIZE.1	RMS1	Program Memory Select Bit 1
ROMSIZE.0	RMS0	Program Memory Select Bit 0

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The DS87C550 allows software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to a 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain inactive when performing on-chip memory access. The default state is ALEOFF = 0 so ALE normally toggles at a frequency of XTAL/4.

PERIPHERAL OVERVIEW

The DS87C550 provides several of the most commonly needed peripheral functions in microcomputer-based systems. New functions include a second serial port, power-fail reset, power-fail interrupt flag, and a programmable watchdog timer. In addition, the DS87C550 contains an analog-to-digital converter and four channels of pulse width modulation for industrial control and measurement applications. Each of these peripherals is described below. More details are available in the High-Speed Micro Data Book (or its most recent addendum).

SERIAL PORTS

The DS87C550 provides a serial port (UART) that is identical to the 80C52. In addition, it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.6 (RXD1) and P1.7 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1, SBUF1) to the original. The new serial port can only use Timer 1 for timer generated baud rates.

Control for serial port 0 is provided by the SCON0 register while its I/O buffer is SBUF0. The registers SCON1 and SBUF1 provide the same functions for the second serial port. A full description of the use and operation of both serial ports may be found in the “High-Speed Microcontroller Data Book.”

ANALOG TO DIGITAL CONVERTER

The DS87C550 contains a 10-bit successive approximation analog-to-digital converter. This converter provides eight multiplexed channels of analog input and allows the user to select either an external or internal precision voltage reference to be used for the conversion process. The A/D converter provides true 9-bit accuracy with a total error of less than ±2 LSBs.

The A/D Converter may be disabled to conserve power by writing a 0 to the SFR ADON bit (ADCON1.1). At reset, this is the default condition, and the user must write a 1 to this bit prior to using the A/D Converter.

A/D CONVERTER INPUT

The A/D Converter of the DS87C550 provides eight channels of analog input on device pins ADC7 through ADC0 (P5.7-P5.0). The signals on these pins are input into an analog multiplexer. The magnitude (and polarity) of these signals is limited by the reference voltage used by the converter (see DC

Specifications section). This reference voltage may be selected to be either an internal band-gap voltage (VBG) or an external reference (Avref+, Avref-). This selection is made by writing a 0 (uses internal reference VBG) or writing a 1 (uses external reference (Avref+, Avref-) to the ADRS bit (PWMADR.7). The default reset condition is for the internal reference to be selected.

Selecting a single analog signal for conversion is achieved by software writing the desired channel number (0 through 7) into SFR bits MUX2 through MUX0 bits of the A/D Control Register 2 (ADCON2.6-4). The single output of the multiplexer is then provided to a sample and hold circuit that maintains a steady signal during the conversion process.

A/D CONVERSION PROCESS

The A/D conversion process can be configured for one-shot or continuous mode operation. For one-shot operation, the SFR bit CONT/SS (ADCON1.5) must be a 0. The conversion process is then initiated by software writing a 1 to the STRT/BSY SFR bit (ADCON1.7) if the ADEX (ADCON1.4) bit is a 0. If the ADEX bit is a 1, then the conversion is initiated by an active low signal on the external pin STADC (P6.7). If continuous mode is selected (CONT/SS = 1), then the first conversion is initiated as described above, but another conversion will be automatically started at the completion of the previous conversion.

Once initiated, the conversion process requires 16 A/D clock periods (T_{ACLK}) to complete. Because of the dynamic nature of the converter, the A/D clock period can be no less that 1 us and no more than 6.25 us. This requirement is expressed as follows:

$$1.0\ us <= T_{ACLK} <= 6.25\ us$$

Therefore any single conversion time can range from 16 us minimum to 100 us maximum, depending on the selected A/D clock frequency.

The A/D clock frequency is a function of the processor's machine cycle clock and the A/D clock's prescaler setting as shown by the following equation:

$$T_{ACLK} = T_{MCLK} * (N+1)$$

where N is the prescaler setting in APS3:0.

The processor's machine cycle clock period (T_{MCLK}) is normally the external crystal (or oscillator) frequency multiplied by 4 (but can be affected by the CD1, CD0, and 4X/$\overline{2X}$ bits). The A/D clock period must be set by the user to ensure that it falls within the minimum and maximum values specified above. As an example, assume the processor's crystal frequency is 33 MHz and that the processor is running in a standard divide-by-4 mode. This means that the period of the processors machine cycle clock, i.e., T_{MCLK}, will be (1/33 MHz)*4 or 121.2 ns. If it is assumed that the application requires the fastest possible conversion time, then the desired T_{ACLK} is 1.0 us. The necessary prescale value can then be calculated as:

$$N = (T_{ACLK}/T_{MCLK})-1$$

Therefore for this example, N = 7.25. Since N must be an integer, the value of N must be 8 (rounded up to the next integer). This results in a conversion clock T_{ACLK} = 1.091 us.

The prescaler value must be stored in SFR bits APS3 through APS0 (ADCON2.3-0) to achieve the proper A/D clock. These bits default to 0 on a processor reset, so they must be set as desired by the processor's initialization software.

A/D OUTPUT

There are two SFR locations that contain the result of the A/D conversion process. They are ADMSB (most significant byte) and ADLSB (least significant byte). The ADLSB byte always contains the 8 least significant bits of the 10-bit result. The ADMSB can be configured in two different ways through the use of the SFR bit OUTCF (ADCON2.7). If OUTCF is a 0, then ADMSB contains the 8 most significant bits of the 10-bit conversion (i.e., bits 9-2). If OUTCF is a 1, then ADMSB contains A/D output bits 9-8 (right justified). The upper 6 bits of the register are set to 0 in this case.

The value stored in the output registers is given by the following equation:

$$1024 \times ((Vin - Avref-)/(Avref+ - Avref-))$$

This equation shows that the A/D conversion result is a 10-bit binary number that represents what fraction of the available reference voltage the input signal is. As you can see with a reference voltage of 2.5 volts, the output has a resolution of 2.44 millivolts. This shows that the reference voltage must be very well regulated to ensure satisfactory performance. It should be noted that the output of the A/D conversion process will be "0000000000" for voltages from Avref- to (Avref- +1/2 LSB). In addition, "1111111111" will be output for voltages from (Avref+ - 3/2 LSB) to Avref+.

The DS87C550 offers a unique feature that allows the result of an A/D conversion to be compared with two user-defined values stored in the WINHI and WINLO registers. The results of this comparison will set or clear the WCM (ADCON 1.2) bit, and this bit can be used as a qualifier to the A/D interrupt. This comparison is built into hardware so that this feature is performed without any burden on the software, and A/D results that are not of particular interest to the application can be ignored. Special function registers WINHI and WINLO are loaded by application software with 8-bit numbers that are compared with the 8 MSBs of the A/D result. These user-defined numbers form a range of values, and the A/D result is evaluated to be inside or outside of this range. When WCIO (ADCON.1) is 0, then WCM is set if the A/D result is found to be inside the range. Otherwise WCM is cleared. When WCIO is a 1, then WCM is set if the A/D result is found to be outside the range. Otherwise WCM is cleared. The state of the WCM bit is expressed by the following equation:

$$WCM = WCIO \oplus (WINHI \leq ADMSB) \oplus (WINLO \leq ADMSB)$$

This equation precisely identifies the relationship between the window registers (WINHI and WINLO), the MSB of the A/D conversion (ADMSB), and the WCIO and WCM bits. However by observation, it is not particularly intuitive as to how this interaction works in a practical sense. If the user makes the assumption that the value stored in WINHI is greater that the value stored in WINLO (this is normally but not necessarily the case), then this equation can be simplified to the following two cases:

For WCIO = 0: $WCM = (WINHI > ADMSB) \text{ AND } (ADMSB \geq WINLO)$

For WCIO = 1: $WCM = (WINHI \leq ADMSB) \text{ OR } (ADMSB < WINLO)$

It is clear that these two equations now express the cases where the A/D result is inside the comparison window (WCIO = 0) and outside the comparison window (WCIO = 1). It is important to note the ≤ and ≥ symbols and account for the specific values that are included in the comparison.

There is another SFR bit, WCQ, that further defines the action taken when the WCM is set. If WCQ is 0, then an A/D Interrupt will occur (if enabled) regardless of the comparison results. When WCQ is set to a

1, then an A/D Interrupt will only occur if WCM is set (i.e., the A/D result comparison was true). This feature allows software to respond only to conditions that meet the programmed range.

PULSE WIDTH MODULATION

The DS87C550 contains four independent 8-bit pulse width modulator (PWMs) functions each with independently selectable clock sources. For more precise modulation operations, two 8-bit PWM functions (PWM0 & PWM1 and/or PWM2 & PWM3) can be cascaded together to form a 16-bit PWM function.

The PWM function is divided into three major blocks: a clock prescaler, a clock generator, and a pulse generator. A single prescaler provides selectable clocks of different frequencies to each of the four clock generator blocks. Each clock generator is an 8-bit reloadable counter that determines the repetition rate (frequency) of its associated PWM. Each pulse generator PWM block is an 8-bit timer clocked by the clock generator's output. When this timer reaches zero, the output of the PWM is set to 1. When the timer reaches the user selected PWM match value stored in SFR PWMx, the PWM output is cleared to 0. In this way, the frequency and duty cycle of the PWM is varied under software control.

PWM PRESCALER

The prescaler block of the PWM function accepts as a clock input the system clock provided to the CPU (and other peripherals), and divides it by 1, 4, 16, and 64. Each of these clocks is available at the output of the prescaler, and is provided to all four of the PWM clock generator blocks. The actual clock used by the clock generator block is dependant on the setting of SFR bits PWxS2:0 (where x is the PWM channel number 0-3) located in the PW01CS or PW23CS registers. In addition to selecting one of the prescaler's CPU clock divided outputs, setting PWxS2 to a 1 allows an external clock to be used as an input to the clock generators. The external clocks are input on device pins PWMC0 (P6.4 for PWM0 or PWM1) or PWMC1 (P6.5 for PWM2 or PWM3). Like all other inputs to the 8051, these inputs are synchronized by sampling them using the internal machine cycle clock. Therefore these inputs must be of sufficient duration for the clock to sample them properly (i.e., 2 machine cycles). The complete functionality of the clock selection SFR bits is as follows:

Prescaler Output	**PWxS2:0**
Machine Cycle_Clock/1	000
Machine Cycle_Clock/4	001
Machine Cycle_Clock/16	010
Machine Cycle_Clock/64	011
PWMCx (external)	1xx

In determining the exact frequency output of the prescaler, it is important to note that the machine cycle clock provided to the prescaler is also software-selectable. The machine cycle clock can be the crystal (or oscillator frequency) divided by 1, 2, 4, or 1024 as determined by the CD1:0 and the 4X/$\overline{2X}$ SFR bits (see Clock Divide Control section for details).

PWM CLOCK GENERATOR

The clock generator blocks of the PWM modules are pre-loaded by software with an 8-bit value, and this value determines the frequency or repetition rate of the PWM function. A value of 0 causes the selected

output of the prescaler to be passed directly to the pulse generator function (i.e., divide by 1). A value of FFh passes a clock to the pulse generator function that is the selected prescaler output divided by 256. In general, the clock generators provide a divide by N+1 selectable repetition rate (i.e., frequency) for their PWM channel.

Each clock generator has an associated SFR that contains the 8-bit reload value. These registers are called PW0FG, PW1FG, PW2FG, and PW3FG (see SFR map for addresses). In addition, there is a frequency generator enable bit (PW0EN, PW1EN, PW2EN, & PW3EN) for each of the clock generator blocks that must be set to a 1 before these blocks will function. These bits are set to 0 after all resets so software must set them to 1 to enable the PWM clocks.

The output of the clock generator block is supplied to the input of the pulse generator block.

PWM PULSE GENERATOR

The pulse generator block of the PWM function produces the PWM output signal on device pins PWMO0 (P6.0), PWMO1(P6.1), PWMO2 (P6.2), AND PWMO3 (P6.3). Each of these output bits has an enable bit: PW0OE (PW01CON.5), PW1OE (PW01CON.1), PW2OE (PW23CON.5), and PW3OE (PW23CON.1) that are cleared to 0 on all resets, and must be set to 1 by software before the PWMs will output a signal.

As described earlier, the pulse generator block is basically a free-running timer with a comparison register that is loaded with an 8-bit value by software. The value of this register establishes the duty cycle of the PWM function. The comparison values are stored in SFRs PWM0, PWM1, PWM2, and PWM3 for the respective PWM channels, and it is these values that determine the pulse duration.

Actually, in accessing these specific SFRs, software has access to both the compare registers and the timer registers of the pulse generator blocks. When the PWM Timer/Compare Value Select SFR bits PW0T/C (PW01CON.4), PW1T/C (PW01CON.0), PW2T/C (PW23CON.4), and PW3T/C (PW23CON.0) are cleared to 0, a read or write to the respective PWMx register accesses the compare register. When these bits are set to 1, a read or write accesses the timer value. With the use of these bits, the timers in the pulse generator sections of the PWM functions can be used as general purpose timers if desired.

When the free-running timer of the pulse generator block rolls over from FFh to 00h, the PWM's output is set to a 1. As the timer continues to count up from 0, the output of the PWM is cleared to 0 when the timer value is equal to the comparison register value. This cycle continues automatically without processor intervention until software or a reset changes some condition.

The value of 0 in the comparison register is a special case of each PWM function. Rather than allow a set and a reset of the PWM output bit, special hardware ensures that 0 will be output continuously if 0 is loaded into the compare register.

There are other SFR bits that affect PWM operation for special modes. Bits PW0DC (PW01CON.6), PW1DC (PW01CON.2), PW2DC (PW23CON.6), and PW3DC (PW23CON.2) cause the output of the respective PWM function to be a constant 1. This feature may be useful for driving a fixed DC voltage into any circuitry attached to the PWM output. Bits PW0F (PW01CON.7), PW1F (PW01CON.3), PW2F (PW23CON.7), and PW3F (PW23CON.3) are flags that are set by the hardware when the respective PWM pulse generator timer rolls over from FFh to 0. These flags must be cleared by software to remove their set condition.

16-BIT MODE

For more precise PWM operations, two 8-bit PWMs may be combined into a single 16-bit PWM function. By setting SFR bit PWE0 (PWMADR.0) to a 1, a new 16-bit PWM0 function is formed from the 8-bit PWM functions PWM0 (LSB) and PWM1 (MSB). Similarly, by setting PWE1 (PWMADR.1) to a 1, a new 16-bit PWM1 function is formed from PWM2 (LSB) and PWM3 (MSB). Since each pair of PWMs can be independently configured into a 16-bit arrangement, the user has the option of having four 8-bit PWM functions, two 8-bit PWM functions and a 16-bit PWM function, or two 16-bit PWM functions.

In 16-bit PWM mode, the prescaler operates exactly as it did in 8-bit mode. Its outputs are available to all four clock generator blocks. However in 16-bit mode, the clock generators for 8-bit PWM1 and PWM3 are not functional. The clock for 16-bit PWM0 function is provided by the clock generator for 8-bit PWM0 and the clock for 16-bit PWM1 function is provided by the clock generator for 8-bit PWM2. The SFR bits PW0EN (clock generator enable) and PW0S2:0 (clock select bits) provide the programmable clock controls for 16-bit PWM channel 0, and bits PW2EN and PW2S2:0 provide the programmable clock controls for 16-bit PWM channel 1. The clock divisor values for the 16-bit PWM operating frequency are contained in the PW0FG and PW2FG registers for 16-bit PWM0 and PWM1 (respectively). Note that these registers remain 8-bit values so the clock division remains the same for 16-bit and 8-bit operation.

When in 16-bit mode, the two 8-bit pulse generator timers are concatenated together forming a 16-bit timer. Therefore the pulse generator section of a 16-bit PWM channel has a repetition rate of the input clock divided by 65,536. As in 8-bit mode when the counter reaches 0, the output of the 16-bit PWM channel is set (i.e., logic 1), and when it reaches the pre-loaded match value it is cleared (i.e., logic 0).

GENERAL PURPOSE TIMERS/COUNTERS

The DS87C550 contains three general-purpose timer/ counters. Timers 0 and 1 are standard 8051 16-bit timer/counters with three modes of operation. Each of these devices can be used as a 13-bit timer/counter, 16-bit timer/counter or 8-bit timer/counter with auto-reload. Timer 0 can also operate as two 8-bit timer counters. Each timer can also be used as a counter of external pulses on the corresponding T0 or T1 pin. The mode of operation is controlled by the Timer Mode (TMOD) register. Each timer/counter consists of a 16-bit register in 2 bytes, which can be found in the SFR map as TL0, TH0, TL1, and TH1. These two timers are enabled by the Timer Control (TCON) register. A complete description of use and operation of these timers may be found in the "High-Speed Microcontroller Data Book."

Timer 2 is a true 16-bit timer/counter with several additional features as compared to timers 1 and 0. With a 16-bit reload register (RLOADL, RLOADH), it provides up/down auto-reload timer/counters and timer output clock generation. Timer 2 also supports a capture/compare function. This new feature provides additional timing control capabilities for real-time applications with less CPU intervention. A more detailed description of this capture/compare feature is provided below.

TIMER 2

The selection of a timer or counter function is controlled by the C/$\overline{T2}$ (T2CON.1) bit When C/$\overline{T2}$ is set to 1, Timer 2 acts as a counter where it counts 1 to 0 transitions on the T2 pin. When C/$\overline{T2}$ is cleared to a 0, Timer 2 functions as a timer where it counts the system clock as determined by the T2M bit (CKCON.5) and the clock divide control bits CD1, CD0 (PMR.7:6) and the 4X/$\overline{2X}$ (PMR.3) bit. A prescaler is used to further divide the input clock by a programmable ratio. The prescaler value is programmable to divide by 1, 2, 4, and 8 as defined by the T2P1 and T2P0 (T2SEL.1:0) bits. Timer 2 is enabled by setting bit TR2 (T2CON.2) to a 1, and disabled by clearing it to a 0.

When the LSB of timer/counter 2 (TL2) overflows, flag TF2B (T2SEL.4) is set, and flag TF2 (T2CON.7) is set when the high byte (TH2) overflows. Setting flag TF2 also sets flag TF2B. Even though only one interrupt is available for Timer 2, either or both of these overflows can be programmed to request an interrupt. To enable the interrupt, the Timer 2 interrupt enable bit ET2 (EIE.7) must be set to a 1. The 8-bit overflow interrupt or the 16-bit overflow interrupt is then individually enabled by setting TF2BS (T2SEL.6) or TF2S (T2SEL.7). Since there is only one interrupt vector for both possible Timer 2 interrupts, the interrupt service routine must determine which event caused the interrupt by polling the available flags. For both interrupt flags, software must clear them upon servicing the interrupt. There is no automatic hardware clearing of these flags.

TIMER 2 CAPTURE FEATURE

One of the new features added to Timer 2 is the capture function. The output of Timer 2 is available to four independent 16-bit capture register pairs (CPTH3:CPTL3, CPTH2:CPTL2, CPTH1:CPTL1, & CPTH0:CPTL0). These registers are loaded with the 16-bit value contained in Timer 2 when transitions occur on the corresponding input pin INT5/CT3, INT4/CT2, INT3/CT1 or INT2/CT0 (P1.3, P1.2, P1.1, or P1.0) respectively. When the capture function is not being used, these input pins also serve as external interrupt inputs. The Capture Trigger Control register (CTCON) can be programmed to make the capture occur on a rising edge, a falling edge, or on either a rising or a falling edge on these input pins. The functionality of the CTCON register is illustrated below. Note that the edge sensitivity established by the setting of CTCON bits applies to both the capture function and the external interrupt function of these input pins. This addition allows maximum flexibility in selecting interrupt polarity. Whether these input pins are used as external interrupt inputs or as capture commands, the input will set the appropriate flag in the External Interrupt Flag register (T2IR.3:0) and will create an interrupt if the associated enable in the Extended Interrupt Enable (EIE.3:0) register is set.

CTCON REGISTER FUNCTIONALITY

CTCON.7	$\overline{CT3}$	Capture register 3 triggered by a falling edge on INT5/CT3
CTCON.6	CT3	Capture register 3 triggered by a rising edge on INT5/CT3
CTCON.5	$\overline{CT2}$	Capture register 2 triggered by a falling edge on INT4/CT2
CTCON.4	CT2	Capture register 2 triggered by a rising edge on INT4/CT2
CTCON.3	$\overline{CT1}$	Capture register 1 triggered by a falling edge on INT3/CT1
CTCON.2	CT1	Capture register 1 triggered by a rising edge on INT3/CT1
CTCON.1	$\overline{CT0}$	Capture register 0 triggered by a falling edge on INT2/CT0
CTCON.0	CT0	Capture register 0 triggered by a rising edge on INT2/CT0

TIMER 2 COMPARE FEATURE

Another new feature added to Timer 2 capabilities is the compare function. Prior to enabling this function, the associated compare register pair (CMPH0:CMPL0, CMPH1:CMPL1, CMPH2:CMPL2) is loaded by software with a 16-bit number. Each time Timer 2 is incremented, the contents of these registers are compared with the new value of the timer. When a match occurs, the corresponding interrupt flag (T2IR.6:4) is set to a 1 on the next machine cycle and an interrupt will occur if the corresponding enable bit is set in the Extended Interrupt Enable (EIE.6:4) register. When a match with CMPH0:CMPL0 occurs, port pins P4.0 through P4.5 are set to a 1 if the corresponding bits of the Set Enable register (SETR) are at logic 1. If the match is with CMPH1:CMPL1, port pins P4.0 through P4.5 are reset to 0 when the corresponding bits in the reset/toggle enable register RSTR are at logic 1. A match with CMPH2:CMPL2 toggles port pins P4.6 and 4.7 if the corresponding bits in the RSTR register are at logic 1. Note that for the toggle function it is not the port pin latch that is actually toggled. Instead, separate flip-flops output the SFR bits TGFF1 and TGFF0 that actually determine the state of the respective port

pin. A 0 in a bit position in either the SETR or the RSTR register disables the corresponding port pin function. The functionality of the SETR and RSTR registers is shown below.

SETR REGISTER FUNCTIONALITY

SETR.7	TGFF1	This bit toggles if CMPH2:CMPL2 and Timer 2 match and CMTE1 is 1
SETR.6	TGFF0	This bit toggles if CMPH2:CMPL2 and Timer 2 match and CMTE0 is 1
SETR.5	CMS5	If 1 then P4.5 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.4	CMS4	If 1 then P4.4 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.3	CMS3	If 1 then P4.3 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.2	CMS2	If 1 then P4.2 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.1	CMS1	If 1 then P4.1 is set on a match between CMPH0:CMPL0 and Timer 2
SETR.0	CMS0	If 1 then P4.0 is set on a match between CMPH0:CMPL0 and Timer 2

RSTR REGISTER FUNCTIONALITY

RSTR.7	CMTE1	If 1 then P4.7 toggles on a match between CMPH2:CMPL2 and Timer 2
RSTR.6	CMTE0	If 1 then P4.6 toggles on a match between CMPH2:CMPL2 and Timer 2
RSTR.5	CMR5	If 1 then P4.5 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.4	CMR4	If 1 then P4.4 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.3	CMR3	If 1 then P4.3 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.2	CMR2	If 1 then P4.2 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.1	CMR1	If 1 then P4.1 is reset on a match between CMPH1:CMPL1 and Timer 2
RSTR.0	CMR0	If 1 then P4.0 is reset on a match between CMPH1:CMPL1 and Timer 2

WATCHDOG TIMER

The free-running watchdog timer, if enabled, will set a flag and cause a reset if not restarted by software within the user selectable timeout period.

A typical application is to allow the flag to cause a reset. When the watchdog times out, it sets the Watchdog Timer Reset Flag (WTRF=WDCON.2) which generates a reset if enabled by the Enable Watchdog Timer Reset (EWT=WDCON.1) bit. In this way if the code execution goes awry and software does not reset the watchdog as scheduled, the processor is put in a known good state: reset.

In a typical initialization, software selects the desired timeout period using the WD1:0 and the system clock control bits. Then, it resets the timer and enables the processor reset function. After enabling the processor reset function, software must then reset the timer before its timeout period or hardware will reset the CPU. Both the EWT and the Watchdog Reset control (RWT = WDCON.0) bits are protected by a Timed Access circuit. This prevents errant software from accidentally clearing the watchdog.

The watchdog timer is controlled by the Clock Control (CKCON) and the Watchdog Control (WDCON) SFRs. CKCON.7 and CKCON.6 are WD1 and WD0 respectively, and they select the watchdog timeout period. Of course, the 4X/$\overline{2X}$ (PMR.3) and CD1:0 (PMR.7:6) system clock control bits also affect the timeout period. Selection of timeout is shown in Table 8.

WATCHDOG TIMEOUT VALUES Table 8

		INTERRUPT TIMEOUT (CLOCKS)				RESET TIME-CLOCKS			
4X/ $\overline{2X}$	CD1:0	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11	WD1:0=00	WD1:0=01	WD1:0=10	WD1:0=11
1	00	2^{15}	2^{18}	2^{21}	2^{24}	2^{15}+512	2^{18}+512	2^{21}+512	2^{24}+512
0	00	2^{16}	2^{19}	2^{22}	2^{25}	2^{16}+512	2^{19}+512	2^{22}+512	2^{25}+512
x	01	2^{17}	2^{20}	2^{23}	2^{26}	2^{17}+512	2^{20}+512	2^{23}+512	2^{26}+512
x	10	2^{17}	2^{20}	2^{23}	2^{26}	2^{17}+512	2^{20}+512	2^{23}+512	2^{26}+512
x	11	2^{25}	2^{28}	2^{31}	2^{34}	2^{25}+512	2^{28}+512	2^{31}+512	2^{34}+512

The watchdog timer uses the internal system clock as a time base so its timeout periods are very accurate. From the table, it can be seen that for a 33 MHz crystal frequency, the watchdog timer is capable of producing timeout periods from 3.97 ms (2^{17} * 1/33 MHz) to over two seconds (2.034 = 2^{26} * 1/33 MHz) with the default setting of CD1:0 (=10). This wide variation in timeout periods allows very flexible system implementation.

In a typical initialization, the user selects one of the possible counter values to determine the timeout. Once the counter chain has completed a full count, hardware will set the interrupt flag (WDIF=WDCON.3). There is no hardware support for a watchdog interrupt, but this flag may be polled to determine if the timeout period has been completed. Regardless of whether the software makes use of this flag, there are then 512 docks left until the reset flag (WTRF=WDCON.2) is set. Software can enable (1) or disable (0) the reset using the Enable Watchdog Reset (EWT=WDCON.1) bit. Note that the watchdog is a free running timer and does not require an enable.

POWER-FAIL RESET

The DS87C550 incorporates an internal precision band-gap voltage reference which, when coupled with a comparator circuit, provides a full power-on and power-fail reset function. This circuit monitors the processor's incoming power supply voltage (V_{CC}) and holds the processor in reset while V_{CC} is out of tolerance. Once V_{CC} has risen above V_{RST}, the DS87C550 will restart the oscillator for the external crystal and count 65,536 clock cycles before program execution begins at location 0000h. This power supply monitor will also invoke the reset state when V_{CC} drops below the threshold condition. This reset condition will remain while power is below the minimum voltage level. When power exceeds the reset threshold, a full power-on reset will be performed. In this way, this internal voltage monitoring circuitry handles both power-up and power down conditions without the need for additional external components.

The processor exits the reset condition automatically once V_{CC} meets V_{RST}. This helps the system maintain reliable operation by only permitting processor operation when its supply voltage is in a known good state. Software can determine that a Power-On Reset has occurred by checking the Power-On Reset flag (POR=WDCON.6). Software should clear the POR bit after reading it.

The Reset pin of the DS87C550 is both an input and an output. When the processor is being held in reset by the power-fail detection circuitry, the reset pin will be actively pulled high by the processor, and can therefore be used as an input to other external devices.

POWER-FAIL INTERRUPT

The band-gap voltage reference that sets a precise reset threshold also generates an optional early warning Power-fail Interrupt (PFI). When enabled by software, the processor will vector to ROM address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (EPFI=WDCON.5). Setting this bit to a logic 1 will enable the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and software must manually clear it.

INTERRUPTS

The DS87C550 provides 16 interrupt sources with three priority levels. The Power-fail Interrupt (PFI) has the highest priority. All interrupts, with the exception of the Power-fail Interrupt, are controlled by a series combination of individual enable bits and a global interrupt enable EA (IE.7). Setting EA to a 1 allows individual interrupts to be enabled. Clearing EA disables all interrupts regardless of their individual enable settings.

The three available priority levels are low, high, and highest. The highest priority level is reserved for the Power-Fail Interrupt only. All other interrupt priority levels have individual priority bits that when set to a 1 establish the particular interrupt as high priority. In addition to the user selectable priorities, each interrupt also has an inherent or "natural priority". Given that all interrupt sources maintain the default low priority, the natural priority determines the priority of simultaneously occurring interrupts. The available interrupt sources, their flags, their enables their natural priority, and their available priority selection bits are identified in Table 9.

INTERRUPT SOURCES AND PRIORITIES Table 9

NAME	DESCRIPTION	VECTOR	NATURAL PRIORITY	FLAG BIT	ENABLE BIT	PRIORITY CONTROL BIT
PFI	Power Fail Interrupt	33h	0	PFI(WDCON.4)	EPFI(WDCON.5)	N/A
$\overline{\text{INT0}}$	External Interrupt 0	03h	1	IEO(TCON.1)	EX0(IE.0)	PX0(IP.0)
SCON1	TI1 or RI1 from serial port 1	0Bh	2	RI_1(SCON1.0) TI_1(SCON1.1)	ES1(IE.5)	PS1(IP.5)
A/D	A/D Converter Interrupt	13h	3	EOC(ADCON1.6)	EAD(IE.6)	PAD(IP.6)
TF0	Timer 0	1Bh	4	TF0(TCON.5)	ET0(IE.1)	PT0(IP.1)
INT2/CF0	External Interrupt 2 or Capture 0	23h	5	IE2/CF0(T2IR.0)	EX2/EC0(EIE.0)	PX2/PC0(EIP.0)
CM0F	Compare Match 0	2Bh	6	CM0F(T2IR.4)	ECM0(EIE.4)	PCM0(EIP.4)
$\overline{\text{INT1}}$	External Interrupt 1	3Bh	7	IE1(TCON.3)	EX1(IE.2)	PX1(IP.2)
INT3/CF1	External Interrupt 3 or Capture 1	43h	8	IE3/CF1(T2IR.1)	EX3/EC1(EIE.1)	PX3/PC1(EIP.1)
CM1F	Compare Match 1	4Bh	9	CM1F(T2IR.5)	ECM1(EIE.5)	PCM1(EIP.5)
TF1	Timer 1	53h	10	TF1(TCON.7)	ET1(IE.3)	PT1(IP.3)
INT4/CF2	External Interrupt 4 or Capture 2	5Bh	11	IE4/CF2(T2IR.2)	EX4/EC2(EIE.2)	PX4/PC2(EIP.2)
CM2F	Compare Match 2	63h	12	CM2F(T2IR.6)	ECM2(EIE.6)	PCM2(EIP.6)
SCON0	TI0 or RI0 from serial port 0	6Bh	13	RI_0(SCON0.0) TI_0(SCON0.1)	ES0(IE.4)	PS0(IP.4)
INT5/CF3	External Interrupt 5 or Capture 3	73h	14	IE5/CF3(T2IR.3)	EX5/EC3(EIE.3)	PX5/PC3(EIP.3)
TF2	Timer 2	7Bh	15	TF2(TCON.7) TF2B(T2SEL.4)	ET2(EIE.7)	PT2(EIP.7)

EPROM PROGRAMMING

The DS87C550 follows 8-kbyte EPROM standards for the 8051 family. It is available in a UV erasable, ceramic windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options.

PROGRAMMING PROCEDURE

The DS87C550 should run from a clock speed between 4 and 6 MHz when programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 10. The diagram in Figure 5 shows the expected electrical connection for programming. Note that the programmer must

apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the Electrical Specifications.

Program the DS87C550 as follows:

1. Apply the address value.
2. Apply the data value.
3. Select the programming option from Table 10 using the control signals.
4. Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM.
5. Pulse the $\overline{PROG}$ signal 5 times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits.
6. Repeat as many times as necessary.

EPROM PROGRAMMING MODES Table 10

MODE		RST	$\overline{PSEN}$	ALE/ $\overline{PROG}$	EA/ V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	PL5*	12.75 V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0-3Fh		H	L	PL25*	12.75 V	L	H	H	L	H
Program Lock Bits	LB1	H	L	PL25*	12.75 V	H	H	H	H	H
	LB2	H	L	PL25*	12.75 V	H	H	H	L	L
	LB3	H	L	PL25*	12.75 V	H	L	H	H	L
Program Option Register Address FCh		H	L	PL25*	12.75 V	L	H	H	L	L
Read Signature or Option Register 30, 31, 60, FCh		H	L	H	H	L	L	L	L	L

*PLn indicates pulse to a logic low n times

EPROM LOCK BITS Table 11

Level	Lock Bits			Protection
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted; verify if Encryption table was programmed.
2	P	U	U	Prevent MOVC instructions in external memory from reading program bytes in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevents MOVX instructions in external memory from reading SRAM (MOVX) in internal memory.
4	P	P	P	Level 3 plus no external execution.

SECURITY OPTIONS

The DS87C550 employs a standard three-level lock that restricts viewing of the EPROM contents. A 64-byte Encryption Array allows the authorized user to verify memory by presenting the data in encrypted form.

Lock Bits

The security lock consists of 3 lock bits. These bits select a total of four levels. Higher levels provide increasing security but also limit application flexibility. Table 11 shows the security settings. Note that the programmer cannot directly read the state of the security lock.

Encryption Array

The Encryption Array allows an authorized user to verify EPROM without allowing the true memory to be dumped. During a verify operation, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the EPROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the verify value will be encrypted.

For encryption to be effective, the Encryption Array must be unknown to the party that is trying to verify memory. The entire EPROM also should be a non-FFh state or the Encryption Array can be discovered.

The Encryption Array is programmed as shown in Table 10. Note that the programmer cannot read the array. Also note that the verify operation always uses the Encryption Array. The array has no impact while FFh. Simply programming the array to a non-FFh state will cause the encryption to function.

EPROM ERASURE CHARACTERISTICS

Erasure of the information stored in the DS87C550's EPROM occurs when the isolated gate structure of the EPROM stage element is exposed to certain wavelengths of light. While the gate structure is to some degree sensitive to a wide range of wavelengths, it is mostly wavelengths shorter than approximately 4,000 angstroms that are most effective in erasing the EPROM. Since fluorescent lighting and sunlight have wavelengths in this range, they can cause erasure if the device is exposed to them over an extended period of time (weeks for sunlight, years in room-level fluorescent light). For this reason (and others mentioned previously), it is recommended that an opaque covering be placed over the window of the -K (windowed PLCC) package type.

For complete EPROM erasure, exposure to ultraviolet light at approximately 2537 angstroms to a dose of 15W-sec/cm^2 at minimum is recommended. In practice, exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes at a distance of approximately 1 inch will normally be sufficient.

OTHER EPROM OPTIONS

The DS87C550 has user-selectable options that must be set before beginning software execution. These options use EPROM bits rather than SFRs.

The EPROM selectable options may be programmed as shown in Table 10. The Option Register sets or reads these selections. The bits in the Option Register have the following function:

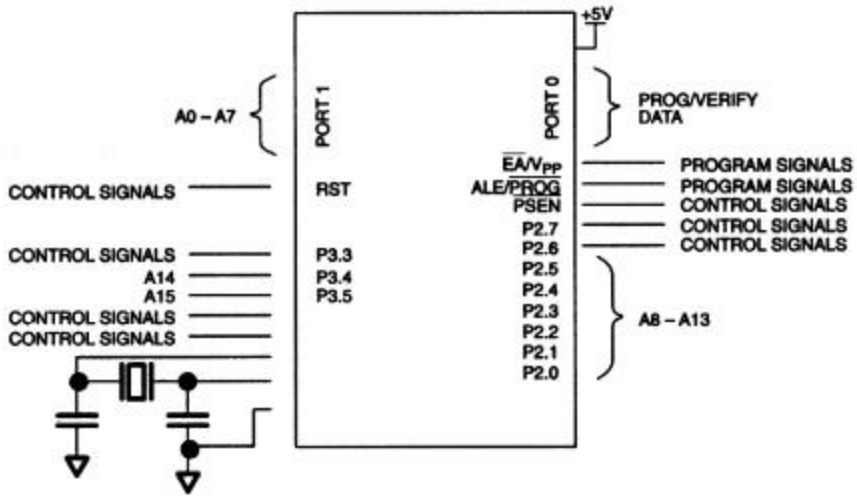
Bit 7 -4 Reserved. Program to a 1.
Bit 3 Watchdog POR default. Set to 1:
Watchdog reset function is disabled on power-up. Set to 0: Watchdog reset function is enabled automatically.
Bit 2-0 Reserved. Program to a 1.

SIGNATURE

The Signature bytes identify the product and programming revision to EPROM programmers. This information is located at programming addresses 30h, 31h, and 60h. This information is as follows:

Address	Value	Meaning
30h	DAh	Manufacturer
31h	55	Model
60h	00	Extension

EPROM PROGRAMMING CONFIGURATION Figure 5



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-0.3V to (V_{CC} +0.5V)
Voltage on V_{CC} Relative to Ground	-0.3V to 6.0V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	160°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Power-fail Warning	V_{PFW}	4.25	4.38	4.5	V	1
Minimum Operating Voltage	V_{RST}	4.0	4.13	4.25	V	1
Supply Current Active Mode	I_{CC}		30		mA	2
Supply Current Idle Mode	I_{IDLE}		15		mA	3
Supply Current Stop Mode	I_{STOP}		1		µA	4
Supply Current Stop Mode W Band-gap	I_{SPBG}		100		µA	4
Input Low Level	V_{IL}	-0.3		+0.8	V	1
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	1
Input High Level XTAL2 and RST	V_{IH2}	3.5		V_{CC}+0.3	V	1
Output Low Voltage Ports 1, 3, 4, 5, 6 @ I_{OL} = 1.6 mA	V_{OL1}		0.15	0.45	V	1
Output Low Voltage Ports 0, 2, $\overline{ALE}$, $\overline{PSEN}$ @ I_{OL} = 3.2 mA	V_{OL2}		0.15	0.45	V	1
Output High Voltage Ports 1, 2, 3, 4, 6, ALE, $\overline{PSEN}$ @ I_{OH} = -50 µA	V_{OH1}	2.4			V	1, 6
Output High Voltage Ports 1, 2, 3, 4, 6, @ I_{OH} = -1.5 mA	V_{OH2}	2.4			V	1, 7
Output High Voltage Ports 0, 2, 5, ALE, $\overline{PSEN}$ in Bus Mode I_{OH} = -8 mA	V_{OH3}	2.4			V	1, 5
Input Low Current Ports 1, 2, 3 @ 0.45V	I_{IL}			-55	µA	11
Transition Current from 1 to 0 Ports 1, 2, 3 @ 2V	I_{TL}			-650	µA	8
Input Leakage Port 0, 5 and $\overline{EA}$	I_L	-10		+10	µA	10

DC ELECTRICAL CHARACTERISTICS

Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	9
RST Pulldown Resistance	R_{RST}	50		170	kO	

NOTES FOR DS87C550 DC ELECTRICAL CHARACTERISTICS:

All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

1. Voltage referenced to digital ground (GND).

2. Active current measured with 33 MHz clock source on XTAL1, V_{CC}=RST=5.5V, other pins disconnected.

3. Idle mode current measured with 33 MHz clock source on XTAL1, V_{CC}=5.5V, RST at ground, other pins disconnected.

4. Stop mode current measured with XTAL1 and RST grounded, V_{CC}=5.5V, all other pins disconnected. This value is not guaranteed. Users that are sensitive to this specification should contact Dallas Semiconductor for more information.

5. When addressing external memory.

6. RST=V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tristated in reset and when at a logic high state during I/O mode.

7. During a 0 to 1 transition, a one-shot drives the ports hard for two oscillator clock cycles. This measurement reflects port in transition mode.

8. Ports 1, 2, 3, 5, 6 source transition current when being pulled down externally. Current reaches its maximum at approximately 2V.

9. 0.45<Vin<V_{CC}. Not a high impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

10. 0.45<Vin<V_{CC}. RST=V_{CC}. This condition mimics operation of pins in I/O mode.

11. This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(@ V_{CC} = 5V ± 10%, 0-70ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Analog Supply Voltage	A_{VCC} A_{VSS}	V_{CC} GND		V_{CC} GND	V	
Analog Supply Current	AI_{DD}			1	mA	
Analog Idle Mode Current	AI_{DDI}			TBD	µA	
Analog Power-Down Mode Current	AI_{DDPD}			300	nA	
Analog Input Voltage Internal Reference External Reference	ADC7-ADC0	0 A_{VREF-}		2.50 A_{VREF+}	V	
External Analog Reference Voltage	A_{VREF-} A_{VREF+}	AV_{SS}-0.2		AV_{CC} + 0.2	V	
Internal Reference Voltage Change with Temperature Change with AV_{CC}	V_{BG} V_{BGT} V_{BGV}	2.4375	2.50 ± 50 ± 10	2.5625	V PPM/°C mV/V	
Analog Input Capacitance	C_{IN}		10	15	PF	
A/D Clock	t_{ACLK}	1		6.25	us	2
Sampling Time	t_{ADS}	5 t_{ACLK}			t_{ACLK}	
Conversion Time	t_{ADC}	16 t_{ACLK}			t_{ACLK}	3
Resolution				10	Bits	
Differential non-linearity	E_{DL}			±1.0	LSB	
Integral non-linearity	E_{IL}			±2.0	LSB	
Offset Error	E_{OS}			±2.0	LSB	
Gain Error	E_G			±1.0	%	
Cross-talk between A/D inputs	E_{CT}			-60	dB	

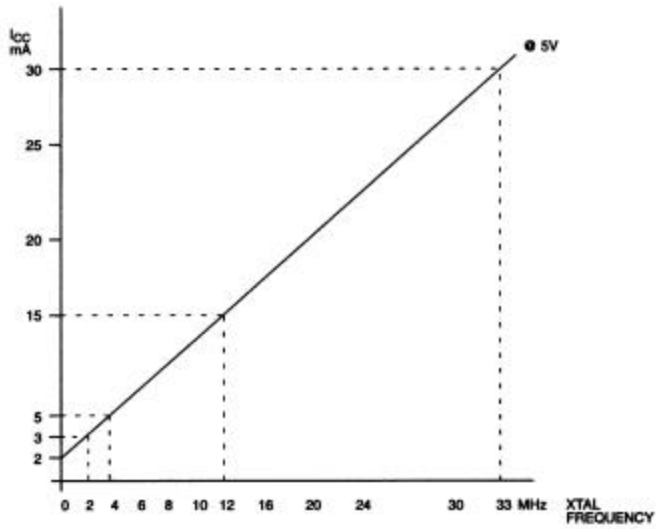
NOTES FOR A/D CONVERTER ELECTRICAL CHARACTERISTICS

1. The following condition must not be exceeded: GND-0.2V < AV_{SS} < V_{CC} + 0.2V.

2. Due to the dynamic nature of the A/D converter, t_{ACLK} has both min and max specifications.

3. A complete conversion cycle requires 16 ACLK periods, including five input sampling periods.

TYPICAL I_{CC} VERSUS FREQUENCY



AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	33 MHz		VARIABLE CLOCK		UNITS
		MIN	MAX	MIN	MAX	
Oscillator Freq. (Ext. Osc.) (Ext. Crystal)	$1/t_{CLCL}$	0 1	33 33	0 1	33 33	MHz
ALE Pulse Width	t_{LHLL}	40		0.375 t_{MCS} -5		ns
Port 0 Address Valid to ALE Low	t_{AVLL}	10		0.125 t_{MCS} -5		ns
Address Hold after ALE Low	t_{LLAX1}	10		0.125 t_{MCS} -5		ns
ALE Low to Valid Instruction In	t_{LLIV}		56		0.625 t_{MCS} -20	ns
ALE Low to $\overline{\text{PSEN}}$ Low	t_{LLPL}	10		0.125 t_{MCS} -5		ns
$\overline{\text{PSEN}}$ Pulse Width	t_{PLPH}	55		0.5 t_{MCS} -5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In	t_{PLIV}		41		0.5t_{MCS} -20	ns
Input Instruction Hold after $\overline{\text{PSEN}}$	t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$	t_{PXIZ}	26			0.25t_{MCS} -5	ns
Port 0 Address to Valid Instruction In	t_{AVIV}	71			0.75t_{MCS} -20	ns
Port 2 Address to Valid Instruction In	t_{AVIV2}	81			0.875 t_{MCS} -25	ns
$\overline{\text{PSEN}}$ Low to Address Float	t_{PLAZ}	0			0	ns

NOTES FOR AC ELECTRICAL CHARACTERISTICS

- The value for t_{MCS} is a time period related to the machine cycle clock in terms of the processor's input clock frequency. Its value is highlighted in the table "STRETCH VALUE TIMING" for all possible settings of the 4X/$\overline{2X}$ and CD1:0 bits. The default condition is CD1 = 1 and CD0 = 0, where 4X/$\overline{2X}$ is disregarded.
- All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

- All signals characterized with load capacitance of 80 pF except Port 0, ALE, $\overline{PSEN}$, $\overline{RD}$ and $\overline{WR}$ with 100 pF.
- Interfacing to memory devices with float times (turn off times) over 25 ns may cause contention. This will not damage the parts, but will cause an increase in operating current.
- Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

MOVX CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK		UNITS	STRETCH VALUES C_{ST} (MD2:0)
		MIN	MAX		
Data Access ALE Pulse Width	t_{LHLL2}	$0.375t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Address Hold after ALE Low for MOVX Write	t_{LLAX2}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Pulse Width	t_{RLRH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{WR}$ Pulse Width	t_{WLWH}	$0.5t_{MCS}$-5 C_{ST}*t_{MCS}-10		ns	C_{ST}=0 1<=C_{ST}<=7
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$0.5t_{MCS}$-20 C_{ST}*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=7
Data Hold after Read	t_{RHDX}	0		ns	
Data Float after Read	t_{RHDZ}		$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-15	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to Valid Data In	t_{LLDV}		$0.625t_{MCS}$-20 (C_{ST}+0.25)*t_{MCS}-40 (C_{ST}+1.25)*t_{MCS}-40	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to Valid Data In	t_{AVDV1}		$0.75t_{MCS}$-20 (C_{ST}+0.375)*t_{MCS}-20 (C_{ST}+1.375)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to Valid Data In	t_{AVDV2}		$0.875t_{MCS}$-20 (C_{ST}+0.5)*t_{MCS}-20 (C_{ST}+1.5)*t_{MCS}-20	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.125t_{MCS}$-5 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10	$1.25t_{MCS}$+5 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL1}	$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $2.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$0.375t_{MCS}$-5 $0.625t_{MCS}$-5 $2.625t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
Data Valid to $\overline{WR}$ Transition	t_{QVWX}	-5		ns	

MOVX CHARACTERISTICS CONT'D

Data Hold after Write	t_{WHQX}	$0.25t_{MCS}$-5 $0.5t_{MCS}$-5 $1.5t_{MCS}$-10		ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7
$\overline{RD}$ Low to Address Float	t_{RLAZ}		-((0.125 t_{MCS})-5)	ns	
$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{WHLH}	0 $0.25t_{MCS}$-5 $1.25t_{MCS}$-10	10 $0.25t_{MCS}$+5 $1.25t_{MCS}$+10	ns	C_{ST}=0 1<=C_{ST}<=3 4<=C_{ST}<=7

NOTES FOR MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES

- t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the value of t_{MCS} for each Stretch selection.
- C_{ST} is the stretch cycle value as determined by the MD2, MD1, & MD0 bits of the CKCON register.

t_{MCS} TIME PERIODS

System Clock Selection	t_{MCS}
4X/$\overline{2X}$, CD1, CD0 = 100	0.5 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = 000	1 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x10	4 t_{CLCL}
4X/$\overline{2X}$, CD1, CD0 = x11	1024 t_{CLCL}

$\overline{RD}$, $\overline{WR}$ PULSE WIDTH WITH STRETCH CYCLES

MD2	MD1	MD0	MOVX Machine Cycles	$\overline{RD}$, $\overline{WR}$ Pulse Width (in oscillator clocks)			
				4X/$\overline{2X}$=1 CD1:0=00	4X/$\overline{2X}$=0 CD1:0=00	4X/$\overline{2X}$=x CD1:0=10	4X/$\overline{2X}$=x CD1:0=11
0	0	0	2	0.5 t_{CLCL}	1 t_{CLCL}	2 t_{CLCL}	2048 t_{CLCL}
0	0	1	3	t_{CLCL}	2 t_{CLCL}	4 t_{CLCL}	4096 t_{CLCL}
0	1	0	4	2 t_{CLCL}	4 t_{CLCL}	8 t_{CLCL}	8192 t_{CLCL}
0	1	1	5	3 t_{CLCL}	6 t_{CLCL}	12 t_{CLCL}	12288 t_{CLCL}
1	0	0	9	4 t_{CLCL}	8 t_{CLCL}	16 t_{CLCL}	16384 t_{CLCL}
1	0	1	10	5 t_{CLCL}	10 t_{CLCL}	20 t_{CLCL}	20480 t_{CLCL}
1	1	0	11	6 t_{CLCL}	12 t_{CLCL}	24 t_{CLCL}	24576 t_{CLCL}
1	1	1	12	7 t_{CLCL}	14 t_{CLCL}	28 t_{CLCL}	28672 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock High Time	t_{CHCX}	10			ns	
Clock Low Time	t_{CLCX}	10			ns	
Clock Rise Time	t_{CLCL}			5	ns	
Clock Fall Time	t_{CHCL}			5	ns	

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Port Clock Cycle Time SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XLXL}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	
Output Data Setup to Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{QVXH}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	
Output Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHQX}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	
Input Data Hold from Clock Rising SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDX}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	
Clock Rising Edge to Input Data Valid SM2=0, 12 clocks per cycle SM2=1, 4 clocks per cycle	t_{XHDV}		 $12t_{CLCL}$ $4t_{CLCL}$		 ns ns	

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t Time
A Address
C Clock
D Input data
H Logic level high
L Logic level low
I Instruction
P $\overline{\text{PSEN}}$
Q Output data
R $\overline{\text{RD}}$ signal
V Valid
W $\overline{\text{WR}}$ signal
X No longer a valid logic level
Z Tristate

POWER CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Start-up Time	t_{CSU}		1.8		ms	1
Power-on Reset Delay	t_{POR}			65536	t_{CLCL}	2

NOTES FOR POWER CYCLE TIMING CHARACTERISTICS

1. Start-up time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592 MHz crystal manufactured by Fox.

2. Reset delay is a synchronous counter of crystal oscillations after crystal start-up. At 33 MHz, this time is 1.99 ms.

EPROM PROGRAMMING AND VERIFICATION

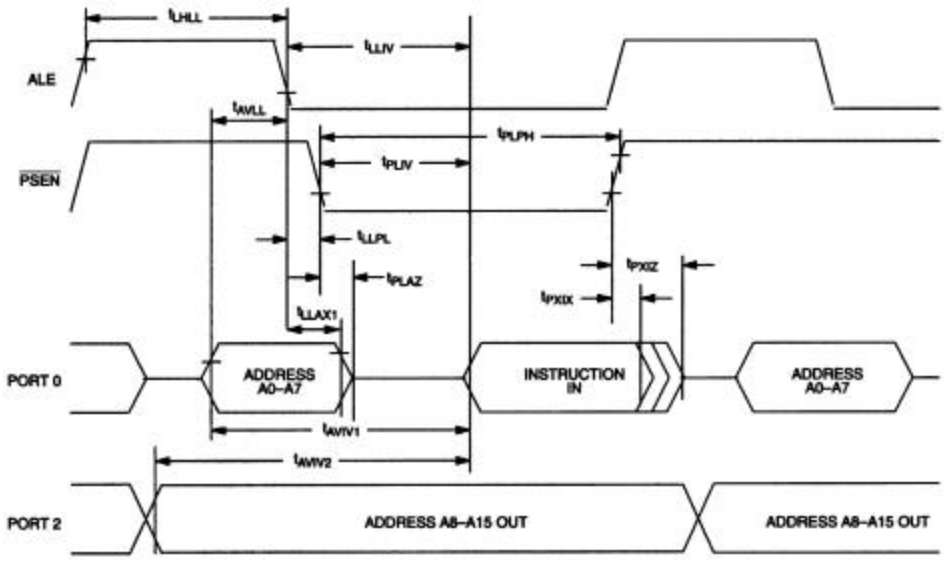
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			75	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
POR Delay	t_{DELAY}	65536			t_{CLCL}	2
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	$48t_{CLCL}$				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	$48t_{CLCL}$				
Data Hold after $\overline{PROG}$	t_{GHDX}	$48t_{CLCL}$				
Enable High to V_{PP}	t_{EHSH}	$48t_{CLCL}$				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{GHSL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			$48t_{CLCL}$		
Enable Low to Data Valid	t_{ELQV}			$48t_{CLCL}$		
Data Float after Enable	t_{EHQZ}	0		$48t_{CLCL}$		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

NOTES FOR EPROM PROGRAMMING AND VERIFICATION

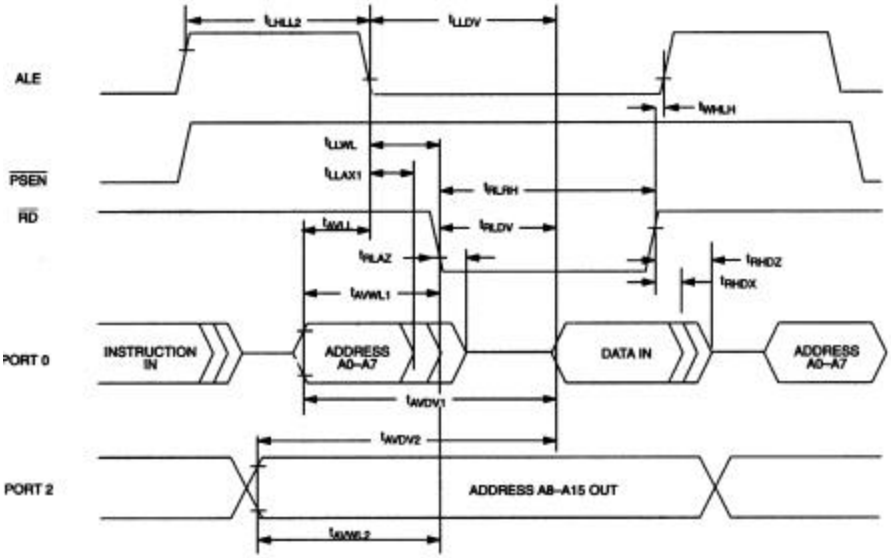
1. All voltage referenced to ground.

2. The microcontroller holds itself in reset for this duration when power is applied. No signals should be manipulated during this interval since the microcontroller is ignoring inputs. At a 4 MHz oscillator frequency, this period is 16.4 ms.

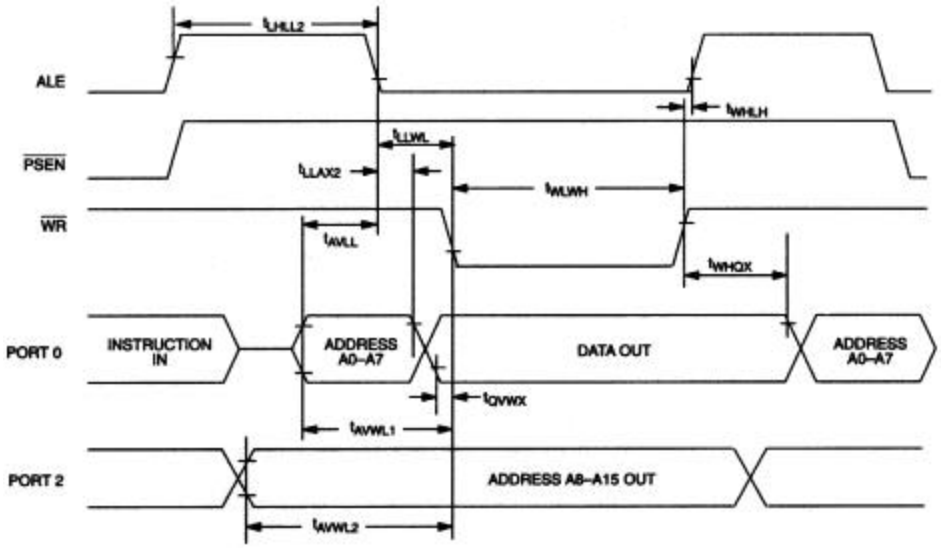
EXTERNAL PROGRAM MEMORY READ CYCLE



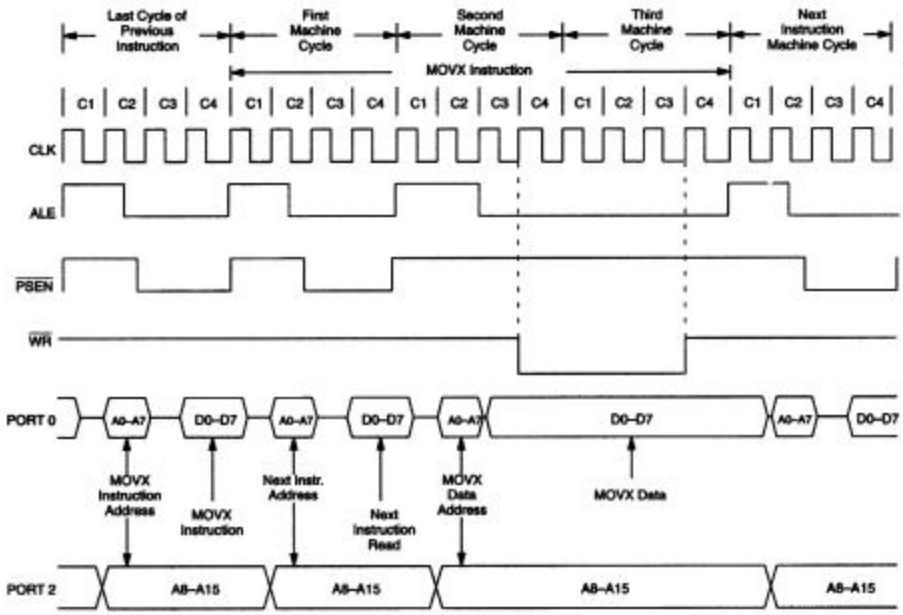
EXTERNAL DATA MEMORY READ CYCLE



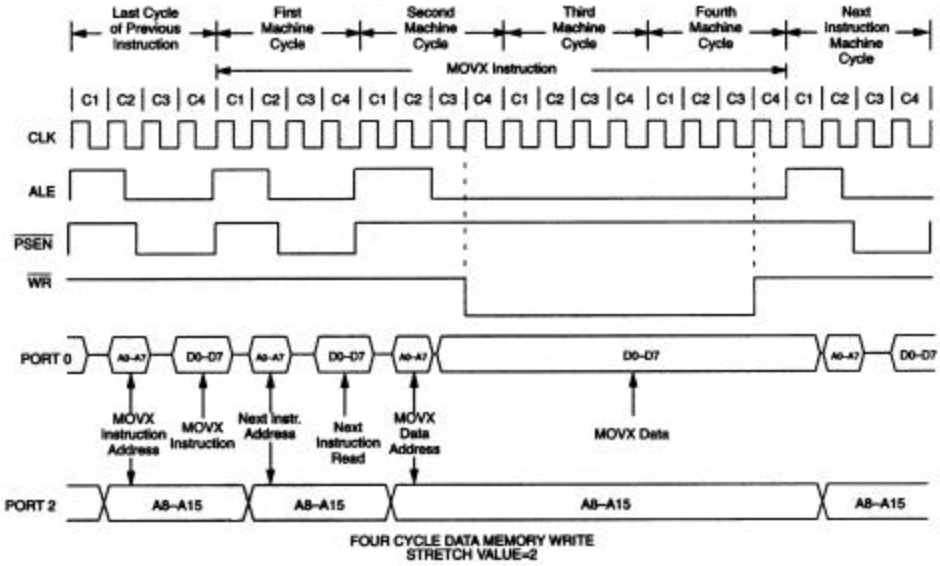
EXTERNAL DATA MEMORY WRITE CYCLE



DAT A MEMORY WRITE WITH STRETCH=1

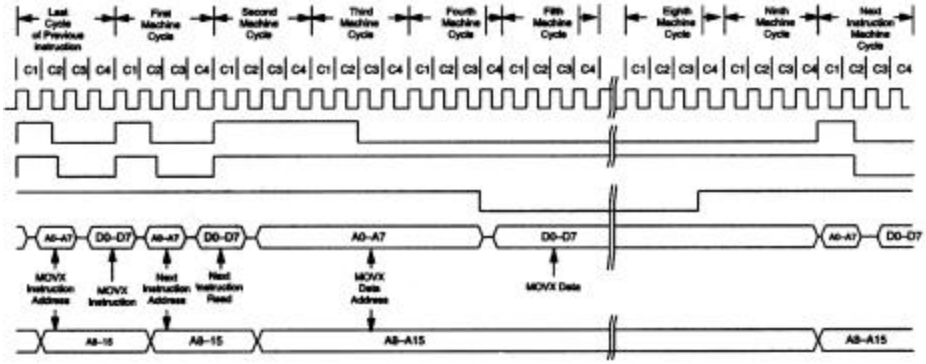


DATA MEMORY WRITE WITH STRETCH=2

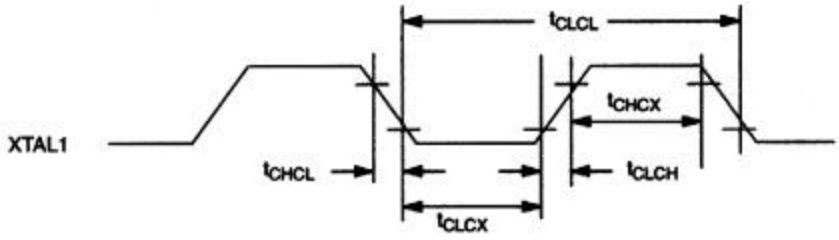


FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

DATA MEMORY WRITE WITH STRETCH=4

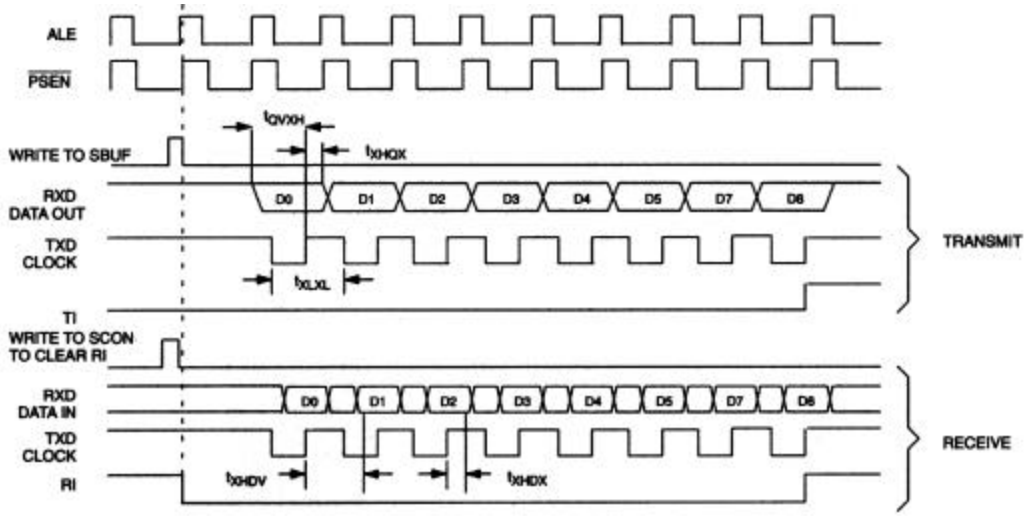


EXTERNAL CLOCK DRIVE

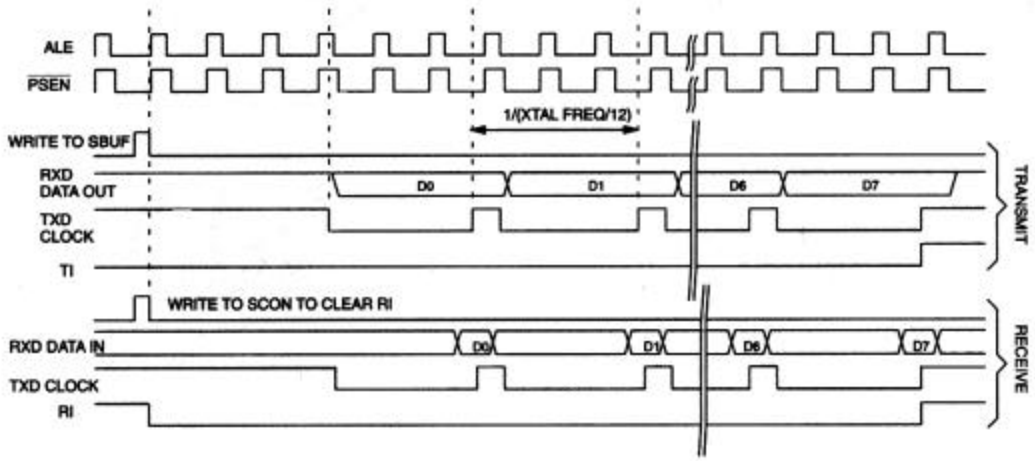


SERIAL PORT MODE 0 TIMING

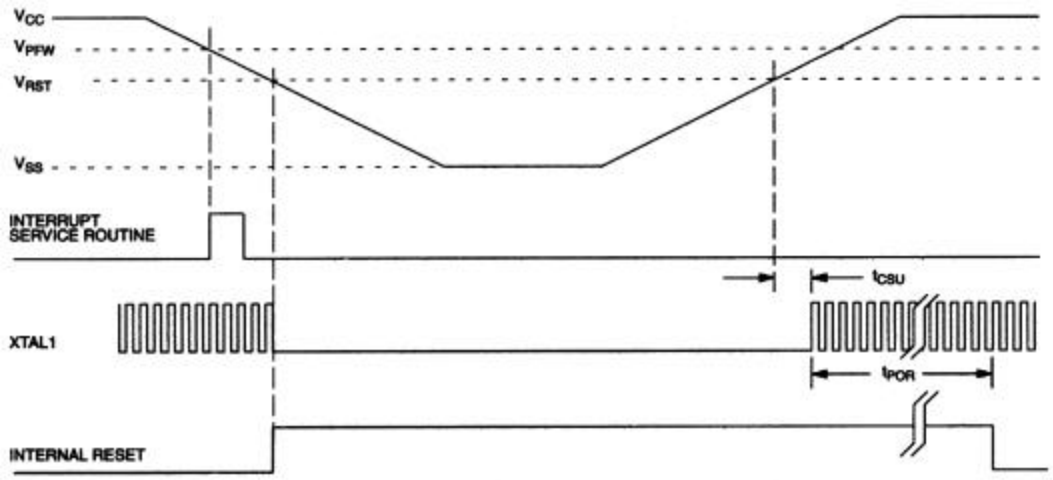
SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2=1=>TXD CLOCK=XTAL/4



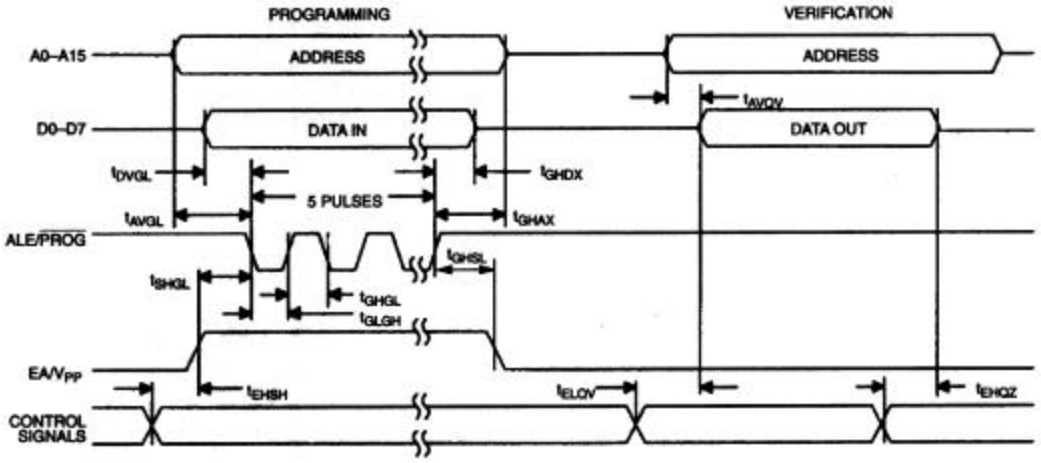
SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2=0=>TXD CLOCK=XTAL/12



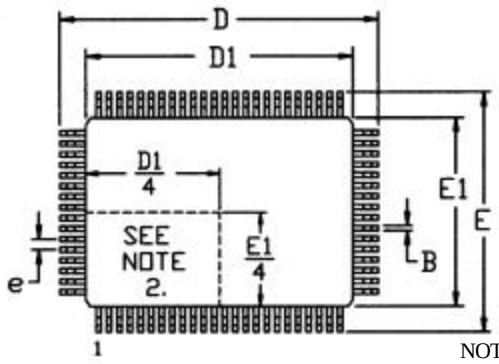
POWER CYCLE TIMING

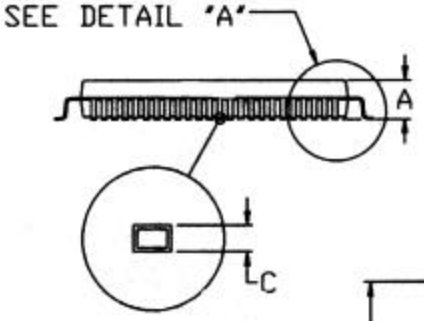


EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



80-PIN QUAD FLAT PACK (14.0 MM X 20.0 MM)

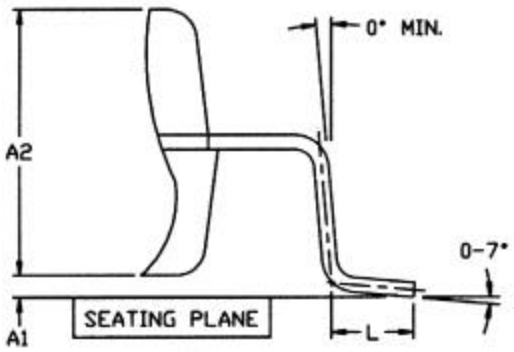




NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSIONS; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.

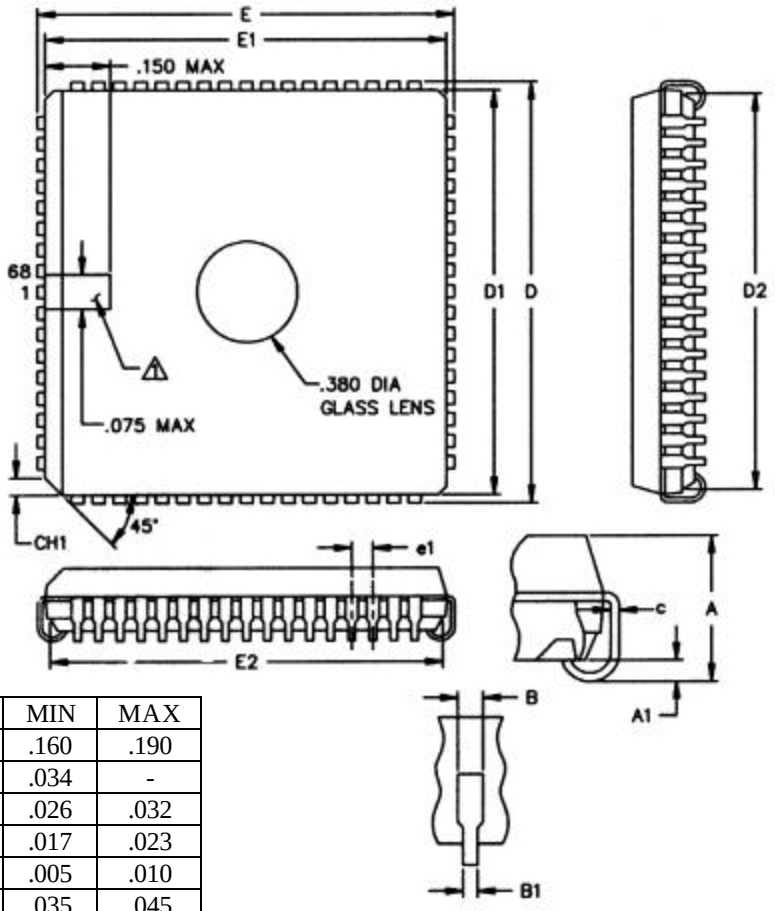
DIM	MIN	MAX
A	-	3.40
A1	0.25	-
A2	2.55	2.87
B	0.30	0.45
C	0.13	0.23
D	23.70	24.10
D1	19.90	20.10
E	17.70	18.10
E1	13.90	14.10
e	0.80 BSC	
L	0.65	0.95



DETAIL A

DIMENSIONS ARE IN MILLIMETERS

68-PIN WINDOWED CLCC



LTR	MIN	MAX
A	.160	.190
A1	.034	-
B	.026	.032
B1	.017	.023
c	.005	.010
CH1	.035	.045
D	.978	.998
D1	.940	.960
D2	.910	.930
E	.978	.998
E1	.940	.960
E2	.910	.930
e1	.050 BSC	

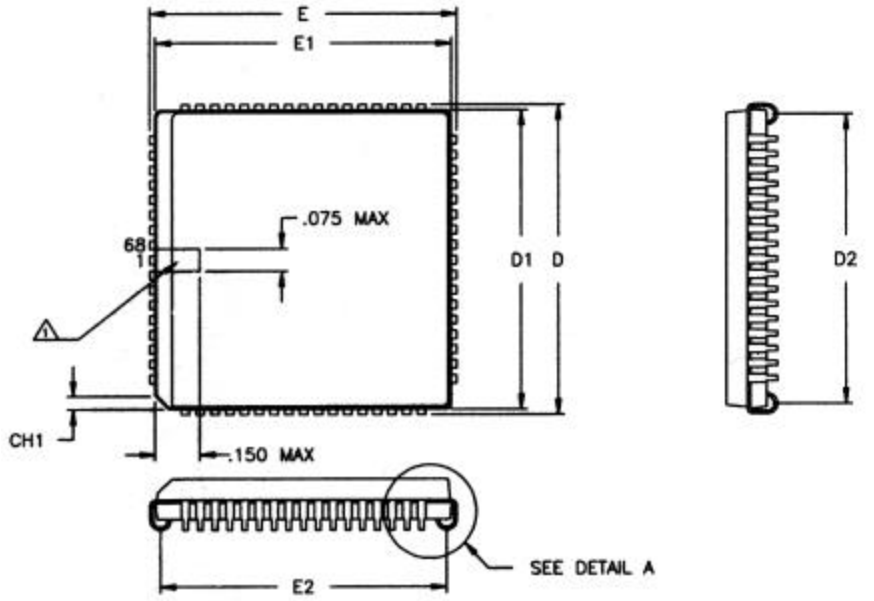
NOTES:

1. PIN-1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. ALL DIMENSIONS SHOWN ARE IN INCHES.

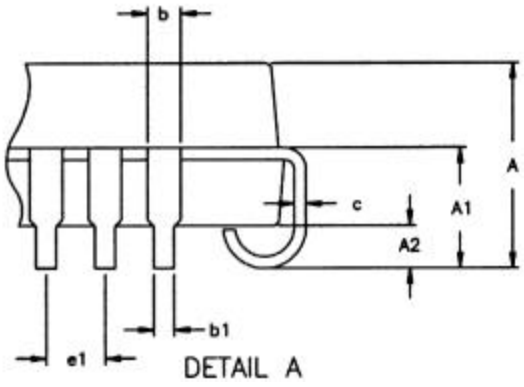
68-PIN PLCC

NOTE:

1. PIN-1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. DIMENSIONS ARE IN INCH UNITS.



DIM	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.020	-
b	.026	.032
b1	.013	.021
c	.0075	.0125
CH1	.042	.048
D	.985	.995
D1	.950	.958
D2	.882	.938
E	.985	.995
E1	.950	.958
E2	.882	.938
e1	.050 BSC	



HISTORY REVISION

The following represent the key differences between the 06/16/98 and the 06/14/99 version of the DS87C550 data sheet. Please review this summary carefully.

1. Corrected minor typographical errors on pages 3, 5, 7, 9, 17, 20, 21, 22, 26 and 33.

2. Added standard “Absolute Maximum Ratings” notation.

3. Added AID Specification conditions (V_{CC} = 5V ± 10%, 0-70°C).

4. Updated port 5’s V_{OL} and I_L specification.

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