National Semiconductor

MICROCIRCUIT DATA SHEET

MN100325-X REV 1B0

Original Creation Date: 10/30/95
Last Update Date: 05/07/04
Last Major Revision Date: 08/21/96

HEX ECL-to-TTL TRANSLATOR

General Description

The 100325 is a hex translator for converting F100K logic level to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 50K ohms pull-down resistors; therefore, the outputs will go LOW when the inputs are left unconnected. When used in the differential mode, the inputs have a common mode rejection of +1V, making this device tolerant of ground offsets and translents between the signal source and the translator. The VEE and VTTL power may be applied in either order.

Industry Part Number

100325

Prime Die

F325

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

100325DMQB
100325FMQB
100325J-QMLV
100325W-QMLV
100325WFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Pin/function compatible with 100125
- 50% power reduction of the 100125
- Differential inputs with built in offset
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Available to industrial grade temperature range
- Available to MIL-STD-883

CONTROLLING DOCUMENTS:

100325DMQB	5962-9153101MXA
100325FMQB	5962-9153101MYA
100325J-QMLV	5962-9153101VXA
100325W-QMLV	5962-9153101VYA
100325WFQMLV	5962F9153101VYA

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature (Tstg)	-65 C to +150 C
Maximum Junction Temperature (Tj)	
Ceramic	+175 C
Plastic	+150 C
Vee Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	-0.5V to +6.0V
Output Current (DC Output HIGH)	-50mA
ESD (Note 2)	$\geq$ 2000V
VTTL Pin Potential to Ground Pin	-0.5V to +6.0V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Military	-55 C to +125 C
Industrial	-40 C to +85 C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, VTTL RANGE:4.5V to 5.5V,Tc=-55c to +125c, VCC=GND

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VTTL=5.0V, VM=-0.87V	1, 3	INPUTS		350	uA	1, 2
			1, 3	INPUTS		500	uA	3
IIL	Input Low Current	VEE=-4.2V, VTTL=5.0V, VM=-1.83V	1, 3	INPUTS	0.5		uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VTTL=4.5V, VIH=-0.87V, VIL=-1.83V, IOH=-2.0mA	1, 3	OUTPUTS	2.5		V	1, 2
			1, 3	OUTPUTS	2.4		V	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VTTL=4.5V, VIH=-0.87V, VIL=-1.83V, IOL=20.0mA	1, 3	OUTPUTS		0.5	V	1, 2, 3
IOS	Short-Circuit Current	VEE=-4.5V, VTTL=5.5V, VM=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VEE=-4.5V, VTTL=5.5V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3
VBBX	Output Reference Voltage	VEE=-4.5V, VTTL=5.0V, IM=-3uA	1, 3	VBB		-1260	mV	1, 2, 3
VBBN	Output Reference Voltage	VEE=-5.7V, VTTL=5.0V, IM=-2.1mA	1, 3	VBB	-1380		mV	1, 2
		VEE= -5.7V, VTTL=5.0V, IM=-3mA	1, 3	VBB	-1396		mV	3
VIH	Input HIGH Voltage	OTHER INPUT AT VBB	1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage	OTHER INPUT AT VBB	1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
VCM	Common Mode Voltage	VEE= -4.2/-5.7V, VTTL=4.5V	1, 3, 7	INPUTS	-2000	-500	mV	1, 2, 3
VDIF	Input Voltage Differential	VEE= -4.2/-5.7V, VTTL=4.5V	1, 3, 7	INPUTS	150		mV	1, 2, 3
IEE	Power Supply Current	VEE=-4.2/-5.7V, VTTL=5.0V, VIN=VBB	1, 3	VEE	-35	-12	mA	1, 2, 3
ITTL	Power Supply Current	VEE=-4.5V, VTTL=5.5V, VIN=VBB	1, 3	VTTL		65	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vee Range: -4.2V to -5.7V, VTTL Range: 4.5V to 5.5V, VCC=GND, LOADING: 50 pF/500 Ohms

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH/tpHL	Propagation Delay	VEE=-4.2/-5.7V, VTTL=4.5/5.5V, VCC=GND	2, 4	Dn to Qn	1.6	4.7	ns	9
			2, 4	Dn to Qn	1.7	5.7	ns	10
			2, 4	Dn to Qn	1.5	5.0	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V, VTTL=4.5/5.5V, VCC=GND	6	Qn	0.5	2.5	ns	9, 10
			6	Qn	0.5	3.0	ns	11

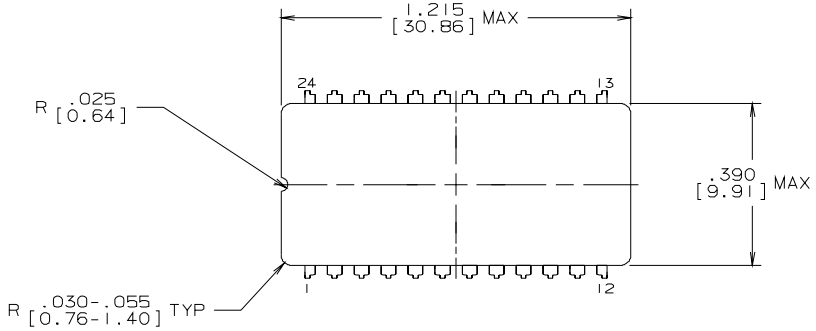
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroup A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

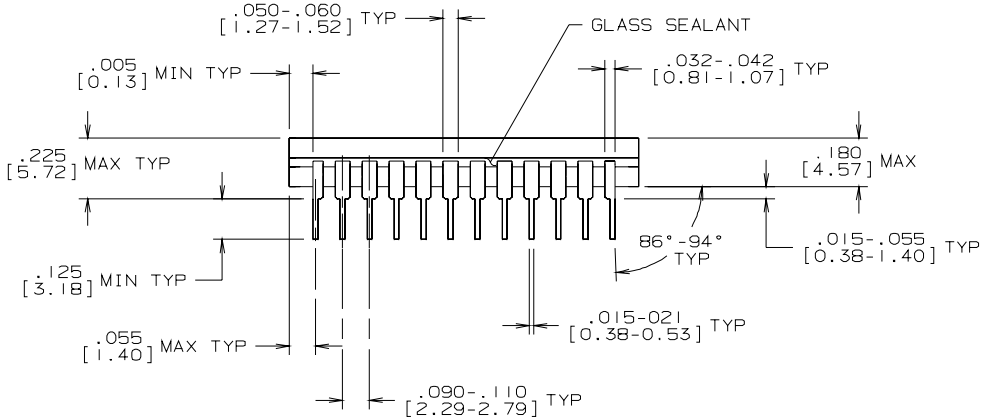
Graphics and Diagrams

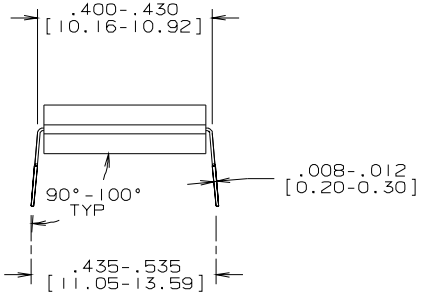
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP (J), 24LD, .400 CENTERS (P/P DWG)
P000054A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000055A	CERPACK, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPACK, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH MM

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 24 LEAD, .400 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B0	M0004382	05/07/04	Rose Malone	Update MDS: MN100325-X, Rev. 1A0 to 1B0. Added NSID 100325WFQMLV to Main Table and to Features Section.

National Semiconductor was acquired by Texas Instruments.

http://www.ti.com/corp/docs/investor_relations/pr_09_23_2011_national_semiconductor.html

This file is the datasheet for the following electronic components:

5962-9153101MYA - http://www.ti.com/product/5962-9153101mya?HQS=TI-null-null-dscatalog-df-pf-null-wwe

5962-9153101MXA - http://www.ti.com/product/5962-9153101mxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe

5962-9153101VXA - http://www.ti.com/product/5962-9153101vxa?HQS=TI-null-null-dscatalog-df-pf-null-wwe

5962-9153101VYA - http://www.ti.com/product/5962-9153101vya?HQS=TI-null-null-dscatalog-df-pf-null-wwe

5962F9153101VYA - http://www.ti.com/product/5962f9153101vya?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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