



BT138X-600D

4Q Triac

29 August 2013

Product data sheet

1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT186A (TO-220F) "full pack" plastic package intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Isolated package
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose phase control
- General purpose switching

4. Quick reference data

Table 1. Quick reference data

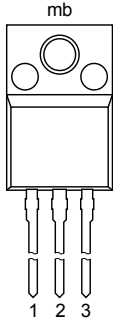

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	95	A
T_j	junction temperature		-	-	125	$^{\circ}\text{C}$
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_h \leq 56\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	12	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	1.3	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7	-	2.8	5	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	3.2	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	5.5	10	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	-	50	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-220F (SOT186A)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BT138X-600D	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 56\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	95	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	105	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	45	A ² s
di_T/dt	rate of rise of on-state current	$I_T = 20\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G+	-	50	A/ μs
		$I_T = 20\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2+ G-	-	50	A/ μs
		$I_T = 20\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G-	-	50	A/ μs
		$I_T = 20\text{ A}$; $I_G = 0.2\text{ A}$; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$; T2- G+	-	10	A/ μs
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C

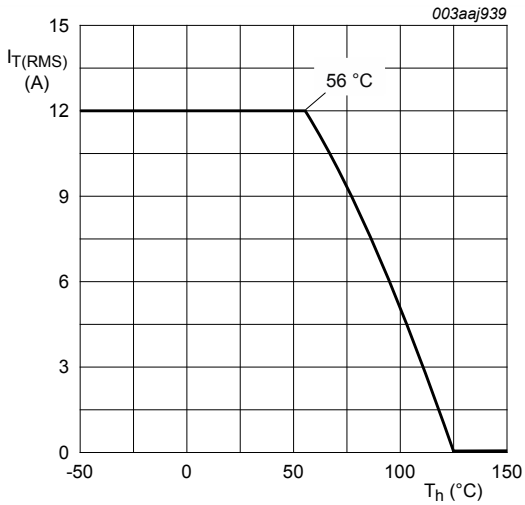


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

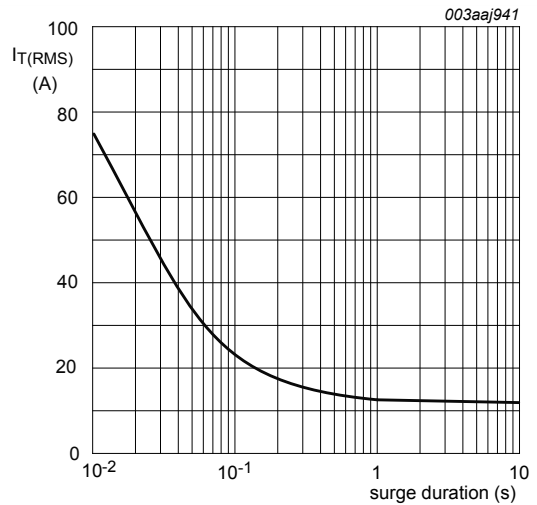


Fig. 2. RMS on-state current as a function of surge duration; maximum values
f = 50 Hz; T_h = 56 °C

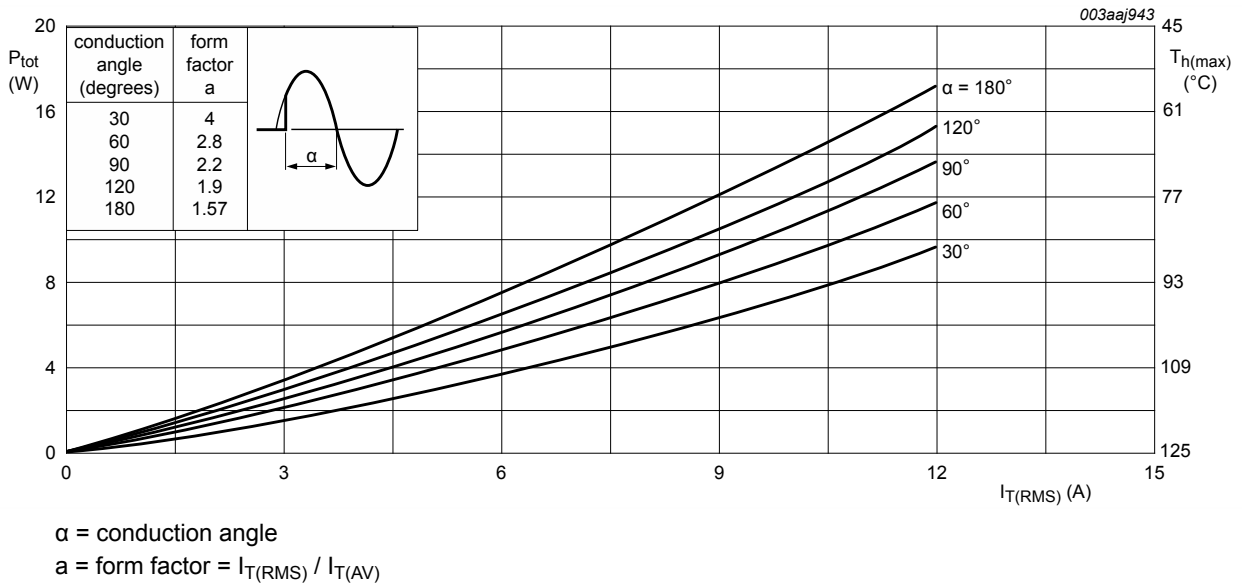


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

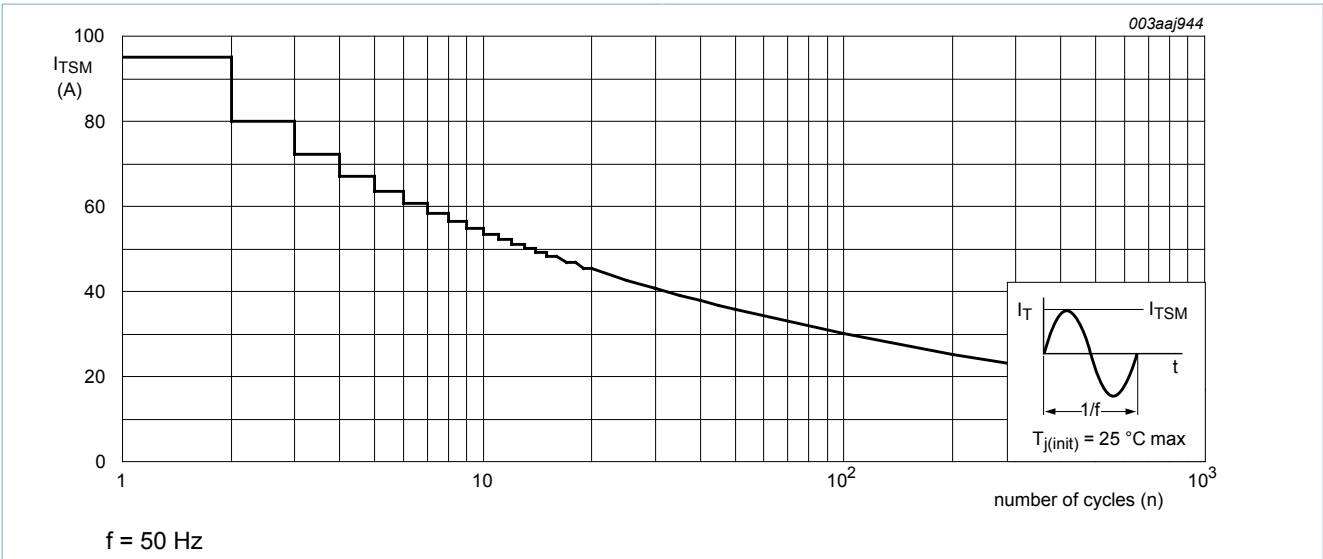


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

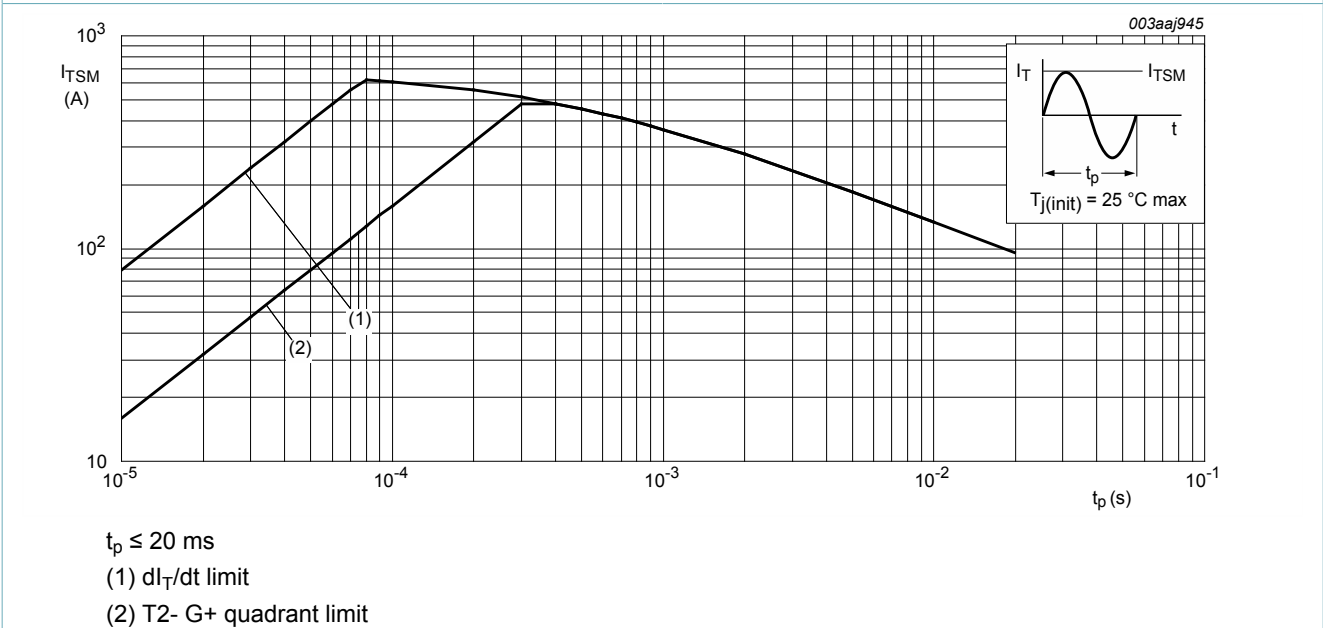
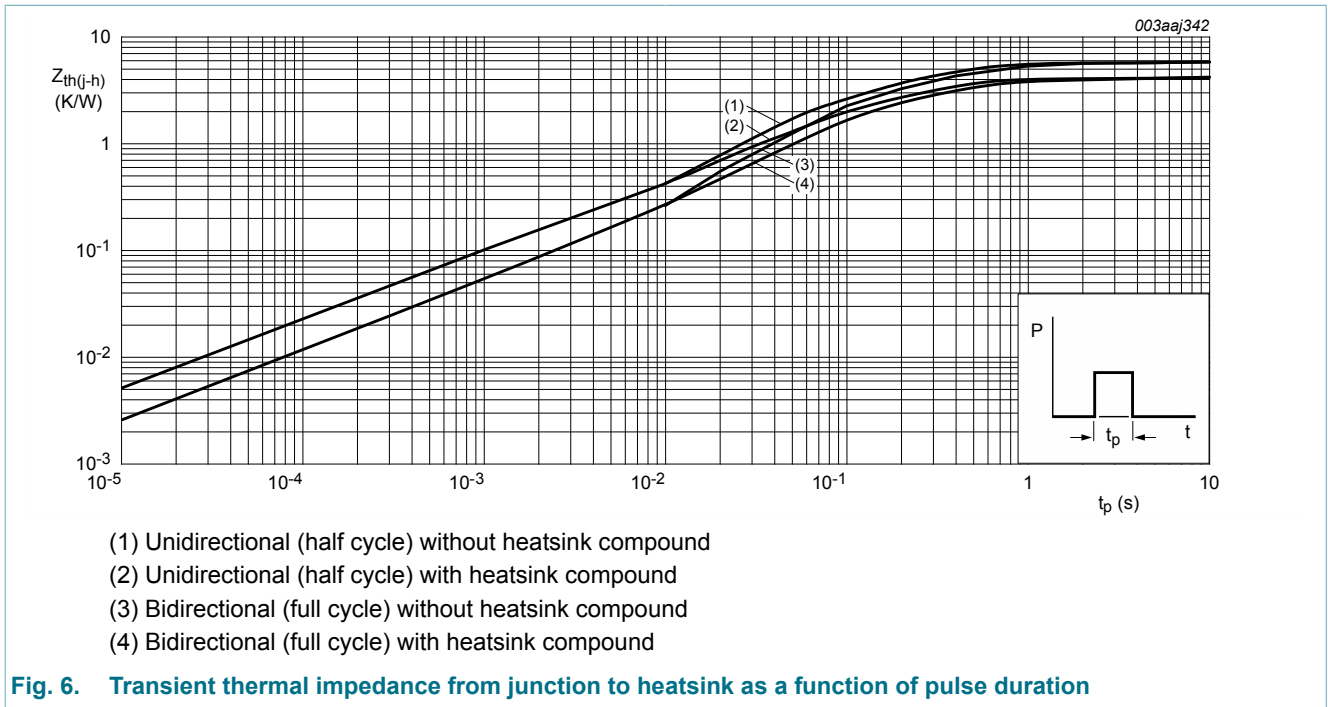


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound; Fig. 6	-	-	4	K/W
		full or half cycle; without heatsink compound; Fig. 6	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free ; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; $T_h = 25\text{ °C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink ; f = 1 MHz; $T_h = 25\text{ °C}$	-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	-	1.3	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	-	2.8	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	-	3.2	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	-	5.5	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	15	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	20	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	15	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	20	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	10	mA
V_T	on-state voltage	$I_T = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.4	1.65	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 11	0.25	0.4	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	-	50	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 16\text{ A}$; $V_D = 600\text{ V}$; $I_G = 0.1\text{ A}$; $dI_G/dt = 5\text{ A}/\mu$ s	-	2	-	μ s



Fig. 7. Normalized gate trigger current as a function of junction temperature

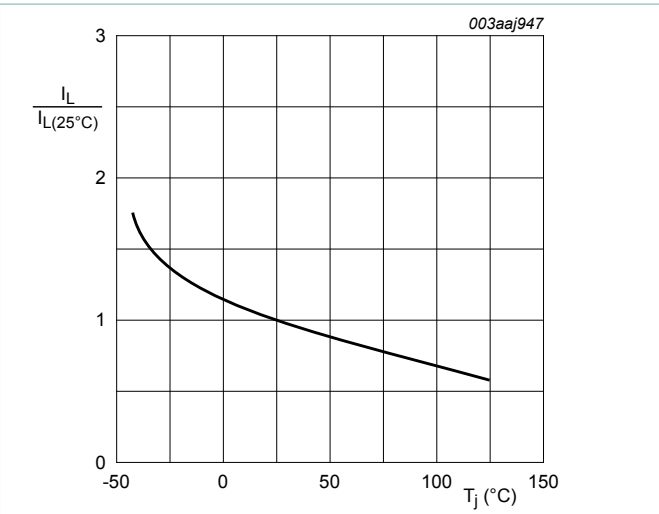


Fig. 8. Normalized latching current as a function of junction temperature

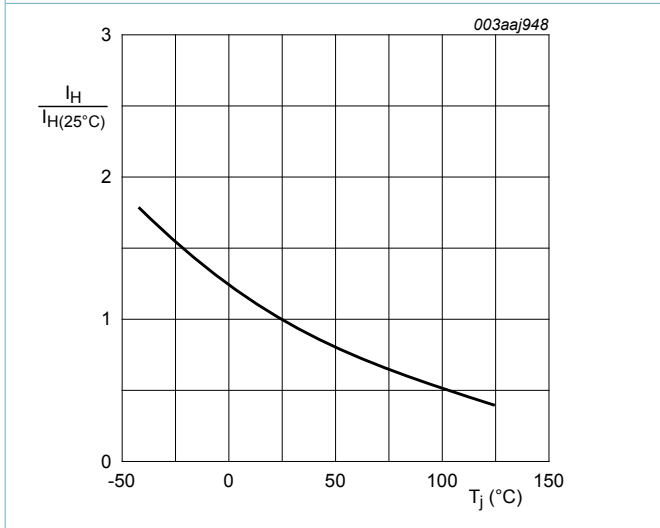


Fig. 9. Normalized holding current as a function of junction temperature

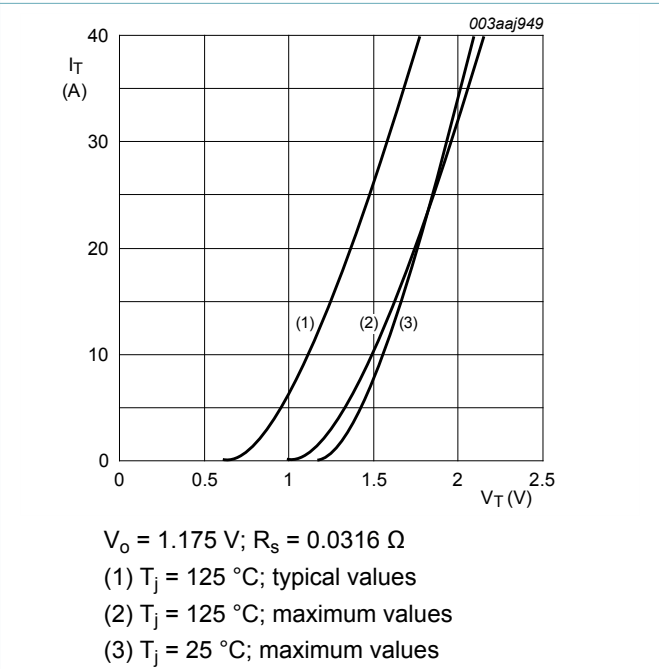


Fig. 10. On-state current as a function of on-state voltage

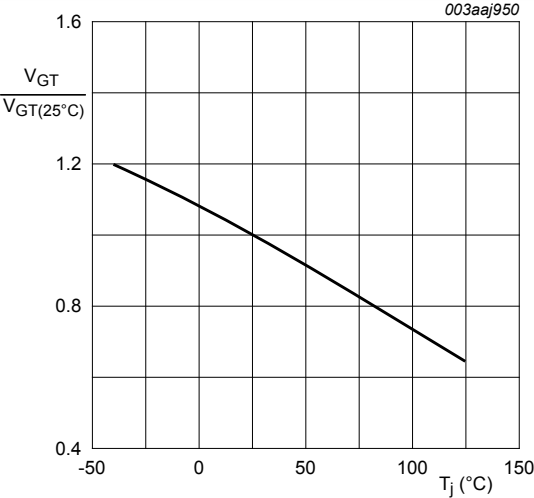
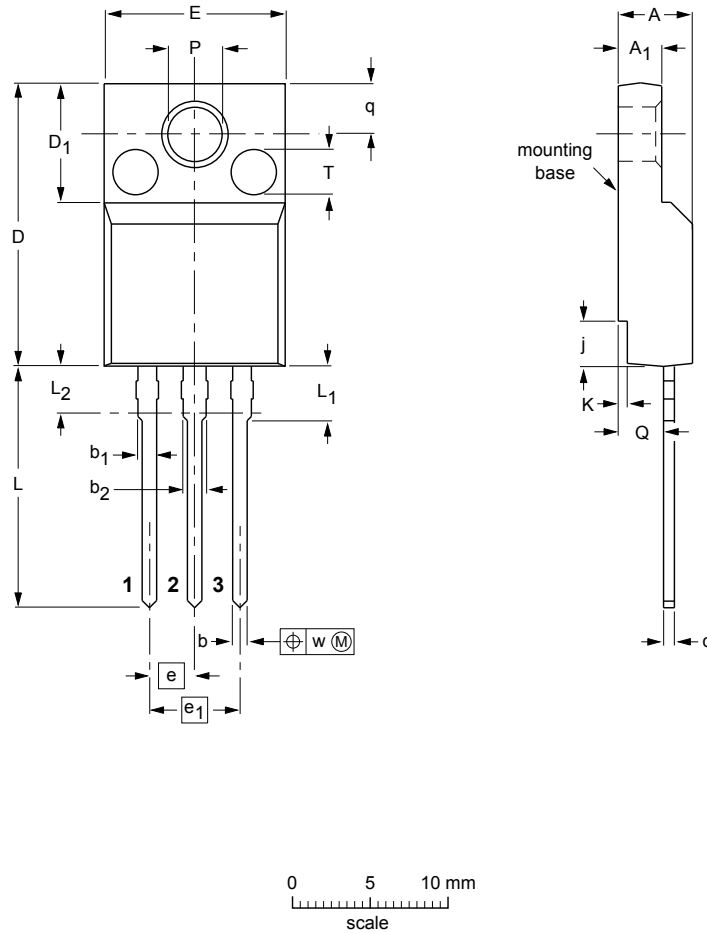


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3-lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j	K	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	T ⁽²⁾	w
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	2.5	0.4
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes

- Terminal dimensions within this zone are uncontrolled.
- Both recesses are # 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3-lead TO-220F			02-04-09 06-02-14

Fig. 12. Package outline TO-220F (SOT186A)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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