



# BT151X-650R

SCR

16 March 2014

Product data sheet

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high bidirectional blocking voltage and high current surge capability with high thermal cycling performance.

## 2. Features and benefits

- High bidirectional blocking voltage capability
- High current surge capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

## 4. Quick reference data

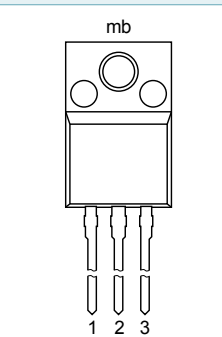

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	650	V
$V_{RRM}$	repetitive peak reverse voltage		-	-	650	V
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	120	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	12	A
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	2	15	mA



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>TO-220F (SOT186A)</p>	 <p>sym037</p>
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151X-650R	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

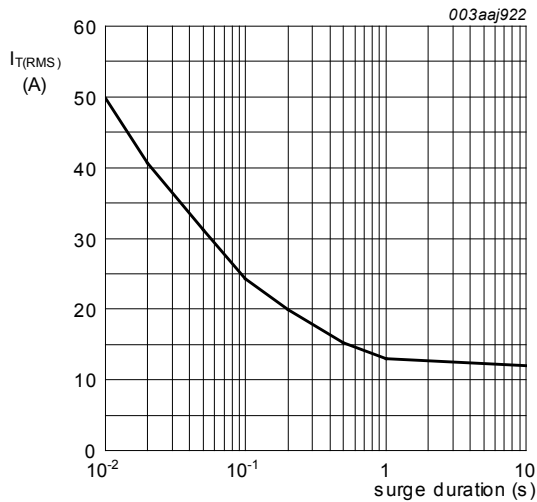
## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

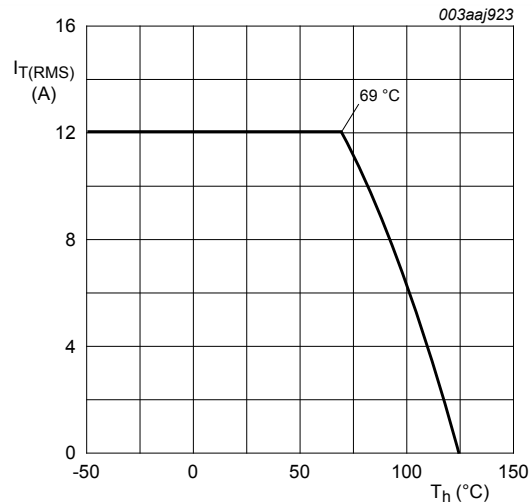
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	650	V
$V_{RRM}$	repetitive peak reverse voltage		-	650	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 69\text{ }^\circ\text{C}$	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 69\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	12	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	120	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 8.3\text{ ms}$	-	132	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	72	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_T = 20\text{ A}$ ; $I_G = 50\text{ mA}$ ; $di_G/dt = 50\text{ mA}/\mu\text{s}$	-	50	A/ $\mu\text{s}$
$I_{GM}$	peak gate current		-	2	A

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C

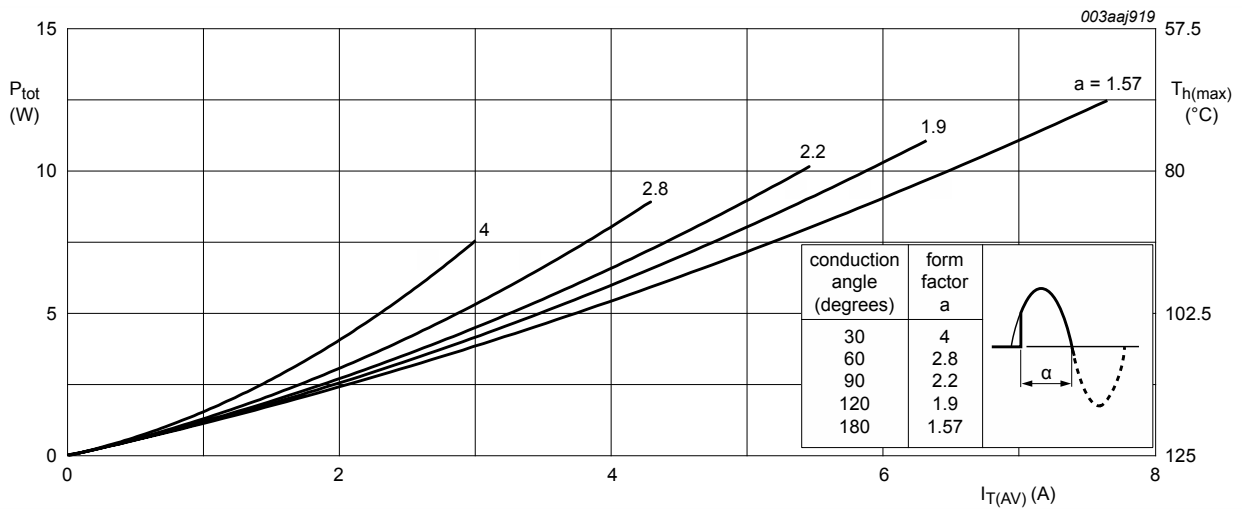


**Fig. 1. RMS on-state current as a function of surge duration; maximum values**

$f = 50 \text{ Hz}; T_h = 69 \text{ °C}$

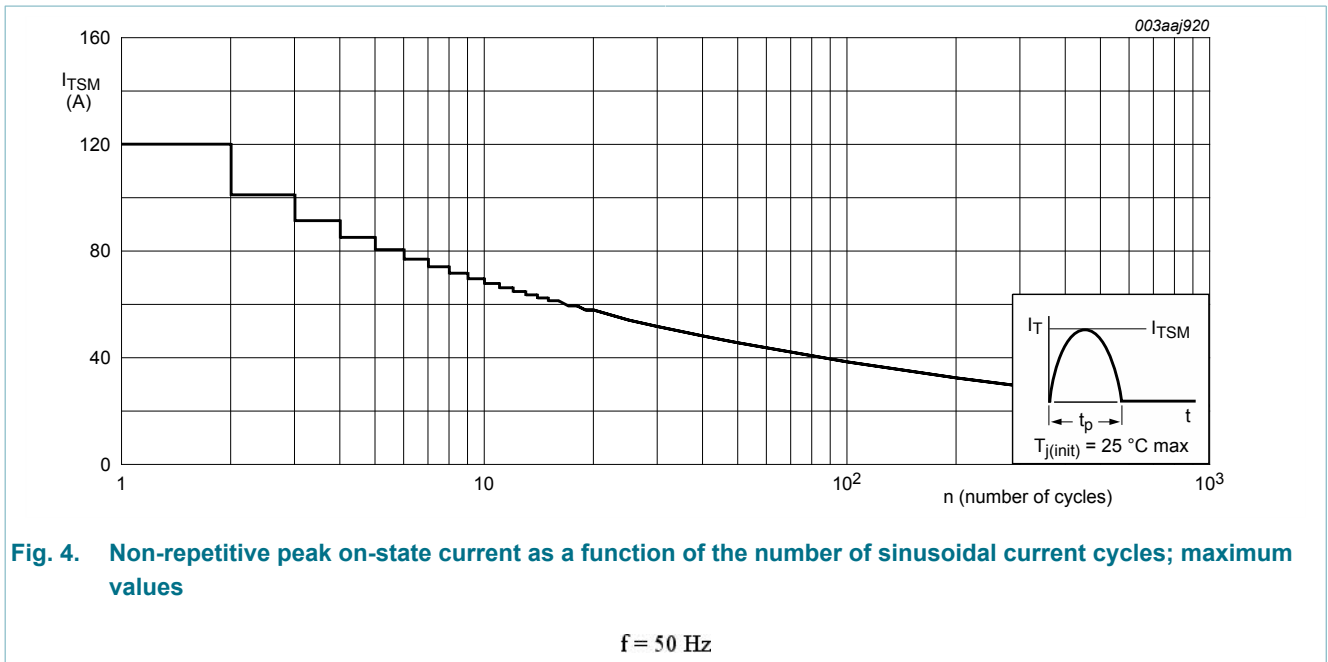


**Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values**

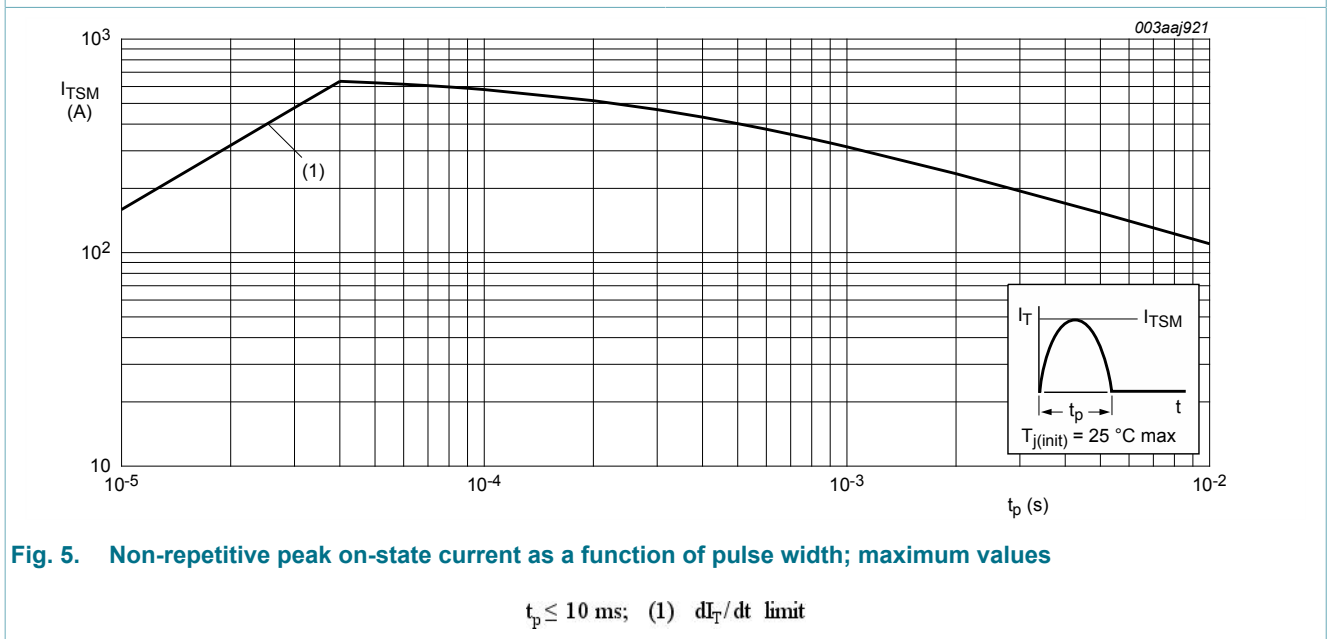


**Fig. 3. Total power dissipation as a function of average on-state current; maximum values**

$a = \text{conduction angle}$      $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$



**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

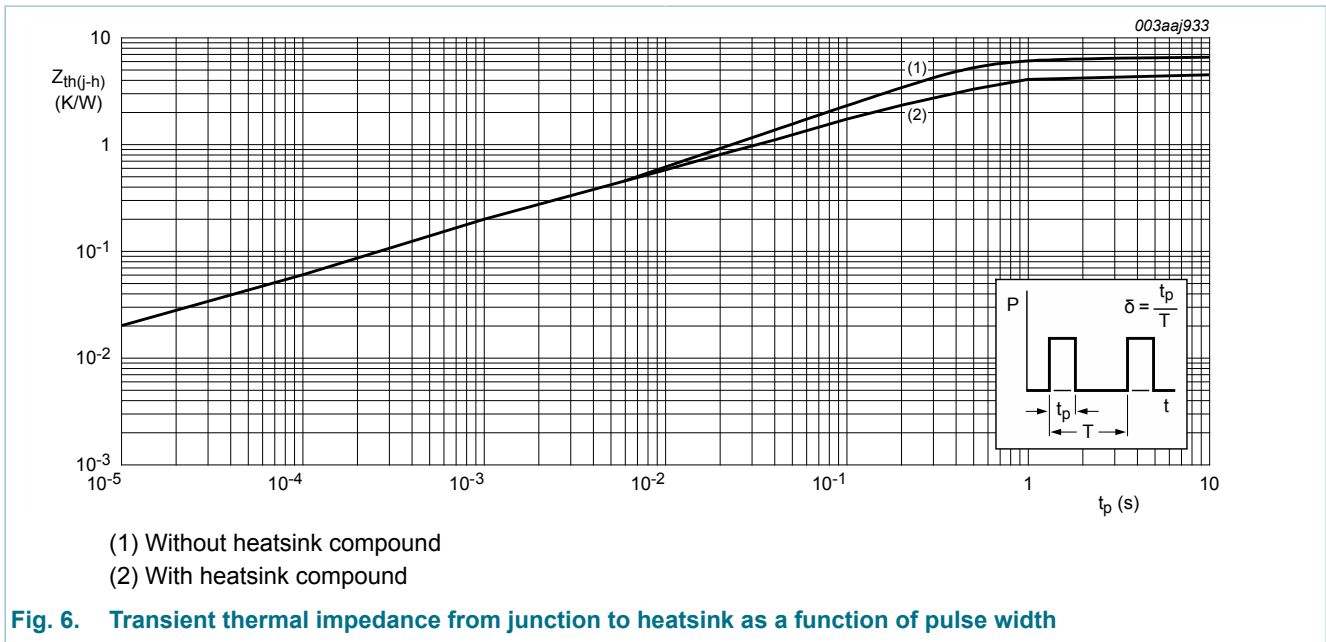


**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; <a href="#">Fig. 6</a>	-	-	4.5	K/W
		without heatsink compound; <a href="#">Fig. 6</a>	-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	55	-	K/W



## 9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; $T_h = 25\text{ °C}$	-	-	2500	V
$C_{isol}$	isolation capacitance	from anode to external heatsink; f = 1 MHz; $T_h = 25\text{ °C}$	-	10	-	pF

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	2	15	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	10	40	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	7	20	mA
$V_T$	on-state voltage	$I_T = 23\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.4	1.75	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	0.6	1	V
		$V_D = 650\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$ ; <a href="#">Fig. 11</a>	0.25	0.4	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_D$	off-state current	$V_D = 650\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
$I_R$	reverse current	$V_R = 650\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 436\text{ V}; T_j = 125\text{ }^\circ\text{C}; R_{GK} = 100\text{ }\Omega;$ ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	200	1000	-	V/ $\mu\text{s}$
		$V_{DM} = 436\text{ V}; T_j = 125\text{ }^\circ\text{C};$ ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a>	50	130	-	V/ $\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 40\text{ A}; V_D = 650\text{ V}; I_G = 100\text{ mA};$ $dI_G/dt = 5\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 436\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{TM} = 20\text{ A};$ $V_R = 25\text{ V}; (dI_T/dt)_M = 30\text{ A}/\mu\text{s}; dV_D/dt = 50\text{ V}/\mu\text{s};$ $R_{GK} = 100\text{ }\Omega;$ ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	70	-	$\mu\text{s}$

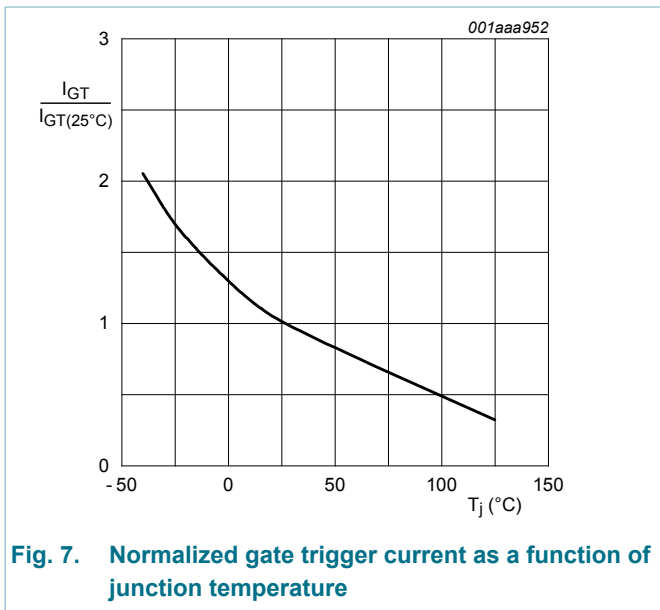


Fig. 7. Normalized gate trigger current as a function of junction temperature

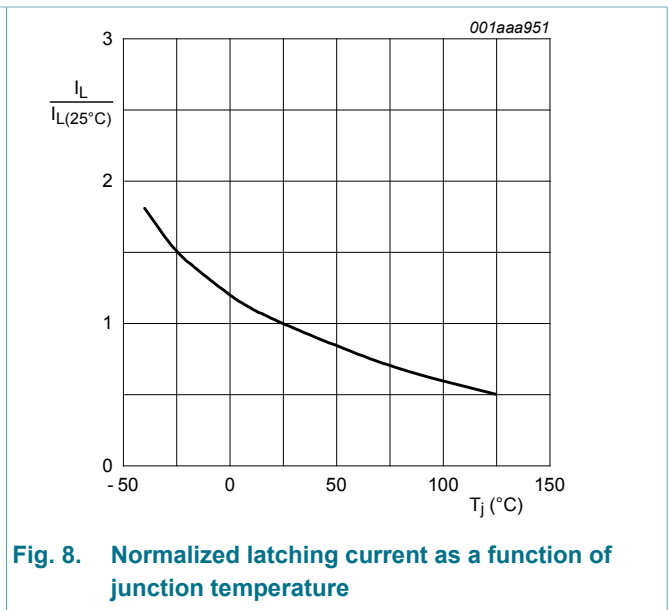
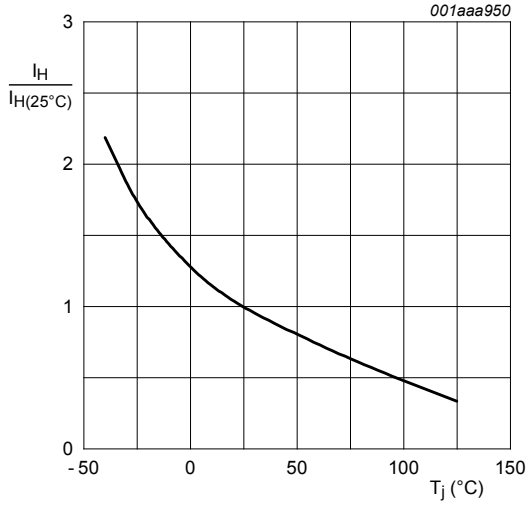
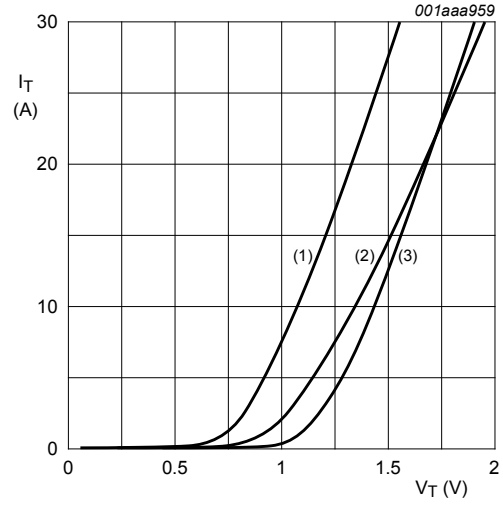


Fig. 8. Normalized latching current as a function of junction temperature

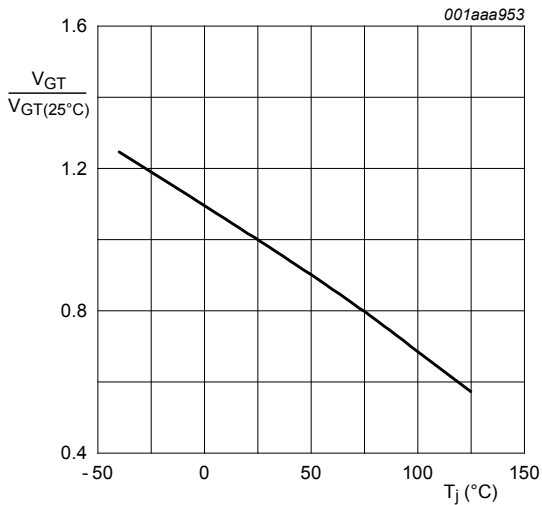


**Fig. 9. Normalized holding current as a function of junction temperature**

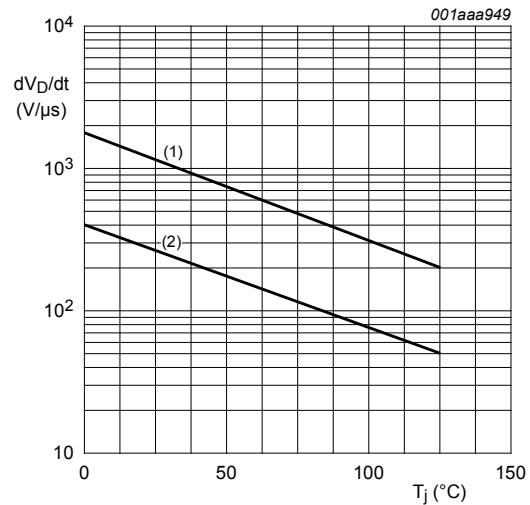


$V_o = 1.06 \text{ V}; R_s = 0.0304 \Omega$   
 (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values  
 (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values  
 (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

**Fig. 10. On-state current as a function of on-state voltage**



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**



(1)  $R_{GK} = 100 \Omega$ ;  
 (2) gate open circuit

**Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values**

### 11. Package outline

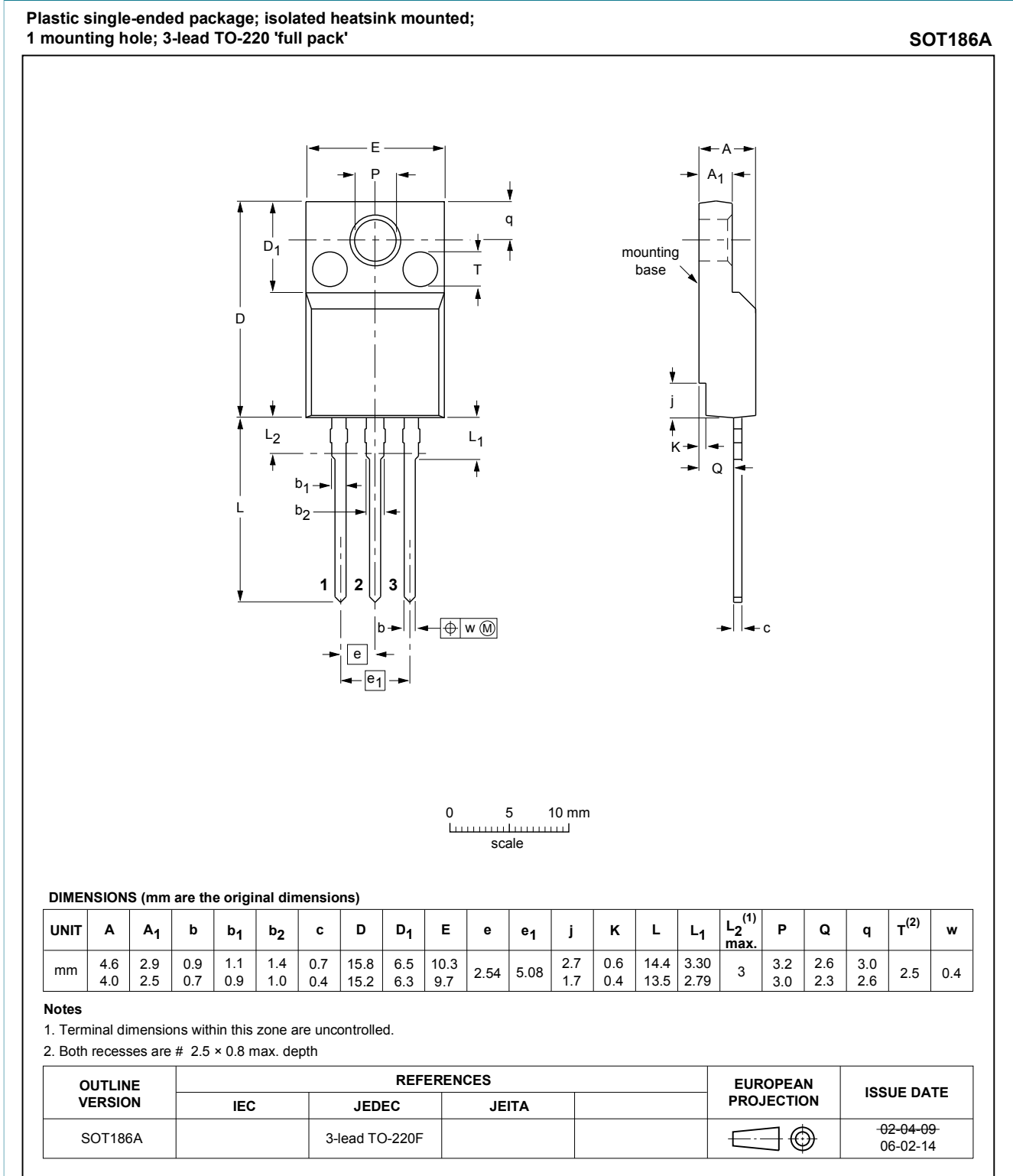


Fig. 13. Package outline TO-220F (SOT186A)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 13. Contents

<b>1</b>	<b>General description .....</b>	<b>1</b>
<b>2</b>	<b>Features and benefits .....</b>	<b>1</b>
<b>3</b>	<b>Applications .....</b>	<b>1</b>
<b>4</b>	<b>Quick reference data .....</b>	<b>1</b>
<b>5</b>	<b>Pinning information .....</b>	<b>2</b>
<b>6</b>	<b>Ordering information .....</b>	<b>2</b>
<b>7</b>	<b>Limiting values .....</b>	<b>2</b>
<b>8</b>	<b>Thermal characteristics .....</b>	<b>4</b>
<b>9</b>	<b>Isolation characteristics .....</b>	<b>5</b>
<b>10</b>	<b>Characteristics .....</b>	<b>5</b>
<b>11</b>	<b>Package outline .....</b>	<b>8</b>
<b>12</b>	<b>Legal information .....</b>	<b>9</b>
12.1	Data sheet status .....	9
12.2	Definitions .....	9
12.3	Disclaimers .....	9
12.4	Trademarks .....	10

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