USE ULTRA37000™ FOR ALL NEW DESIGNS

CY7C342B

128-Macrocell MAX® EPLD

Features

- **128 macrocells in eight logic array blocks (LABs)**
- **Eight dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **Advanced 0.65-micron CMOS technology to increase performance**
- **Available in 68-pin HLCC, PLCC, and PGA packages**

Functional Description

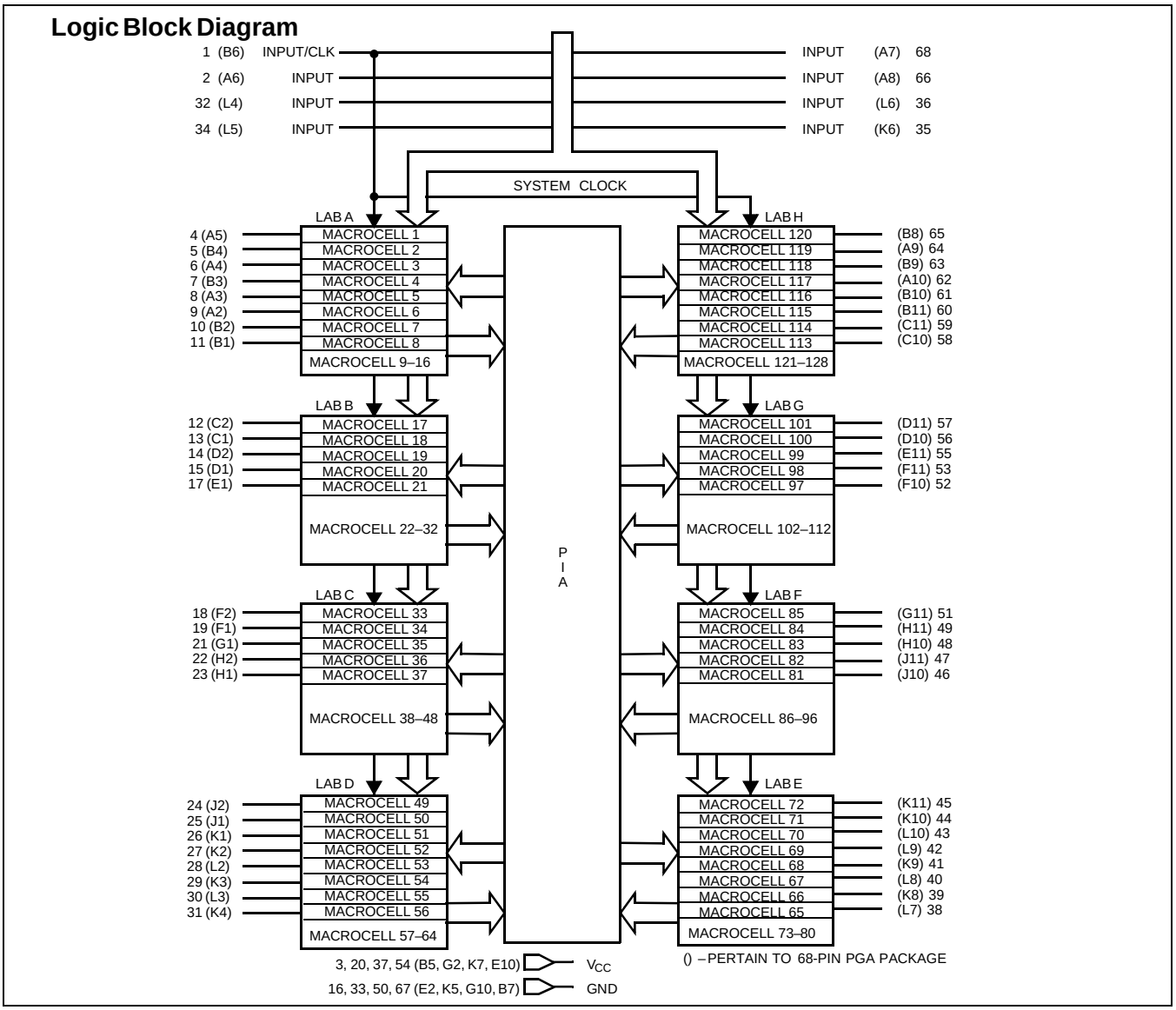
The CY7C342B is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX® architecture is 100% user-configurable, allowing the device to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342B are divided into eight LABs, 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB.

Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C342B allows it to be used in a wide range of applications, from replacement of large amounts of 7400-series TTL logic, to complex controllers and multifunction chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342B allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342B reduces board space, part count, and increases system reliability.

Logic Block Diagram

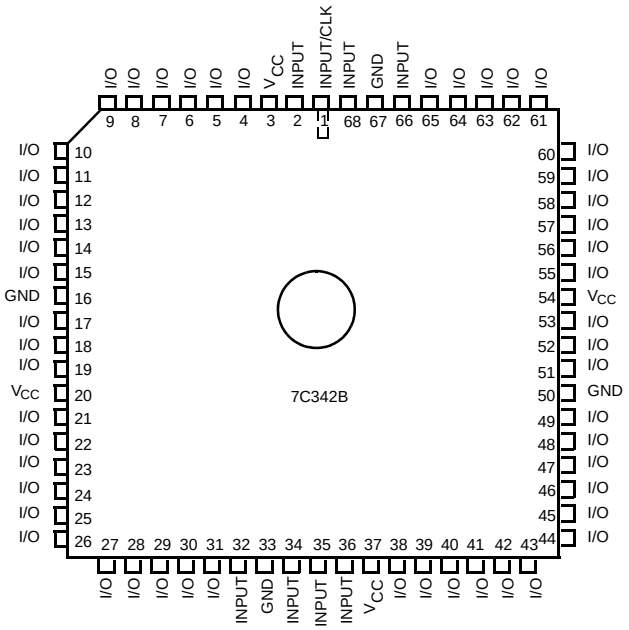


Selection Guide

	7C342B-15	7C342B-20	7C342B-25	7C342B-30	7C342B-35	Unit
Maximum Access Time	15	20	25	30	35	ns

Pin Configurations

HLCC, PLCC
Top View



PGA
Bottom View

	1	2	3	4	5	6	7	8	9	10	11
L		I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	I/O	I/O	
K	I/O	I/O	I/O	I/O	GND	INPUT	VCC	I/O	I/O	I/O	I/O
J	I/O	I/O								I/O	I/O
H	I/O	I/O								I/O	I/O
G	I/O	VCC								GND	I/O
F	I/O	I/O				7C342B				I/O	I/O
E	I/O	GND								VCC	I/O
D	I/O	I/O								I/O	I/O
C	I/O	I/O								I/O	I/O
B	I/O	I/O	I/O	I/O	VCC	INPUT/ CLK	GND	I/O	I/O	I/O	I/O
A	■	I/O	I/O	I/O	I/O	INPUT	INPUT	INPUT	I/O	I/O	

Logic Array Blocks

There are eight logic array blocks in the CY7C342B. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342B provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins that may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals that may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a signal pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342B may be easily determined using *Warp*®, *Warp* Professional™, or *Warp* Enterprise™ software by the model shown in *Figure 1*. The CY7C342B has fixed internal delays, allowing the user to determine the worst-case timing delays for any design.

Design Recommendations

Operation of the devices described herein with conditions above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342B contains circuitry to protect device pins from high static voltages or electric fields, but normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages.

For proper operation, input and output pins must be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types have.

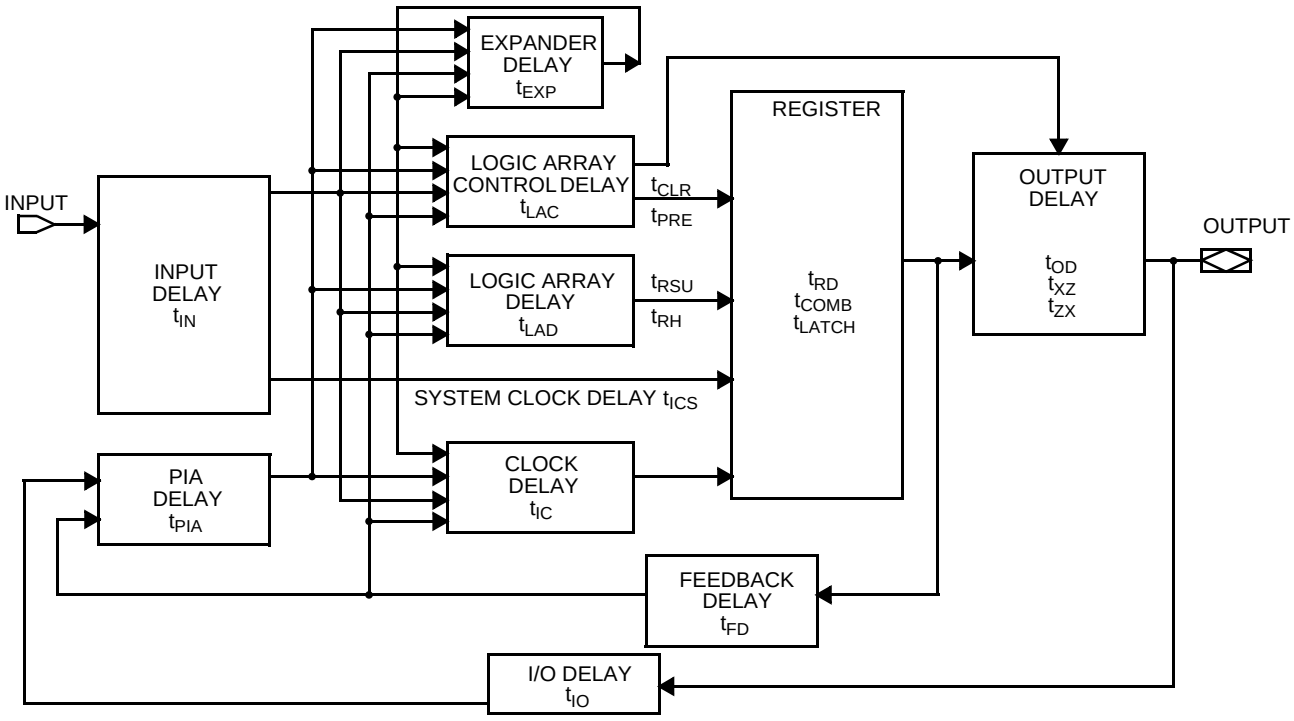


Figure 1. CY7C342B Internal Timing Model

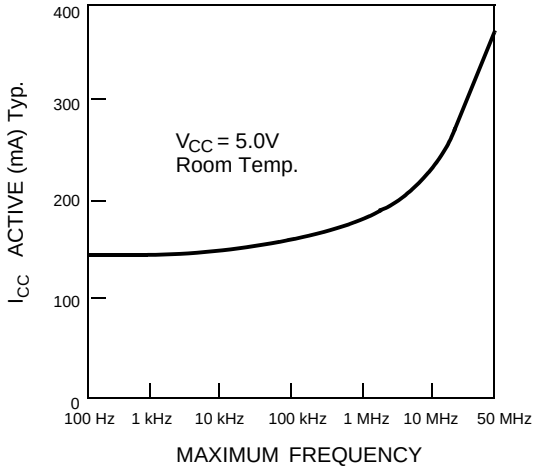
Design Security

The CY7C342B contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the entire device.

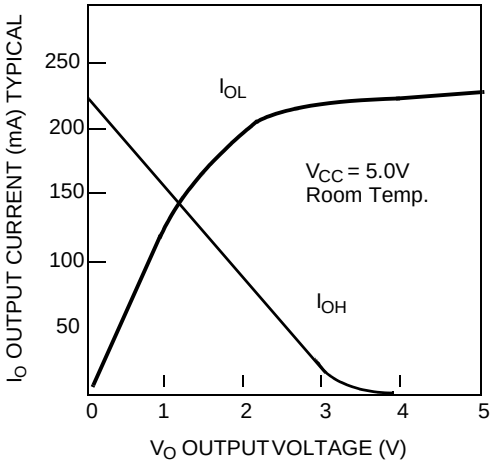
The CY7C342B is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Typical I_{CC} vs. f_{MAX}



Output Drive Current



Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders, add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from straight input pin.

When calculating synchronous frequencies, use t_{SU} if all inputs are on dedicated input pins. When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +135°C

Ambient Temperature with Power Applied..... –65°C to +135°C

Maximum Junction Temperature (under bias)..... 150°C

Supply Voltage to Ground Potential .....–2.0V to +7.0V[1]

DC Output Current per Pin[1] ..... –25 mA to +25 mA

DC Input Voltage[1] .....–2.0V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	–40°C to +85°C	5V ± 10%

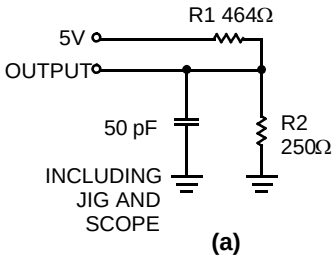
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage	Maximum V_{CC} rise time is 10 ms	4.75(4.5)	5.25(5.5)	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA DC[2]	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA DC[2]		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Current	V_I = V_{CC} or ground	–10	+10	µA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or ground	–40	+40	µA
t_R	Recommended Input Rise Time			100	ns
t_F	Recommended Input Fall Time			100	ns

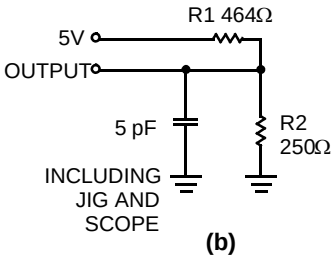
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1.0 MHz	20	pF

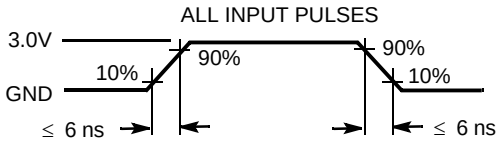
AC Test Loads and Waveforms



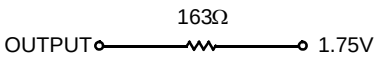
(a)



(b)



Equivalent to: THÉVENIN EQUIVALENT (commercial/military)



Notes:

1. Minimum DC input is –0.3V. During transactions, input may undershoot to –2.0V or overshoot to 7.0V for input currents less then 100 mA and periods shorter than 20 ns.
2. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.

Commercial and Industrial External Synchronous Switching Characteristics Over Operating Range

Parameter	Description	7C342B-15		7C342B-20		Unit
		Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[3]		15		20	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[3]		25		33	ns
t_{SU}	Global Clock Set-Up Time	10		13		ns
t_{CO1}	Synchronous Clock Input to Output Delay[3]		8		9	ns
t_{H}	Input Hold Time from Synchronous Clock Input	0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	5		7		ns
t_{WL}	Synchronous Clock Input LOW Time	5		7		ns
f_{MAX}	Maximum Register Toggle Frequency[4]	100		71.4		MHz
t_{CNT}	Minimum Global Clock Period		12		15	ns
f_{CNT}	Maximum Internal Global Clock Frequency[5]	83.3		66.7		MHZ

Commercial and Industrial External Synchronous Switching Characteristics Over Operating Range

Parameter	Description	7C342B-25		7C342B-30		7C342B-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[3]		25		30		35	ns
t_{PD2}	I/O Input to Combinatorial Output Delay[3]		40		45		55	ns
t_{SU}	Global Clock Set-Up Time	15		20		25		ns
t_{CO1}	Synchronous Clock Input to Output Delay[3]		14		16		20	ns
t_{H}	Input Hold Time from Synchronous Clock Input	0		0		0		ns
t_{WH}	Synchronous Clock Input HIGH Time	8		10		12.5		ns
t_{WL}	Synchronous Clock Input LOW Time	8		10		12.5		ns
f_{MAX}	Maximum Register Toggle Frequency[4]	62.5		50		40		MHz
t_{CNT}	Minimum Global Clock Period		20		25		30	ns
t_{ODH}	Output Data Hold Time After Clock	2		2		2		ns
f_{CNT}	Maximum Internal Global Clock Frequency[5]	50		40		33.3		MHz

Commercial and Industrial External Asynchronous Switching Characteristics Over Operating Range

Parameter	Description	7C342B-15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[3]		15		20	ns
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[6]	5		6		ns
t_{AH}	Input Hold Time from Asynchronous Clock Input	5		6		ns
t_{AWH}	Asynchronous Clock Input HIGH Time[6]	5		7		ns
t_{AWL}	Asynchronous Clock Input LOW Time[6]	5		7		ns
t_{ACNT}	Minimum Internal Array Clock Frequency		12		15	ns
f_{ACNT}	Maximum Internal Array Clock Frequency[5]	83.3		66.7		MHz
t_{ACO1}	Asynchronous Clock Input to Output Delay[3]		25		30	
t_{AS1}	Dedicated Input or Feedback Set-Up Time to Asynchronous Clock Input[5]	5		6		10
t_{AH}	Input Hold Time from Asynchronous Clock Input	6		8		10

Notes:

3. C1 = 35 pF.
4. The f_{MAX} values represent the highest frequency for pipeline data.
5. This parameter is measured with a 16-bit counter programmed into each LAB
6. This parameter is measured with a positive-edge triggered clock at the register. For negative edge triggering, the t_{AWH} and t_{AWL} parameters must be swapped.

Commercial and Industrial External Asynchronous Switching Characteristics Over Operating Range (continued)

Parameter	Description	7C342B-15		7C342B–20		Unit
		Min.	Max.	Min.	Max.	
t_{AWH}	Asynchronous Clock Input HIGH Time[5]	11		14		16
t_{AWL}	Asynchronous Clock Input LOW Time[5]	9		11		14
t_{ACNT}	Minimum Internal Array Clock Frequency		20		25	
f_{ACNT}	Maximum Internal Array Clock Frequency[5]	50		40		33.3

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range

Parameter	Description	7C342B-15		7C342B-20		Unit
		Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay		3		4	ns
t_{IO}	I/O Input Pad and Buffer Delay		3		4	ns
t_{EXP}	Expander Array Delay		8		10	ns
t_{LAD}	Logic Array Data Delay		8		12	ns
t_{LAC}	Logic Array Control Delay		5		5	ns
t_{OD}	Output Buffer and Pad Delay[3]		3		3	ns
t_{ZX}[8]	Output Buffer Enable Delay[3]		5		5	ns
t_{XZ}	Output Buffer Disable Delay[7]		5		5	ns
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	2		1		ns
t_{RH}	Register Hold Time Relative to Clock Signal at Register	7		10		ns
t_{LATCH}	Flow Through Latch Delay		1		1	ns
t_{RD}	Register Delay		1		1	ns
t_{COMB}[9]	Transparent Mode Delay		1		1	ns
t_{IC}	Asynchronous Clock Logic Delay		6		8	ns
t_{ICS}	Synchronous Clock Delay		0		0	ns
t_{FD}	Feedback Delay		1		1	ns
t_{PRE}	Asynchronous Register Preset Time		3		3	ns
t_{CLR}	Asynchronous Register Clear Time		3		3	ns
t_{PIA}	Programmable Interconnect Array Delay Time		10		13	ns
t_{IN}	Dedicated Input Pad and Buffer Delay		5		7	
t_{IO}	I/O Input Pad and Buffer Delay		6		6	
t_{EXP}	Expander Array Delay		12		14	
t_{LAD}	Logic Array Data Delay		12		14	
t_{LAC}	Logic Array Control Delay		10		12	
t_{OD}	Output Buffer and Pad Delay[3]		5		5	
t_{ZX}[8]	Output Buffer Enable Delay[3]		10		11	
t_{XZ}	Output Buffer Disable Delay[7]		10		11	
t_{RSU}	Register Set-Up Time Relative to Clock Signal at Register	6		8		10
t_{RH}	Register Hold Time Relative to Clock Signal at Register	4		6		8
t_{LATCH}	Flow Through Latch Delay		3		4	
t_{RD}	Register Delay		1		2	

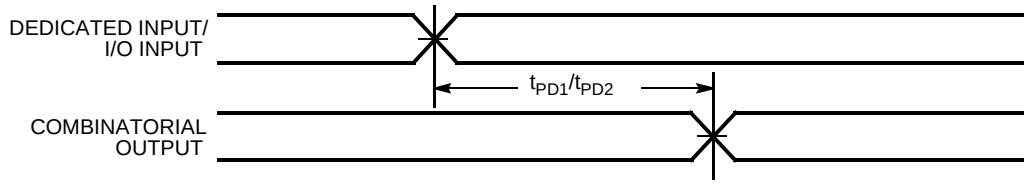
Notes:
7. C1 = 5 pF.
8. Sample tested only for an output change of 500 mV.
9. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

Commercial and Industrial Typical Internal Switching Characteristics Over Operating Range (continued)

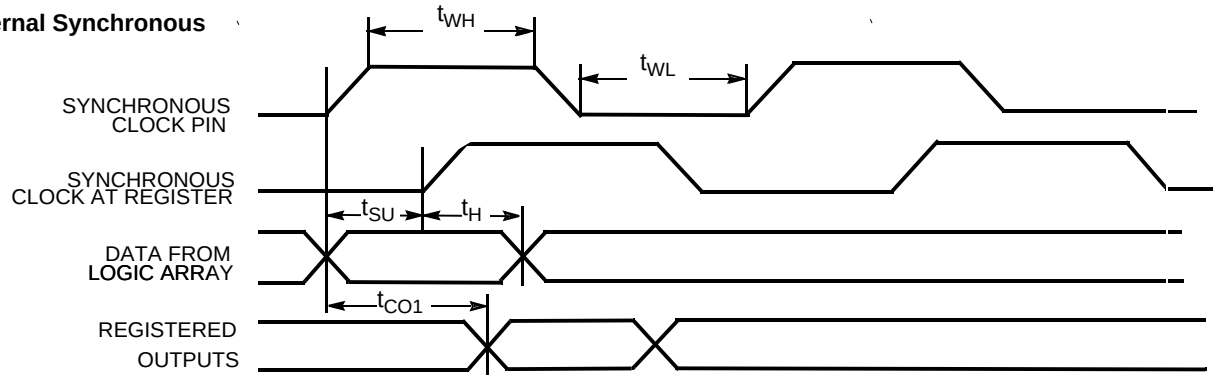
Parameter	Description	7C342B-25		7C342B-30		7C342B-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{COMB}[9]	Transparent Mode Delay		3		4		4	ns
t_{IC}	Asynchronous Clock Logic Delay		14		16		16	ns
t_{ICS}	Synchronous Clock Delay		3		2		1	ns
t_{FD}	Feedback Delay		1		1		2	ns
t_{PRE}	Asynchronous Register Preset Time		5		6		7	ns
t_{CLR}	Asynchronous Register Clear Time		5		6		7	ns
t_{PIA}	Programmable Interconnect Array Delay Time		14		16		20	ns

Switching Waveforms

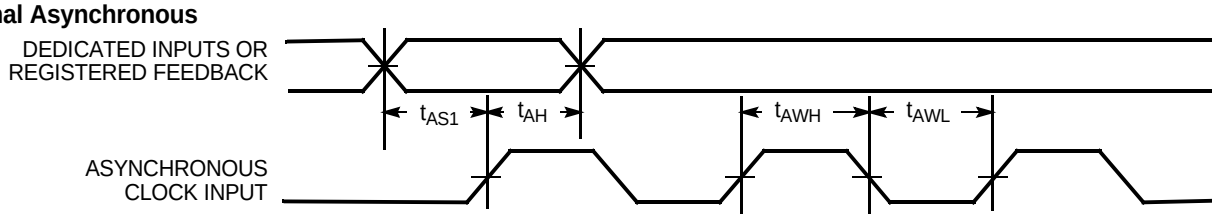
External Combinatorial



External Synchronous

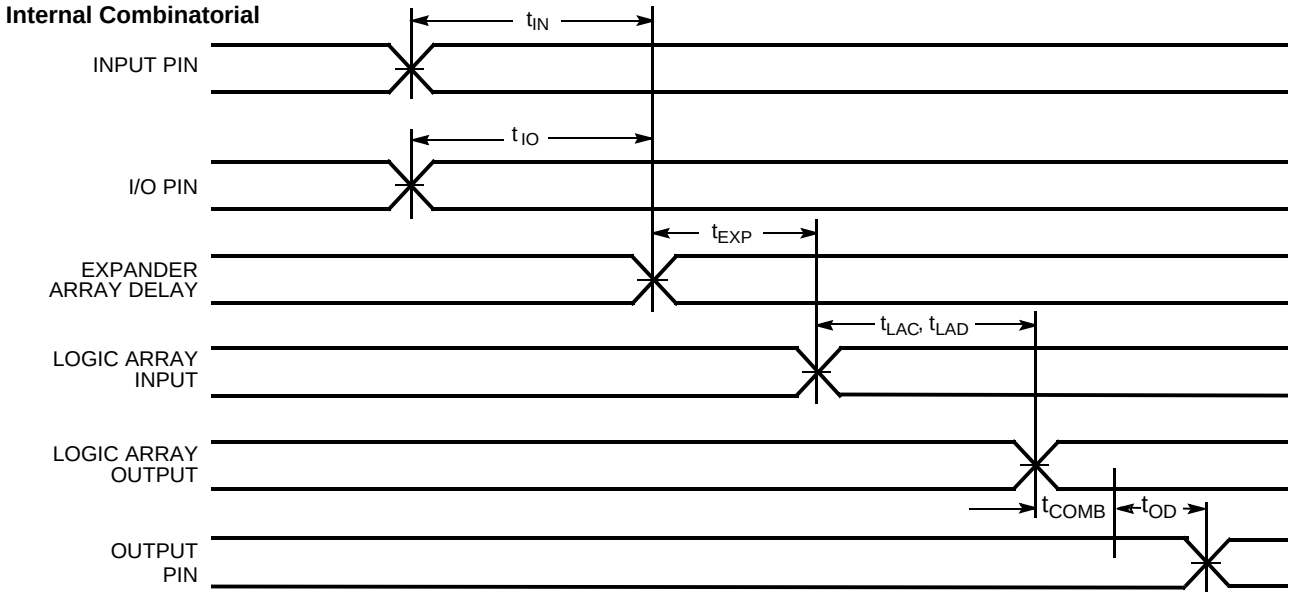


External Asynchronous

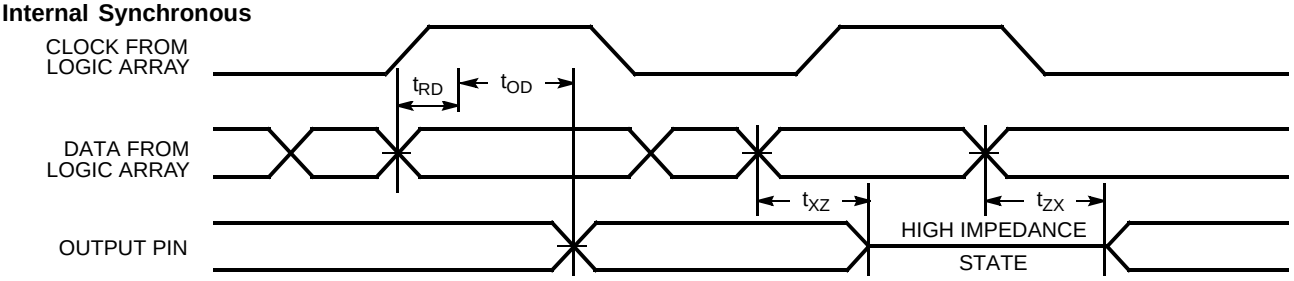


Switching Waveforms (continued)

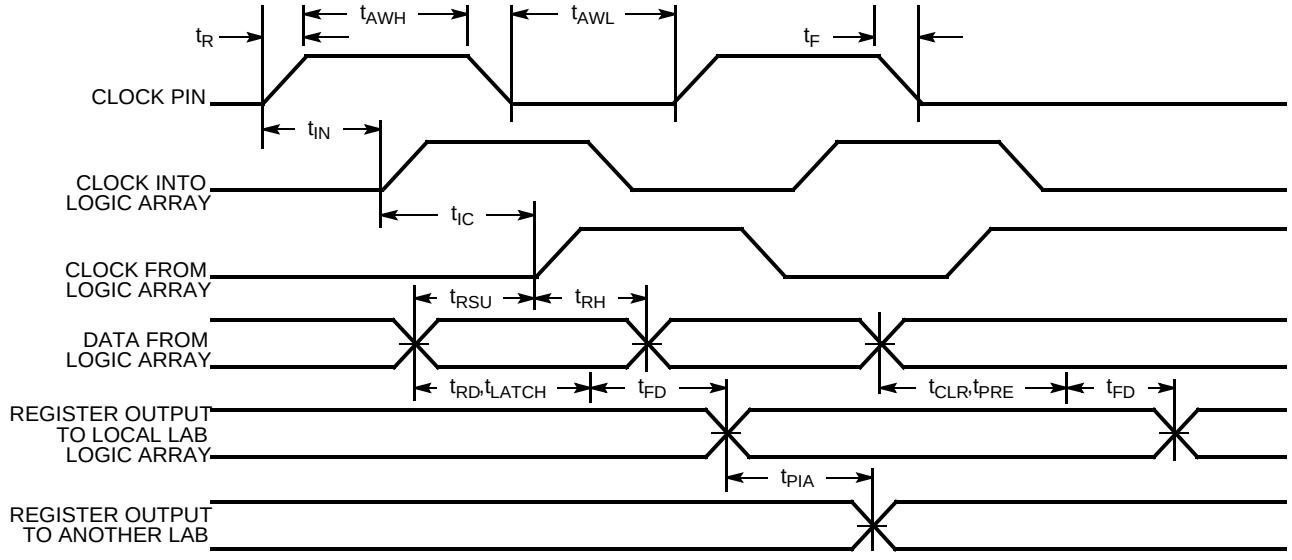
Internal Combinatorial



Internal Synchronous

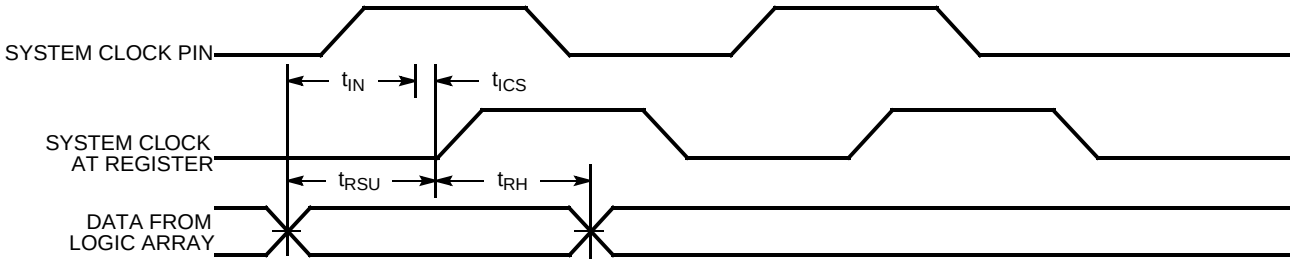


Internal Asynchronous



Switching Waveforms (continued)

Internal Synchronous

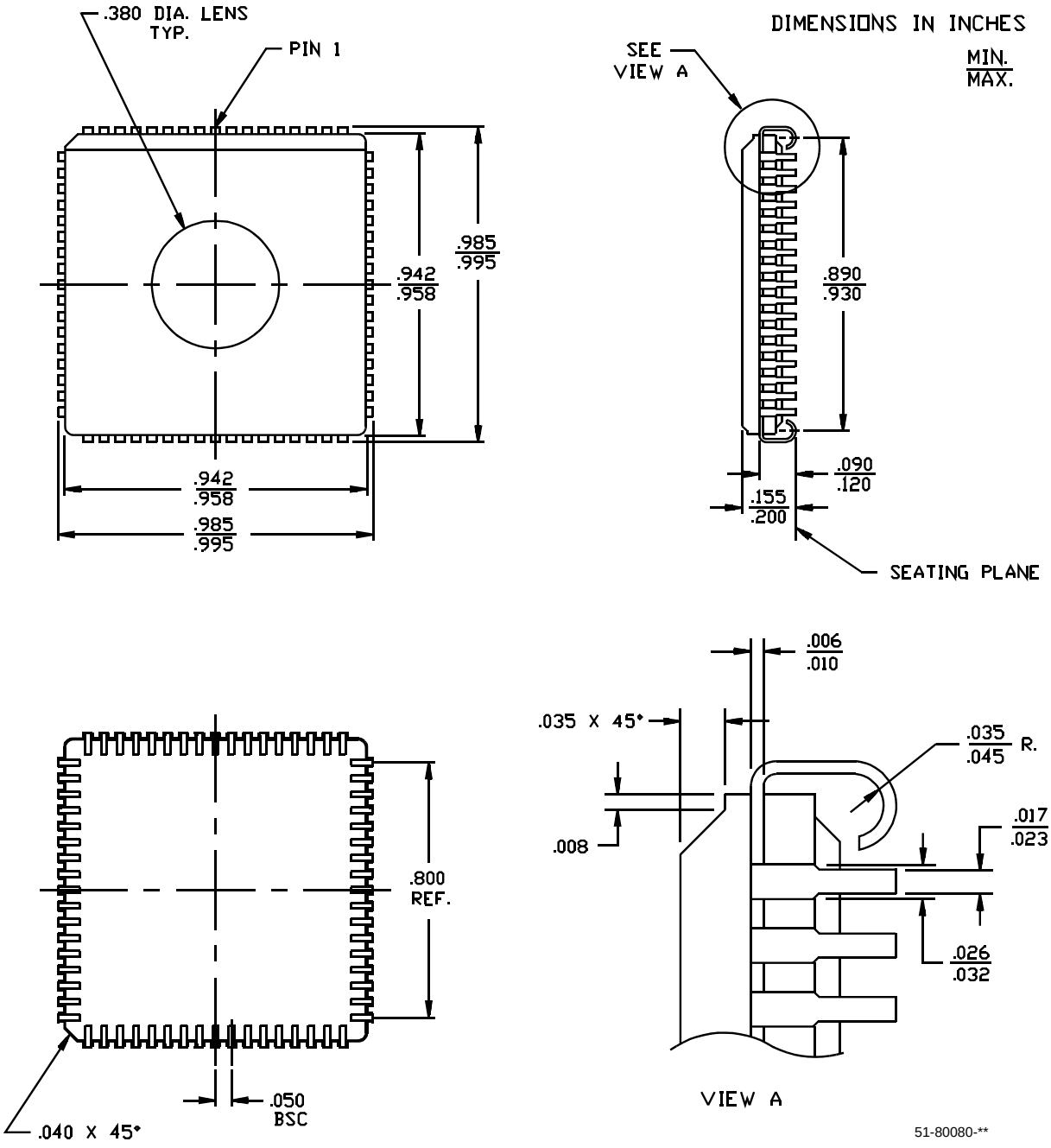


Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C342B-15JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
20	CY7C342B-20JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
25	CY7C342B-25HC/HI	H81	68-pin Windowed Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B-25JC/JI	J81	68-lead Plastic Leaded Chip Carrier	
	CY7C342B-25RC/RI	R68	68-pin Windowed Ceramic Pin Grid Array	
30	CY7C342B-30JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
35	CY7C342B-35JC/JI	J81	68-lead Plastic Leaded Chip Carrier	Commercial/ Industrial
	CY7C342B-35RJ/RI	R68	68-pin Windowed Ceramic Pin Grid Array	

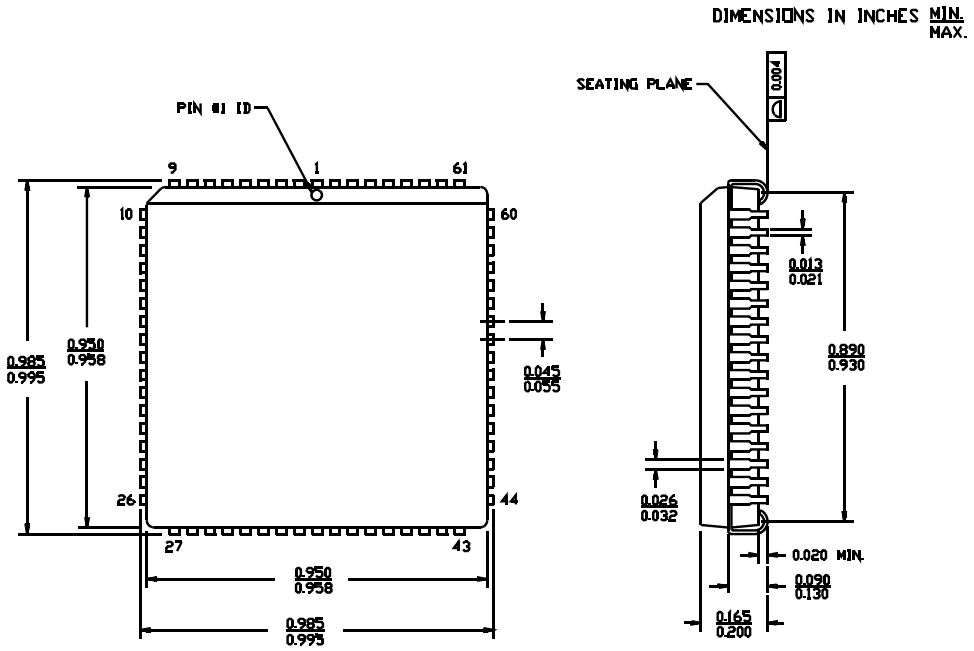
Package Diagrams

68-pin Windowed Leaded Chip Carrier H81



Package Diagrams (continued)

68-lead Plastic Leaded Chip Carrier J81



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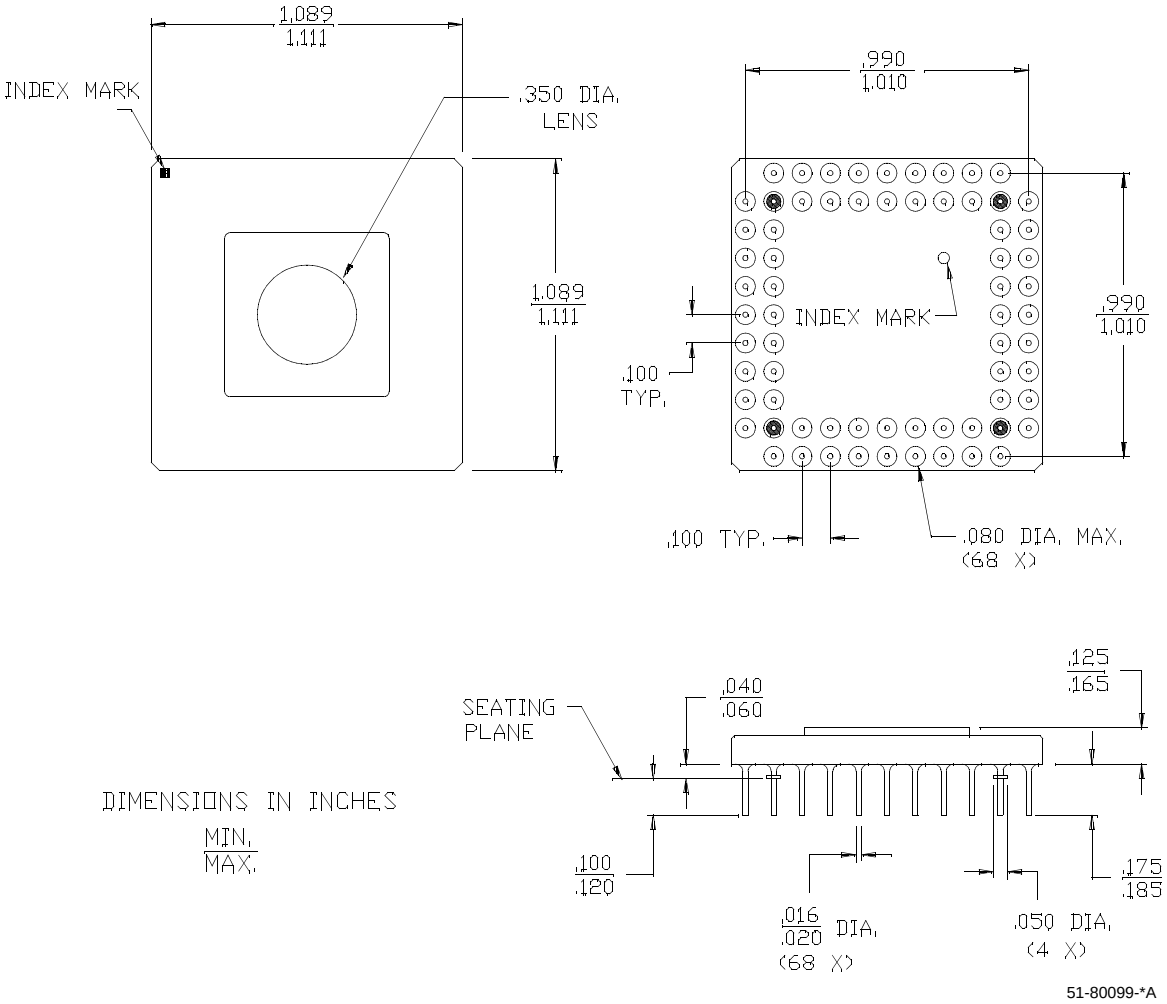
Package Diagrams (continued)

68-Pin Windowed PGA Ceramic R68



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Document History Page

Document Title: CY7C342B 128-Macrocell MAX® EPLD Document Number: 38-03014				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106314	04/25/01	SZV	Change from Spec number: 38-00119 to 38-03014
*A	113612	04/11/02	OOR	PGA package diagram dimensions were updated
*B	213375	See ECN	FSG	Added note to title page: “Use Ultra37000 For All New Designs”

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