8-/10-/12-Bit, High Bandwidth, Multiplying DACs with Parallel Interface

AD5424/AD5433/AD5445*

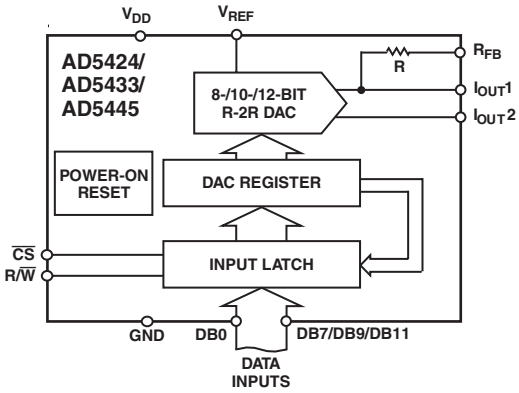
FEATURES

2.5 V to 5.5 V Supply Operation
Fast Parallel Interface (17 ns Write Cycle)
10 MHz Multiplying Bandwidth
±10 V Reference Input
Extended Temperature Range –40°C to +125°C
20-Lead TSSOP and Chip Scale (4 mm × 4 mm) Packages
8-, 10-, and 12-Bit Current Output DACs
Upgrades to AD7524/AD7533/AD7545
Pin Compatible 8-, 10-, and 12-Bit DACs in Chip Scale
Guaranteed Monotonic
4-Quadrant Multiplication
Power-On Reset with Brownout Detection
Readback Function
0.4 μA Typical Power Consumption

APPLICATIONS

Portable Battery-Powered Applications
Waveform Generators
Analog Processing
Instrumentation Applications
Programmable Amplifiers and Attenuators
Digitally-Controlled Calibration
Programmable Filters and Oscillators
Composite Video
Ultrasound
Gain, Offset, and Voltage Trimming

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5424/AD5433/AD5445 are CMOS 8-, 10-, and 12-bit current output digital-to-analog converters (DACs), respectively.

These devices operate from a 2.5 V to 5.5 V power supply, making them suited to battery-powered applications and many other applications.

These DACs utilize data readback allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with 0s and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS submicron process, they offer excellent 4-quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10 MHz.

The applied external reference input voltage (V_{REF}) determines the full-scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full-scale voltage output when combined with an external I-to-V precision amplifier.

While these devices are upgrades of AD7524/AD7533/AD7545 in multiplying bandwidth performance, they have a latched interface and cannot be used in transparent mode.

The AD5424 is available in small 20-lead LFCSP and 16-lead TSSOP packages, while the AD5433/AD5445 DACs are available in small 20-lead LFCSP and TSSOP packages.

*U.S. Patent No. 5,689,257

REV. 0

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AD5424/AD5433/AD5445–SPECIFICATIONS[1]

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = 10 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. DC performance measured with OP1177, AC performance with AD8038, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Conditions
STATIC PERFORMANCE					
AD5424					
Resolution			8	Bits	
Relative Accuracy			±0.25	LSB	
Differential Nonlinearity			±0.5	LSB	Guaranteed monotonic
AD5433					
Resolution			10	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
AD5445					
Resolution			12	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			–1/+2	LSB	Guaranteed monotonic
Gain Error			±10	mV	
Gain Error Temperature Coefficient[2]		±5		ppm FSR/°C	
Output Leakage Current[2]			±10	nA	Data = 0x0000, T_A = 25°C, $I_{OUT}1$
			±20	nA	Data = 0x0000, $I_{OUT}1$
REFERENCE INPUT[2]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = –50 ppm/°C
R_{FB} Resistance	8	10	12	kΩ	Input resistance TC = –50 ppm/°C
Input Capacitance					
Code 0		3	6	pF	
Code 4095		5	8	pF	
DIGITAL INPUTS/OUTPUT[2]					
Input High Voltage, V_{IH}	1.7			V	
Input Low Voltage, V_{IL}			0.6	V	
Input Leakage Current, I_{IL}			1	μA	
Input Capacitance		4	10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} – 1			V	I_{SOURCE} = 200 μA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} – 0.5			V	I_{SOURCE} = 200 μA
DYNAMIC PERFORMANCE[2]					
Reference Multiplying Bandwidth		10		MHz	V_{REF} = ±3.5 V; DAC loaded all 1s
Output Voltage Settling Time					V_{REF} = 10 V, R_{LOAD} = 100 Ω, C_{LOAD} = 15 pF
AD5424		30	60	ns	Measured to ±16 mV of full scale
AD5433		35	70	ns	Measured to ±4 mV of full scale
AD5445		80	120	ns	Measured to ±1 mV of full scale
Digital Delay		20	40	ns	Interface delay time
10% to 90% Settling Time		15	30	ns	Rise and Fall time, V_{REF} = 10 V, R_{LOAD} = 100 Ω
Digital to Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, V_{REF} = 0 V
Multiplying Feedthrough Error					DAC latch loaded with all 0s. V_{REF} = ±3.5 V
		70		dB	Reference = 1 MHz
		48		dB	Reference = 10 MHz

Parameter	Min	Typ	Max	Unit	Conditions
Output Capacitance					
$I_{OUT}2$		22	25	pF	All 0s loaded
		10	12	pF	All 1s loaded
$I_{OUT}1$		12	17	pF	All 0s loaded
		25	30	pF	All 1s loaded
Digital Feedthrough		1		nV-s	Feedthrough to DAC output with $\overline{CS}$ high and alternate loading of all 0s and all 1s
Total Harmonic Distortion		–81		dB	V_{REF} = 3.5 V pk-pk; all 1s loaded, f = 100 kHz
Digital THD					
Clock = 10 MHz					
50 kHz f_{OUT}		65		dB	
Output Noise Spectral Density		25		nV$\sqrt{Hz}$	@ 1 kHz
SFDR Performance (Wide Band)					AD5445, 65k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		55		dB	
100 kHz f_{OUT}		63		dB	
50 kHz f_{OUT}		65		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		50		dB	
100 kHz f_{OUT}		60		dB	
50 kHz f_{OUT}		62		dB	
SFDR Performance (Narrow Band)					AD5445, 65k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
500 kHz f_{OUT}		73		dB	
100 kHz f_{OUT}		80		dB	
50 kHz f_{OUT}		87		dB	
Clock = 25 MHz					
500 kHz f_{OUT}		70		dB	
100 kHz f_{OUT}		75		dB	
50 kHz f_{OUT}		80		dB	
Intermodulation Distortion					AD5445, 65k codes, V_{REF} = 3.5 V
Clock = 10 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		65		dB	
f_1 = 40 kHz, f_2 = 50 kHz		72		dB	
Clock = 25 MHz					
f_1 = 400 kHz, f_2 = 500 kHz		51		dB	
f_1 = 40 kHz, f_2 = 50 kHz		65		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			0.6	μA	T_A = 25°C, logic inputs = 0 V or V_{DD}
		0.4	5	μA	Logic inputs = 0 V or V_{DD}

NOTES
[1]Temperature range is as follows: Y version: –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{REF} = 5 V, I_{OUT}2 = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	V_{DD} = 2.5 V to 5.5 V	V_{DD} = 4.5 V to 5.5 V	Unit	Conditions/Comments
t_1	0	0	ns min	R/$\overline{W}$ to $\overline{CS}$ setup time
t_2	0	0	ns min	R/$\overline{W}$ to $\overline{CS}$ hold time
t_3	10	10	ns min	$\overline{CS}$ low time (write cycle)
t_4	6	6	ns min	Data setup time
t_5	0	0	ns min	Data hold time
t_6	5	5	ns min	R/$\overline{W}$ high to $\overline{CS}$ low
t_7	9	7	ns min	$\overline{CS}$ min high time
t_8	20	10	ns typ	Data access time
	40	20	ns max	
t_9	5	5	ns typ	Bus relinquish time
	10	10	ns max	

NOTES

[1]See Figure 1. Temperature range is as follows: Y version: –40°C to +125°C. Guaranteed by design and characterization, not subject to production test.

[2]All input signals are specified with tr = tf = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. Digital output timing measured with load circuit in Figure 2.

Specifications subject to change without notice.

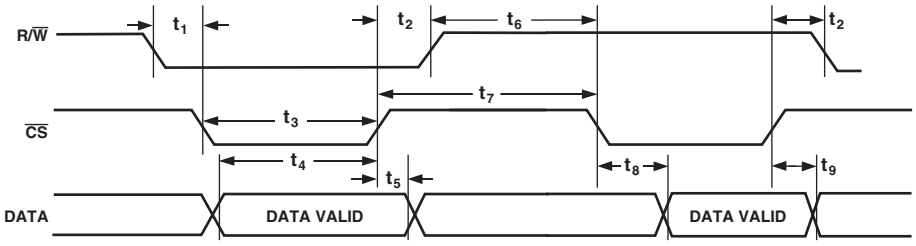


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +7 V
V_{REF}, R_{FB} to GND . . . . . –12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND . . . . . –0.3 V to +7 V
Logic Inputs and Output[2] . . . . . –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Extended Industrial (Y Version) . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
16-Lead TSSOP θ_{JA} Thermal Impedance . . . . . 150°C/W
20-Lead TSSOP θ_{JA} Thermal Impedance . . . . . 143°C/W
20-Lead LFCSP θ_{JA} Thermal Impedance . . . . . 135°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature (<20 seconds) . . . . . 235°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2] Overvoltages at DBx, $\overline{CS}$, and R/$\overline{W}$, will be clamped by internal diodes.

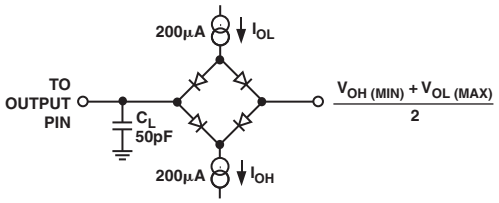


Figure 2. Load Circuit for Data Output Timing Specifications

ORDERING GUIDE

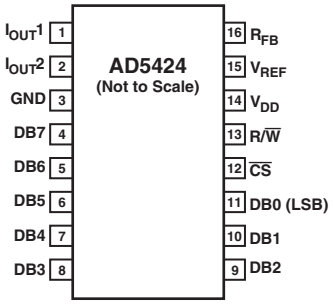
Model	Resolution (Bits)	INL (LSB)	Temperature Range	Package Description	Package Option
AD5424YRU	8	±0.25	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-16
AD5424YRU-REEL	8	±0.25	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5424YRU-REEL7	8	±0.25	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5424YCP	8	±0.25	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5424YCP-REEL	8	±0.25	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5424YCP-REEL7	8	±0.25	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5433YRU	10	±0.5	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5433YRU-REEL	10	±0.5	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5433YRU-REEL7	10	±0.5	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5433YCP	10	±0.5	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5433YCP-REEL	10	±0.5	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5433YCP-REEL7	10	±0.5	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5445YRU	12	±1	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5445YRU-REEL	12	±1	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5445YRU-REEL7	12	±1	–40°C to +125°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5445YCP	12	±1	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5445YCP-REEL	12	±1	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
AD5445YCP-REEL7	12	±1	–40°C to +125°C	LFCSP (Chip Scale Package)	CP-20
EVAL-AD5424EB				Evaluation Kit	
EVAL-AD5433EB				Evaluation Kit	
EVAL-AD5445EB				Evaluation Kit	

CAUTION

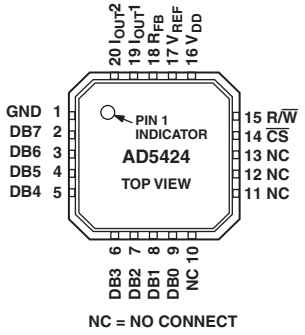
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5424/AD5433/AD5445 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

TSSOP



LFCSP



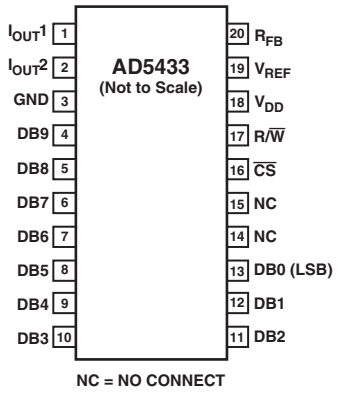
NC = NO CONNECT

AD5424 PIN FUNCTION DESCRIPTIONS

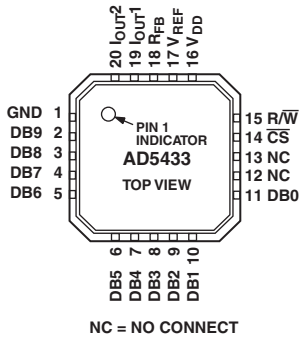
Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground
4–11	2–9	DB7–DB0	Parallel Data Bits 7 to 0.
	10–13	NC	No Internal Connection.
12	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
13	15	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to readback contents of DAC register.
14	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
15	17	V_{REF}	DAC Reference Voltage Input Terminal.
16	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATIONS

TSSOP



LFCSP

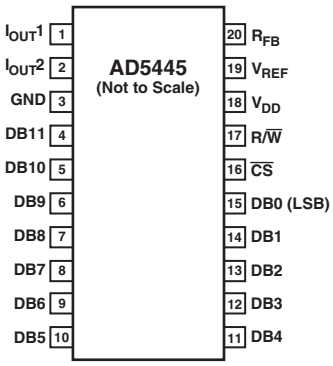


AD5433 PIN FUNCTION DESCRIPTIONS

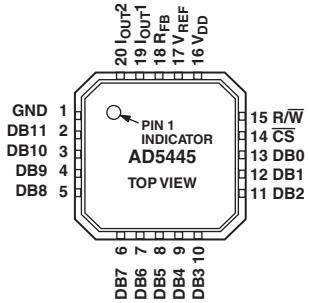
Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground
4–13	2–11	DB9–DB0	Parallel Data Bits 9 to 0.
14, 15	12, 13	NC	Not Internally Connected.
16	14	$\overline{CS}$	Chip Select Input. Active low. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register. Rising edge of $\overline{CS}$ loads data.
17	15	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to readback contents of DAC register.
18	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of 2.5 V to 5.5 V.
19	17	V_{REF}	DAC Reference Voltage Input Terminal.
20	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATIONS

TSSOP

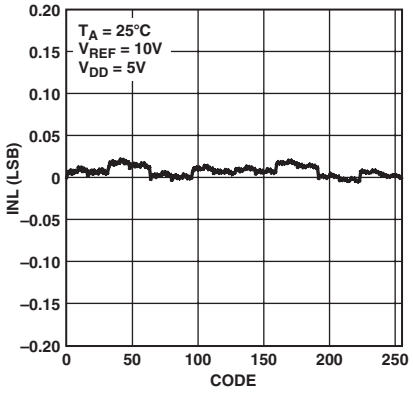


LFCSP

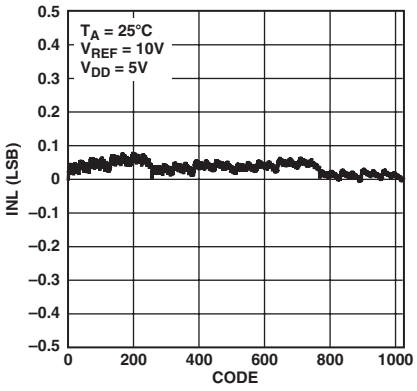


AD5445 PIN FUNCTION DESCRIPTIONS

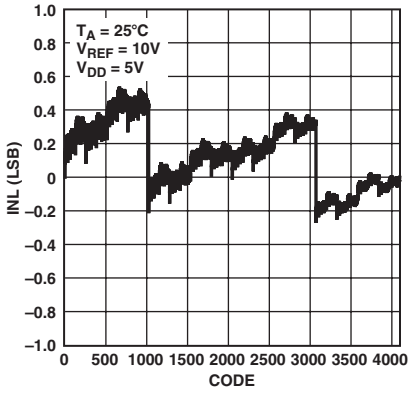
Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4–15	2–13	DB11–DB0	Parallel Data Bits 11 to 0.
16	14	$\overline{CS}$	Chip Select Input. Active low. Rising edge of $\overline{CS}$ loads data. Used in conjunction with R/$\overline{W}$ to load parallel data to the input latch or to read data from the DAC register.
17	15	R/$\overline{W}$	Read/Write. When low, used in conjunction with $\overline{CS}$ to load parallel data. When high, use with $\overline{CS}$ to readback contents of DAC register.
18	16	V_{DD}	Positive Power Supply Input. These parts can be operated from a supply of +2.5 V to +5.5 V.
19	17	V_{REF}	DAC Reference Voltage Input Terminal.
20	18	R_{FB}	DAC Feedback Resistor Pin. Establish voltage output for the DAC by connecting to external amplifier output.



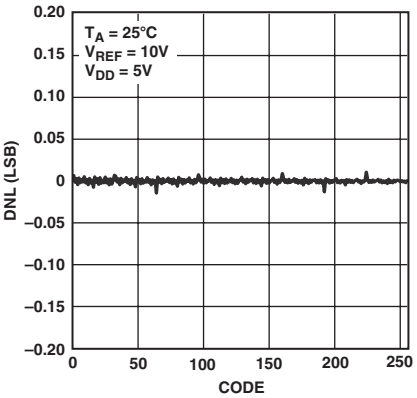
TPC 1. INL vs. Code (8-Bit DAC)



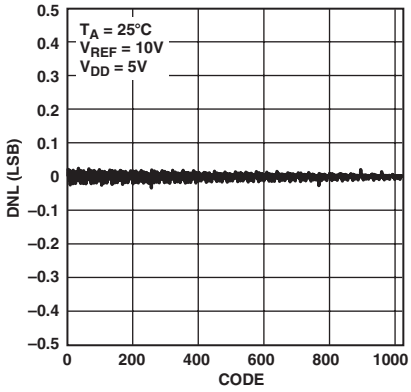
TPC 2. INL vs. Code (10-Bit DAC)



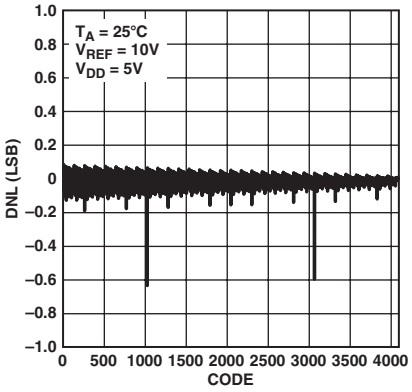
TPC 3. INL vs. Code (12-Bit DAC)



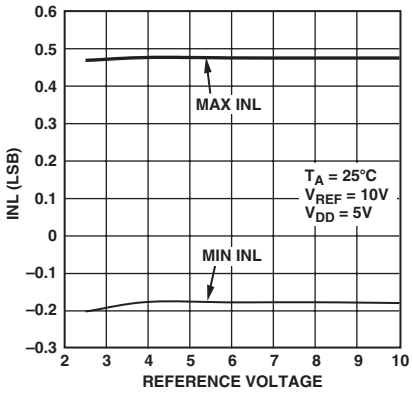
TPC 4. DNL vs. Code (8-Bit DAC)



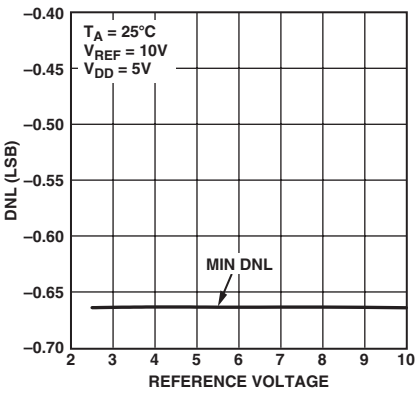
TPC 5. DNL vs. Code (10-Bit DAC)



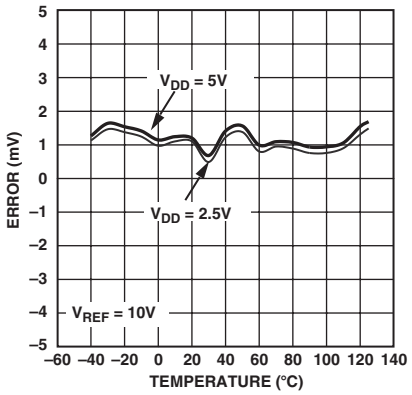
TPC 6. DNL vs. Code (12-Bit DAC)



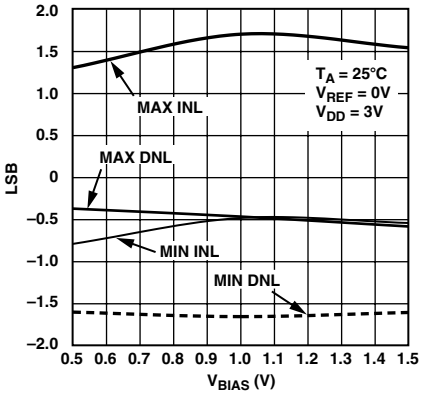
TPC 7. INL vs. Reference Voltage, AD5445



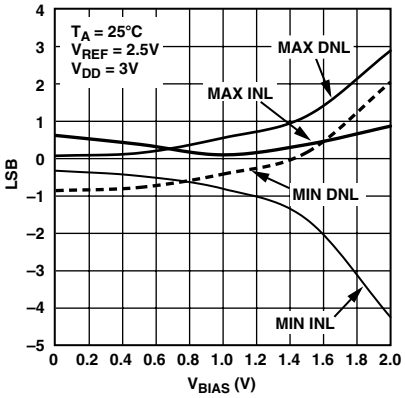
TPC 8. DNL vs. Reference Voltage, AD5445



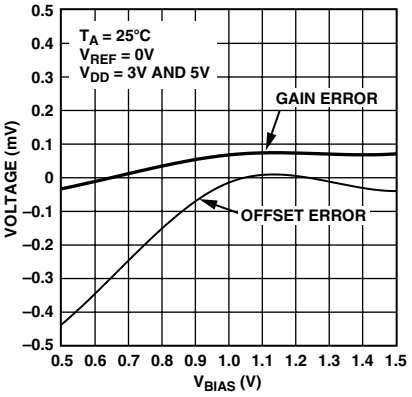
TPC 9. Gain Error vs. Temperature



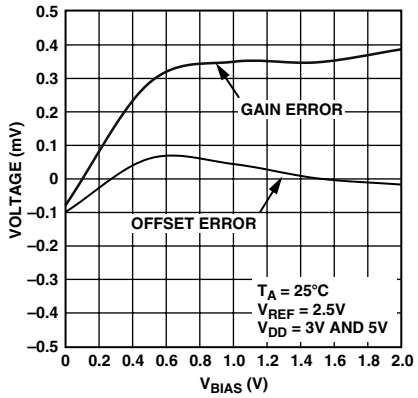
TPC 10. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445



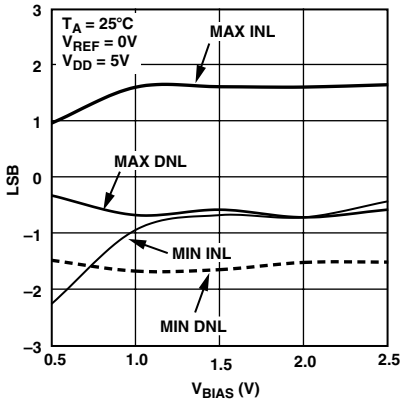
TPC 11. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445



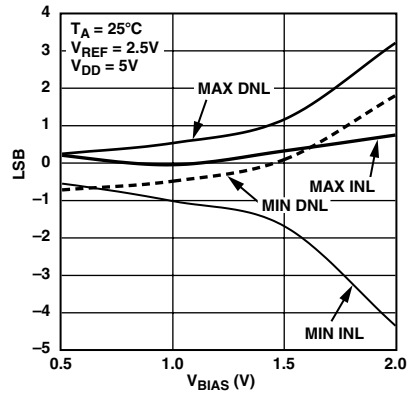
TPC 12. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$



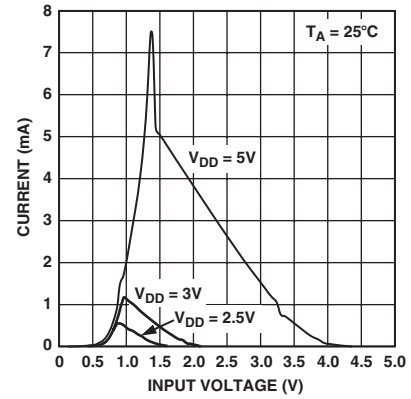
TPC 13. Gain and Offset Errors vs. V_{BIAS} Voltage Applied to $I_{OUT}2$



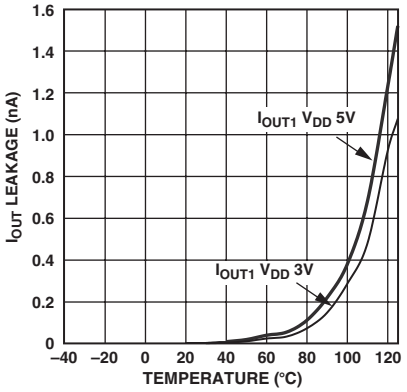
TPC 14. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445



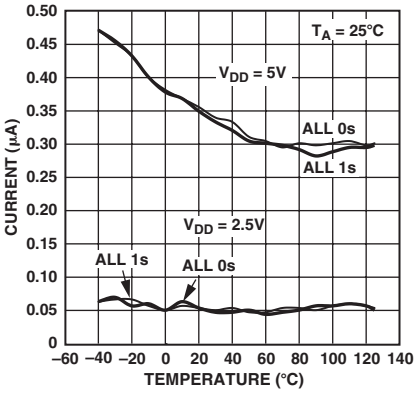
TPC 15. Linearity vs. V_{BIAS} Voltage Applied to $I_{OUT}2$, AD5445



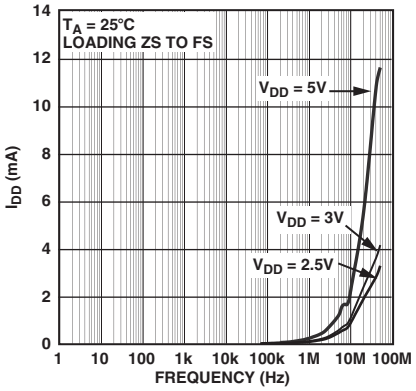
TPC 16. Supply Current vs. Logic Input Voltage (Driving DB0–DB11, All Other Digital Inputs @ Supplies)



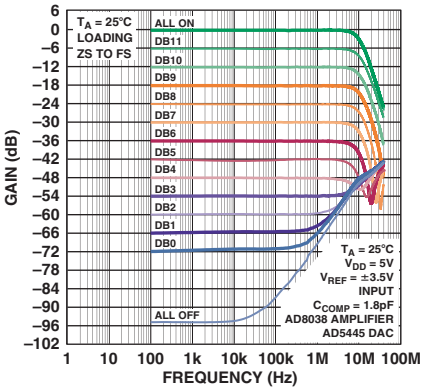
TPC 17. $I_{OUT}1$ Leakage Current vs. Temperature



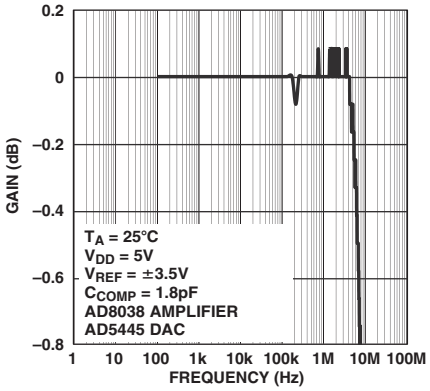
TPC 18. Supply Current vs. Temperature



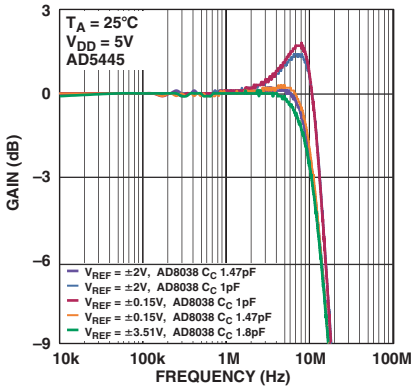
TPC 19. Supply Current vs. Update Rate



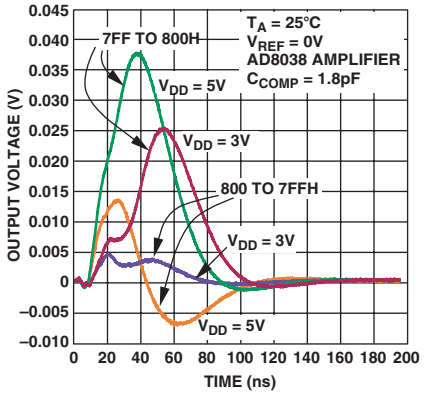
TPC 20. Reference Multiplying Bandwidth vs. Frequency and Code



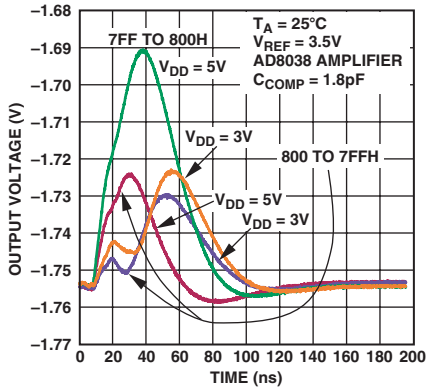
TPC 21. Reference Multiplying Bandwidth—All Ones Loaded



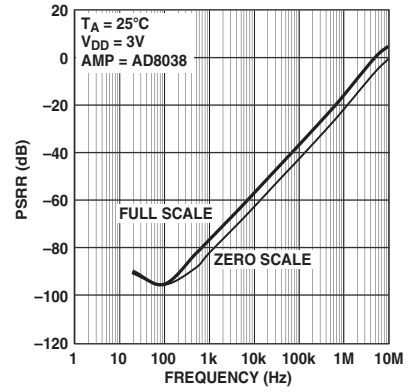
TPC 22. Reference Multiplying Bandwidth vs. Frequency and Compensation Capacitor



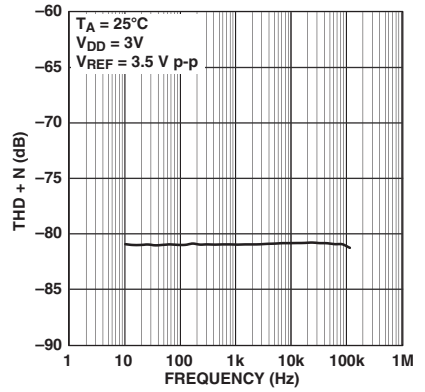
TPC 23. Midscale Transition, V_{REF} = 0 V



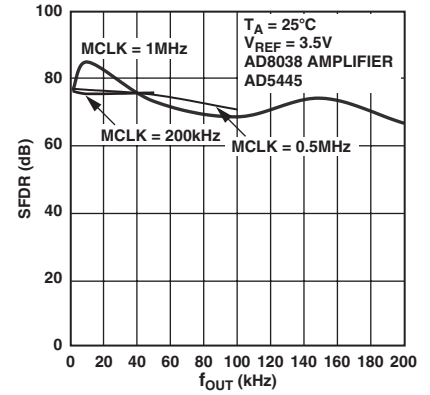
TPC 24. Midscale Transition, V_{REF} = 3.5 V



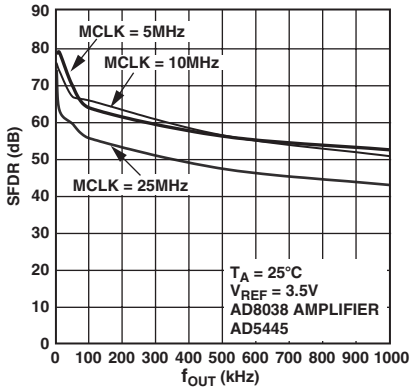
TPC 25. Power Supply Rejection vs. Frequency



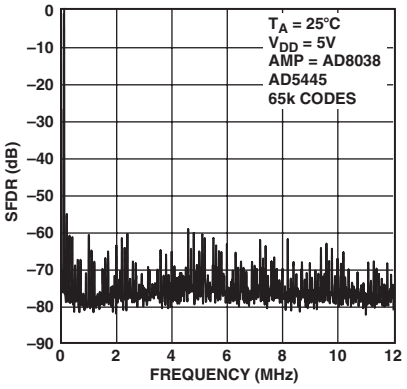
TPC 26. THD and Noise vs. Frequency



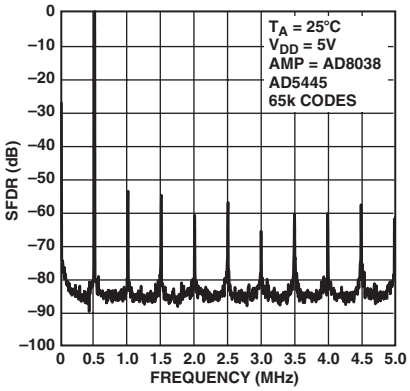
TPC 27. Wideband SFDR vs. f_{OUT} Frequency



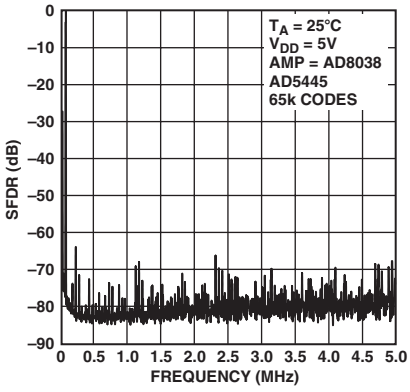
TPC 28. Wideband SFDR vs. f_{OUT} Frequency



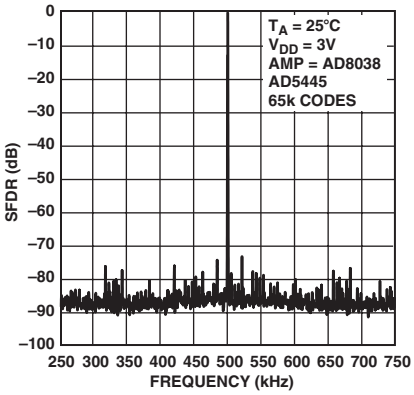
TPC 29. Wideband SFDR, f_{OUT} = 100 kHz, Clock = 25 MHz



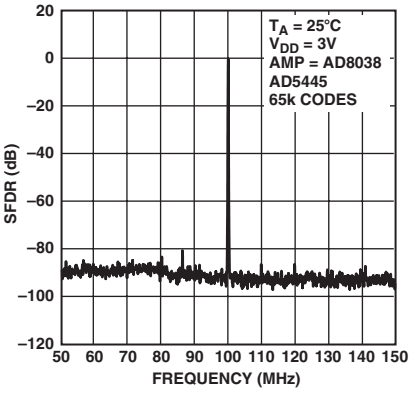
TPC 30. Wideband SFDR, f_{OUT} = 500 kHz, Clock = 10 MHz



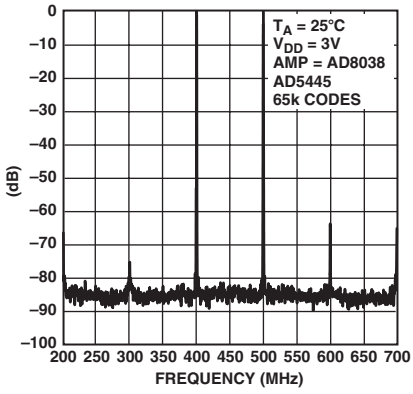
TPC 31. Wideband SFDR, f_{OUT} = 50 kHz, Clock = 10 MHz



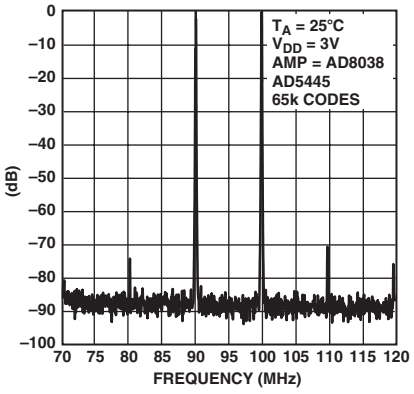
TPC 32. Narrow-Band Spectral Response, f_{OUT} = 500 kHz, Clock = 25 MHz



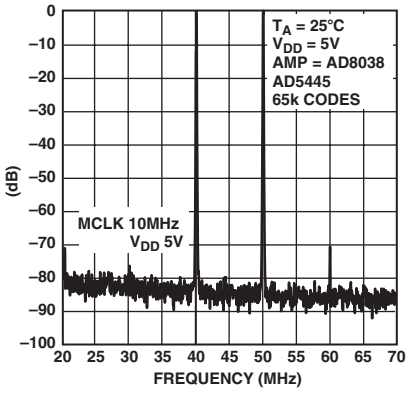
TPC 33. Narrow-Band SFDR, f_{OUT} = 100 kHz, MCLK = 25 MHz



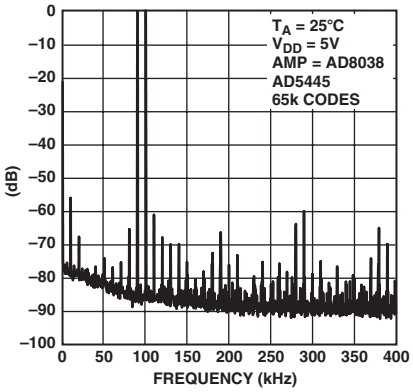
TPC 34. Narrow-Band IMD, f_{OUT} = 400 kHz, 500 kHz, Clock = 10 MHz



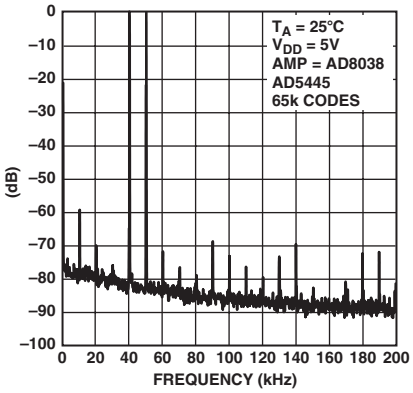
TPC 35. Narrow-Band IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 10 MHz



TPC 36. Narrow-Band IMD, f_{OUT} = 40 kHz, 50 kHz, Clock = 10 MHz



TPC 37. Wideband IMD, f_{OUT} = 90 kHz, 100 kHz, Clock = 25 MHz



TPC 38. Wideband IMD, f_{OUT} = 60 kHz, 50 kHz, Clock = 10 MHz

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for 0 and full scale and is normally expressed in LSBs or as a percentage of full-scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of –1 LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} – 1 LSB. Gain error of the DACs is adjustable to 0 with external resistance.

Output Leakage Current
Output leakage current is current that flows in the DAC ladder switches when these are turned off. For the $I_{OUT}1$ terminal, it can be measured by loading all 0s to the DAC and measuring the $I_{OUT}1$ current. Minimum current will flow in the $I_{OUT}2$ line when the DAC is loaded with all 1s.

Output Capacitance
Capacitance from $I_{OUT}1$ or $I_{OUT}2$ to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full scale input change. For these devices, it is specified with a 100 Ω resistor to ground.

The settling time specification includes the digital delay from $\overline{CS}$ rising edge to the full-scale output change.

Digital to Analog Glitch lmpulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs may be capacitively coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC $I_{OUT}1$ terminal, when all 0s are loaded to the DAC.

Total Harmonic Distortion (THD)
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonics are included, such as second to fifth.

$$THD = 20\log\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}$$

Digital Intermodulation Distortion
Second-order intermodulation distortion (IMD) measurements are the relative magnitude of the fa and fb tones generated digitally by the DAC and the second-order products at 2fa – fb and 2fb – fa.

Spurious-Free Dynamic Range (SFDR)
It is the usable dynamic range of a DAC before spurious noise interferes or distorts the fundamental signal. SFDR is the measure of difference in amplitude between the fundamental and the largest harmonically or nonharmonically related spur from dc to full Nyquist bandwidth (half the DAC sampling rate, or $f_S/2$). Narrow band SFDR is a measure of SFDR over an arbitrary window size, in this case 50% of the fundamental. Digital SFDR is a measure of the usable dynamic range of the DAC when the signal is digitally generated sine wave.

DAC SECTION

The AD5424, AD5433, and AD5445 are 8-, 10- and 12-bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-bit AD5424 is shown in Figure 3. The matching feedback resistor R_{FB} has a value of R. The value of R is typically 10 kΩ (minimum 8 kΩ and maximum 12 kΩ). If $I_{OUT}1$ and $I_{OUT}2$ are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant and nominally of resistance value R. The DAC output (I_{OUT}) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the DAC on the amplifiers inverting input node.

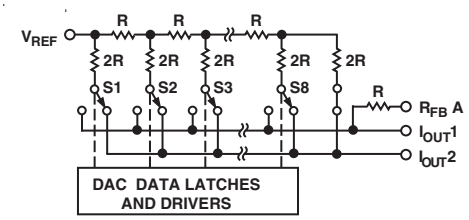


Figure 3. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, $I_{OUT}1$ and $I_{OUT}2$ terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, 4-quadrant multiplication in bipolar mode or in single-supply modes of operation. Note that a matching switch is used in series with the internal R_{FB} feedback resistor. If users attempt to measure R_{FB}, power must be applied to V_{DD} to achieve continuity.

PARALLEL INTERFACE

Data is loaded to the AD5424/33/45 in the format of an 8-, 10-, or 12-bit parallel word. Control lines $\overline{CS}$ and R/$\overline{W}$ allow data to be written to or read from the DAC register. A write event takes place when $\overline{CS}$ and R/$\overline{W}$ are brought low, data available on the data lines fills the shift register, and the rising edge of $\overline{CS}$ latches the data and transfers the latched data-word to the DAC register. The DAC latches are not transparent, thus a write sequence must consist of a falling and rising edge on $\overline{CS}$ to ensure data is loaded to the DAC register and its analog equivalent reflected on the DAC output.

A read event takes place when R/$\overline{W}$ is held high and $\overline{CS}$ is brought low. Now data is loaded from the DAC register back to the input register and out onto the data line where it can be read back to the controller for verification or diagnostic purposes.

CIRCUIT OPERATION

Unipolar Mode

Using a single op amp, these devices can easily be configured to provide 2-quadrant multiplying operation or a unipolar output voltage swing as shown in Figure 4.

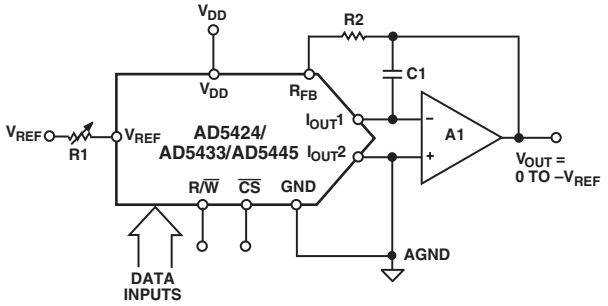


Figure 4. Unipolar Operation

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times \frac{D}{2^n}$$

where *D* is the fractional representation of the digital word loaded to the DAC and *n* is the resolution of the DAC.

D = 0 to 255 (8-Bit AD5424)
= 0 to 1023 (10-Bit AD5433)
= 0 to 4095 (12-Bit AD5445)

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal digital logic to drive the DAC switches' on and off states.

These DACs are also designed to accommodate ac reference input signals in the range of –10 V to +10 V.

With a fixed 10 V reference, the circuit shown in Figure 4 will give a unipolar 0 V to –10 V output voltage swing. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication.

Table I shows the relationship between digital code and expected output voltage for unipolar operation. (AD5424, 8-bit device).

Table I. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

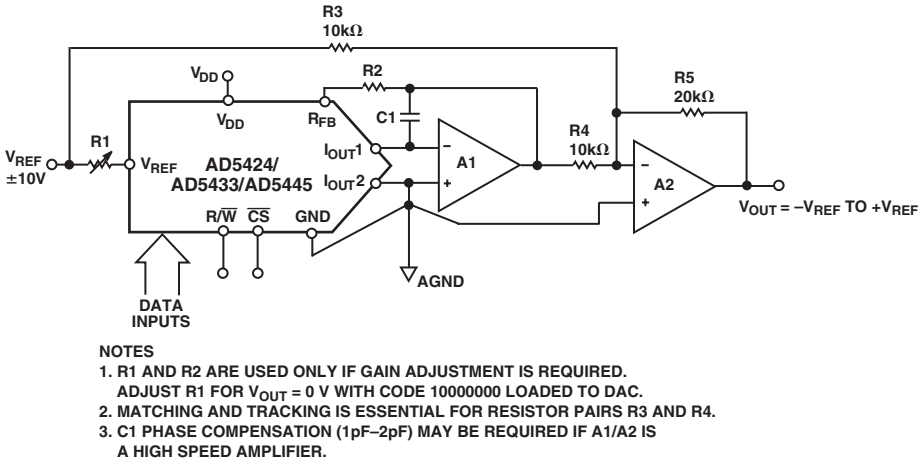


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Bipolar Operation

In some applications, it may be necessary to generate full 4-quadrant multiplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors as shown in Figure 5. In this circuit, the second amplifier A2 provides a gain of 2. Biasing the external amplifier with an offset from the reference voltage results in full 4-quadrant multiplying operation. The transfer function of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero ($V_{OUT} = -V_{REF}$) to midscale ($V_{OUT} = 0$ V) to full scale ($V_{OUT} = +V_{REF}$).

$$V_{OUT} = \left(V_{REF} \times D/2^{n-1}\right) - V_{REF}$$

where *D* is the fractional representation of the digital word loaded to the DAC and *n* is the resolution of the DAC.

D = 0 to 255 (8-Bit AD5424)
= 0 to 1023 (10-Bit AD5433)
= 0 to 4095 (12-Bit AD5445)

When V_{IN} is an ac signal, the circuit performs 4-quadrant multiplication.

Table II shows the relationship between digital code and the expected output voltage for bipolar operation (AD5426, 8-bit device).

Table II. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

Stability

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout techniques must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node. This parasitic capacitance introduces a pole into the open-loop response, which can cause ringing or instability in closed-loop applications.

An optional compensation capacitor, C1, can be added in parallel with R_{FB} for stability as shown in Figures 4 and 5. Too small a value of C1 can produce ringing at the output, while too large a value can adversely affect the settling time. C1 should be found empirically but 1 pF to 2 pF is generally adequate for compensation.

SINGLE-SUPPLY APPLICATIONS

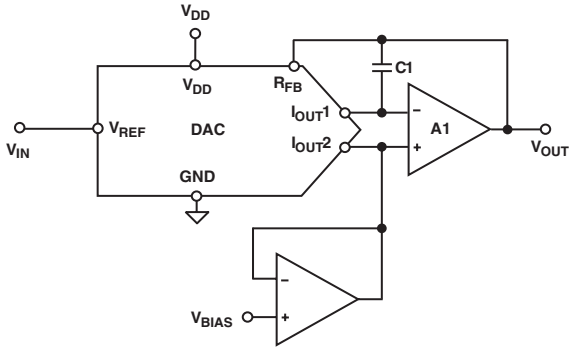
Current Mode Operation

Figure 6 shows a typical circuit for operation with a single 2.5 V to 5 V supply. In the current mode circuit of Figure 6, $I_{OUT}2$ and hence $I_{OUT}1$ is biased positive by the amount applied to V_{BIAS}. In this configuration, the output voltage is given by

$$V_{OUT} = \left\{D \times \left(R_{FB}/R_{DAC}\right) \times \left(V_{BIAS} - V_{IN}\right)\right\} + V_{BIAS}$$

As D varies from 0 to 255 (AD5424), 1023 (AD5433), or 4095 (AD5445), the output voltage varies from $V_{OUT} = V_{BIAS}$ to $V_{OUT} = 2\ V_{BIAS} - V_{IN}$.

V_{BIAS} should be a low impedance source capable of sinking and sourcing all possible variations in current at the $I_{OUT}2$ terminal.



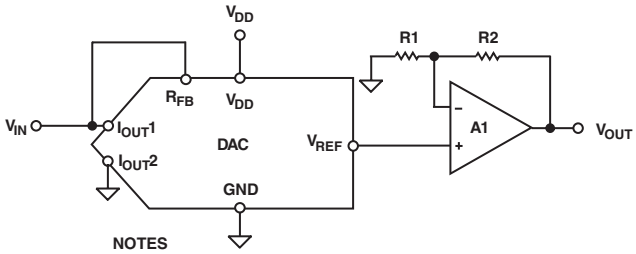
NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY
2. C1 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 6. Single-Supply Current Mode Operation

Voltage Switching Mode of Operation

Figure 7 shows these DACs operating in the voltage-switching mode. The reference voltage, V_{IN}, is applied to the $I_{OUT}1$ pin; $I_{OUT}2$ is connected to AGND; and the output voltage is available at the V_{REF} terminal. In this configuration, a positive reference voltage results in a positive output voltage making single-supply operation possible. The output from the DAC is voltage at a constant impedance (the DAC ladder resistance), thus an op amp is necessary to buffer the output voltage. The reference input no longer sees a constant input impedance, but one that varies with code. So, the voltage input should be driven from a low impedance source.

It is important to note that V_{IN} is limited to low voltages because the switches in the DAC ladder no longer have the same source-drain drive voltage. As a result, their on resistance differs, which degrades the linearity of the DAC. See TPCs 10–15. Also, V_{IN} must not go negative by more than 0.3 V or an internal diode will turn on, exceeding the max ratings of the device. In this type of application, the full range of multiplying capability of the DAC is lost.

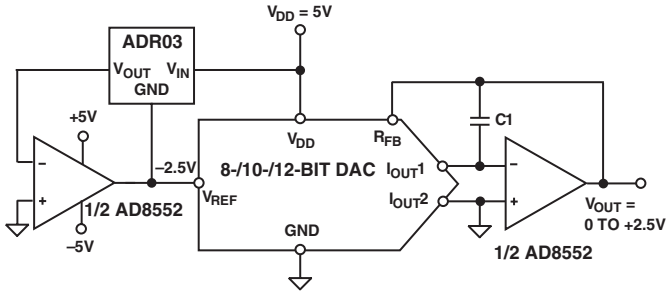


NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY
2. C1 PHASE COMPENSATION (1pF– 2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 7. Single-Supply Voltage Switching Mode Operation

POSITIVE OUTPUT VOLTAGE

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages. In order to achieve a positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor tolerance errors. To generate a negative reference, the reference can be level shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and –2.5 V respectively, as shown in Figure 8.



NOTES
1. ADDITIONAL PINS OMITTED FOR CLARITY
2. C1 PHASE COMPENSATION (1pF–2pF) MAY BE REQUIRED IF A1 IS A HIGH SPEED AMPLIFIER.

Figure 8. Positive Voltage Output with Minimum of Components

ADDING GAIN

In applications where the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier or it can also be achieved in a single stage. It is important to consider the effect of temperature coefficients of the thin film resistors of the DAC. Simply placing a resistor in series with the RFB resistor will cause mismatches in the temperature coefficients resulting in larger gain temperature coefficient errors. Instead, the circuit of Figure 9 is a recommended method of increasing the gain of the circuit. R1, R2, and R3 should all have similar temperature coefficients, but they need not match the temperature coefficients of the DAC. This approach is recommended in circuits where gains of great than 1 are required.

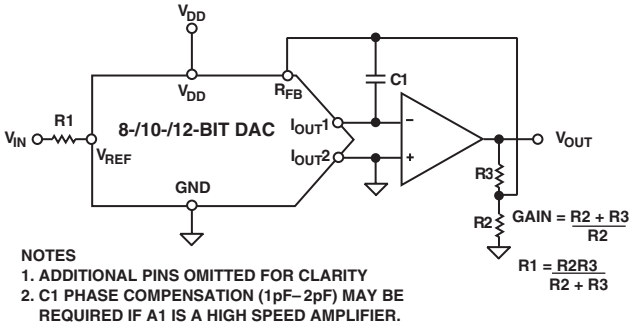


Figure 9. Increasing Gain of Current Output DAC

USING DACS AS A DIVIDER OR A PROGRAMMABLE GAIN ELEMENT

Current steering DACs are very flexible and lend themselves to many different applications. If this type of DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor as shown in Figure 10, then the output voltage is inversely proportional to the digital input fraction D. For D = $1 - 2^n$ the output voltage is

$$V_{OUT} = -V_{IN}/D = -V_{IN}/\left(1-2^{-n}\right)$$

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an 8-bit DAC driven with the binary code 10H (00010000), i.e., 16 decimal, in the circuit of Figure 10 should cause the output voltage to be 16× V_{IN}. However, if the DAC has a linearity specification of ±0.5 LSB then D can in fact have the weight anywhere in the range 15.5/256 to 16.5/256 so that the possible output voltage will be in the range 15.5 V_{IN} to 16.5 V_{IN}—an error of +3% even though the DAC itself has a maximum error of 0.2%.

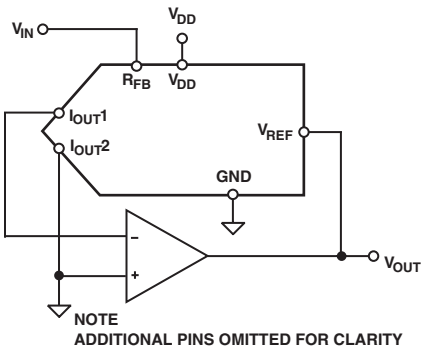


Figure 10. Current Steering DAC Used as a Divider or Programmable Gain Element

Table III. Suitable ADI Precision References Recommended for Use with AD5424/AD5433/AD5445 DACs

Part No.	Output Voltage	Initial Tolerance	Temperature Drift	0.1 Hz to 10 Hz Noise	Package
ADR01	10 V	0.1%	3 ppm/°C	20 μV p-p	SC70, TSOT, SOIC
ADR02	5 V	0.1%	3 ppm/°C	10 μV p-p	SC70, TSOT, SOIC
ADR03	2.5 V	0.2%	3 ppm/°C	10 μV p-p	SC70, TSOT, SOIC
ADR425	5 V	0.04%	3 ppm/°C	3.4 μV p-p	MSOP, SOIC

Table IV. Some Precision ADI Op Amps Suitable for Use with AD5424/AD5433/AD5445 DACs

Part No.	Max Supply Voltage (V)	V_{OS} (max) (μV)	I_B (max) (nA)	GBP (MHz)	Slew Rate (V/μs)
OP97	±20	25	0.1	0.9	0.2
OP1177	±18	60	2	1.3	0.7
AD8551	±6	5	0.05	1.5	0.4

Table V. Some High Speed ADI Op Amps Suitable for Use with AD5424/AD5433/AD5445 DACs

Part No.	Max Supply Voltage (V)	BW @ A_{CL} (MHz)	Slew Rate (V/μs)	V_{OS} (max) (μV)	I_B (max) (nA)
AD8065	±12	145	180	1500	0.01
AD8021	±12	200	100	1000	1000
AD8038	±5	350	425	3000	0.75
AD9631	±5	320	1300	10000	7000

DAC leakage current is also a potential error source in divider circuits. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction D of the current into the V_{REF} terminal is routed to the $I_{OUT}1$ terminal, the output voltage has to change as follows:

Output Error Voltage Due to DAC Leakage = (Leakage × R)/D

where *R* is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10 nA, R = 10 kΩ and a gain (i.e., 1/D) of 16 the error voltage is 1.6 mV.

REFERENCE SELECTION

When selecting a reference for use with the AD5424 series of current output DACs, pay attention to the references output voltage temperature coefficient specification. This parameter not only affects the full-scale error, but can also affect the linearity (INL and DNL) performance. The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1 LSB over the temperature range 0°C to 50°C dictates that the maximum *system drift* with temperature should be less than 78 ppm/°C. A 12-bit system with the same temperature range to overall specification within 2 LSBs requires a maximum drift of 10 ppm/°C. By choosing a precision reference with low output temperature coefficient this error source can be minimized. Table III suggests some references available from Analog Devices that are suitable for use with this range of current output DACs.

AMPLIFIER SELECTION

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable gain (due to the code dependent output resistance of the DAC) of the circuit. A change in this noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed on the desired change in output between the two codes and gives rise to a differential linearity error, which if large enough, could cause the DAC to be nonmonotonic. In general, the input offset voltage should be <1/4 LSB to ensure monotonic behavior when stepping through codes.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor RFB. Most op amps have input bias currents low enough to prevent any significant errors in 12-bit applications.

Common-mode rejection of the op amp is important in voltage switching circuits since it produces a code dependent error at the voltage output of the circuit. Most op amps have adequate common mode rejection for use at 8-, 10-, and 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew rate and settling time of a voltage switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time in this configuration, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low inputs capacitance buffer amplifiers and careful board design.

Most single-supply circuits include ground as part of the analog signal range, which in turns requires an amplifier that can handle rail-to-rail signals; there is a large range of single-supply amplifiers available from Analog Devices.

PCB LAYOUT AND POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5424/AD5433/AD5445 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the DAC is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

These DACs should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies, to handle transient currents due to internal logic switching. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple.

Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

It is good practice to employ compact, minimum lead length PCB layout design. Leads to the input should be as short as possible to minimize IR drops and stray inductance.

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error. To maximize on high frequency performance, the I-to-V amplifier should be located as close to the device as possible.

EVALUATION BOARD FOR THE AD5424/AD5433/AD5445

The board consists of a 12-bit AD5445 and a current to voltage amplifier AD8065. Included on the evaluation board is a 10 V reference ADR01. An external reference may also be applied via an SMB input.

The evaluation kit consists of a CD-ROM with self-installing PC software to control the DAC. The software simply allows the user to write a code to the device.

OPERATING THE EVALUATION BOARD

Power Supplies

The board requires ±12 V, and +5 V supplies. The +12 V V_{DD} and V_{SS} are used to power the output amplifier, while the +5 V is used to power the DAC (V_{DD1}) and transceivers (V_{CC}).

Both supplies are decoupled to their respective ground plane with 10 μF tantalum and 0.1 μF ceramic capacitors.

Link1 (LK1) is provided to allow selection between the on-board reference (ADR01) or an external reference applied through J2.

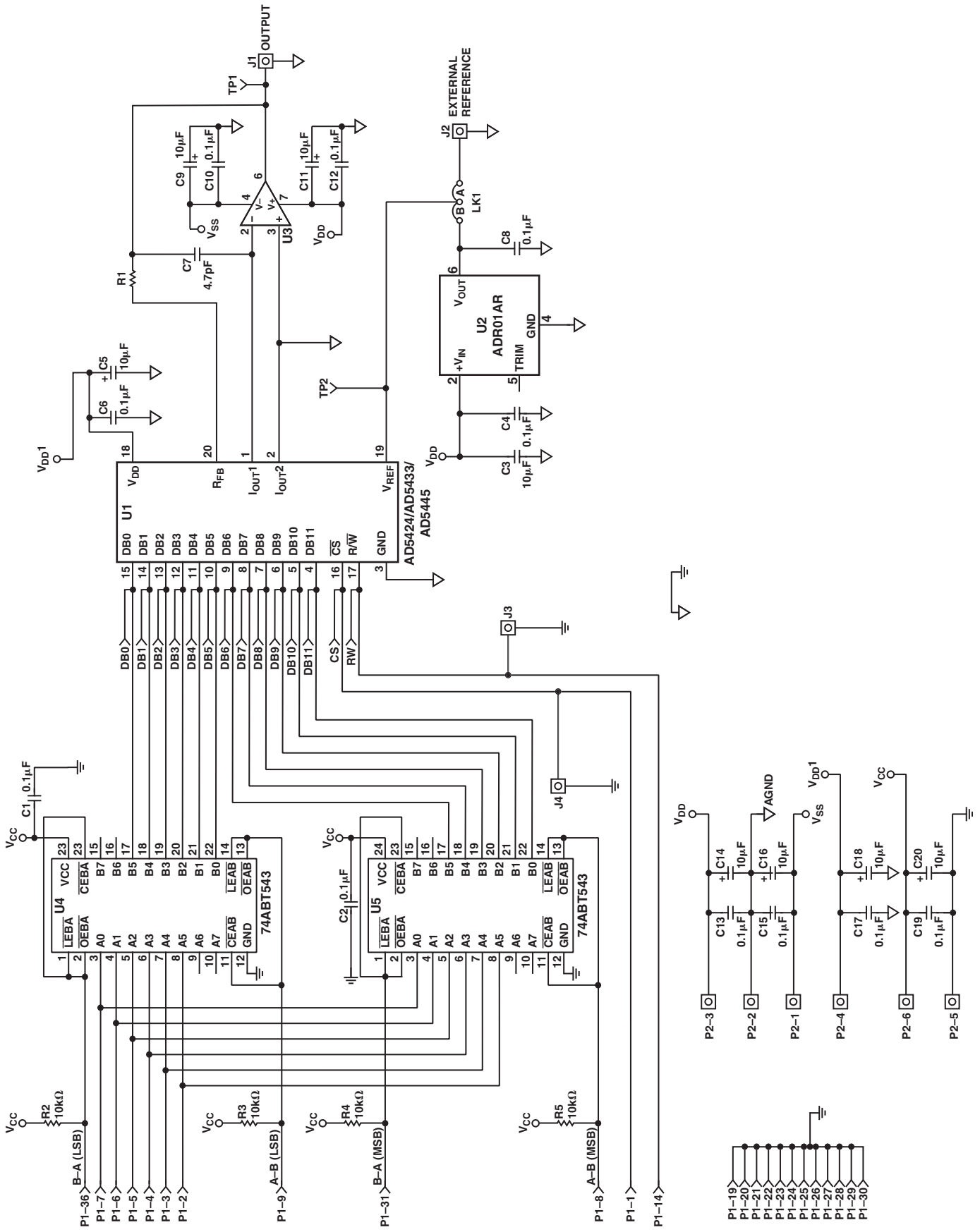


Figure 11. Evaluation Board Schematic

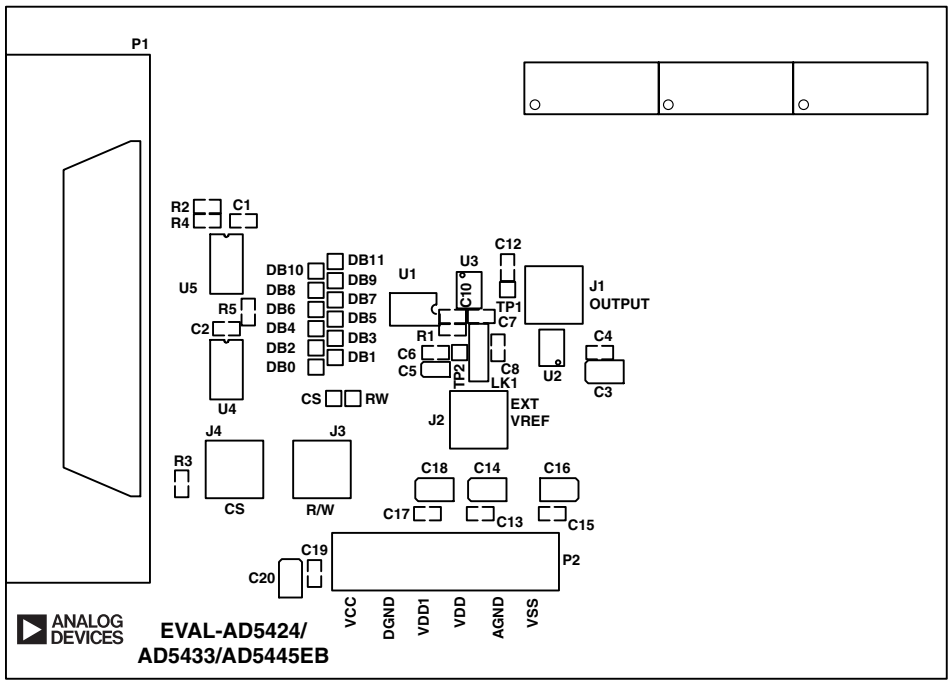


Figure 12. Silkscreen—Component Side View

Table VI. Bill of Materials for AD5424/AD5433/AD5445 Evaluation Board

Name	Part Description	Value	Tolerance	PCB Decal	Stock Code
C1, C2, C4, C6, C8	X7R Ceramic Capacitor	0.1 μF	10%	0603	FEC 499-675
C10, C12, C13, C15	X7R Ceramic Capacitor	0.1 μF	10%	0603	FEC 499-675
C3, C5, C9, C11, C14	Tantalum Capacitor – Taj Series	10 μF 20 V	10%	CAP\TAJ_B	FEC 197-427
C17, C19	X7R Ceramic Capacitor	0.1 μF	10%	0603	FEC 499-675
C16, C18, C20	Tantalum Capacitor – Taj Series	10 μF 10 V	10%	CAP\TAJ_A	FEC 197-130
C7	X7R Ceramic Capacitor	4.7 pF	10%	0603	
CS	TESTPOINT			TESTPOINT	FEC 240-345 (Pack)
DB0–DB11	Red Testpoint			TESTPOINT	FEC 240-345 (Pack)
J1–J4	SMB Socket			SMB	FEC 310-682
LK1	3-Pin Header (3 × 1)			LINK-3P-	FEC 511-717 and 150-411
P1	36-Pin Centronics Connector			36WAY	FEC 147-753
P2	6-Pin Terminal Block			CON\POWER6	FEC 151-792
R1	0.063 W Resistor			0603	Not Inserted
R2, R3, R4, R5	0.063 W Resistor	10 kΩ	1%	0603	FEC 911-355
RW, TP1, TP2	Red Testpoint			TESTPOINT	FEC 240-345 (Pack)
U1	AD5445			TSSOP20	AD5445BRU
U2*	ADR425/ADR01/ADR02/ADR03			SO8NB	ADR01AR
U3*	AD8065			SO8NB	AD8065AR
U4	74ABT543			TSSOP24	Fairchild 74ABT543CMTC
U5	74ABT543			TSSOP24	Fairchild 74ABT543CMTC
Each Corner	Rubber Stick-on Feet				FEC 148-922

*See section on Amplifier and Reference Selection
FEC - Farnell Electronic Components, Units 4 and 5 Gofton Court, Jamestown Road, Finglas, Dublin 11, Ireland. Tel. Int +353 (0)1 8309277
www.farnell.com

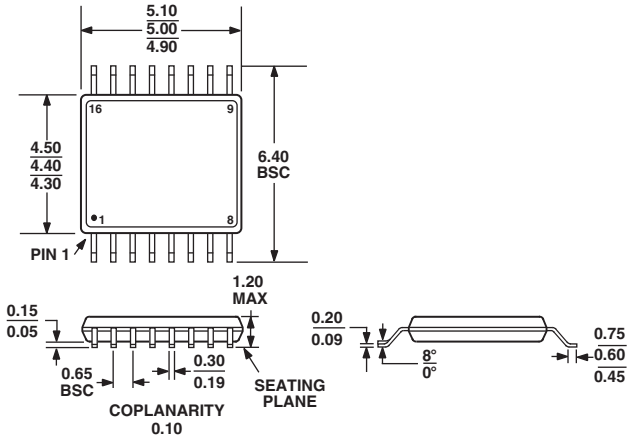
Overview of AD54xx Devices

Part No.	Resolution	No. DACs	INL	t_S max	Interface	Package	Features
AD5403*	8	2	±0.25	60 ns	Parallel	CP-40	10 MHz Bandwidth, 10 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5410*	8	1	±0.25	100 ns	Serial	RU-16	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5413*	8	2	±0.25	100 ns	Serial	RU-24	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5424	8	1	±0.25	60 ns	Parallel	RU-16, CP-20	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5425	8	1	±0.25	100 ns	Serial	RM-10	Byte Load, 10 MHz Bandwidth, 50 MHz Serial
AD5426	8	1	±0.25	100 ns	Serial	RM-10	10 MHz Bandwidth, 50 MHz Serial
AD5428	8	2	±0.25	60 ns	Parallel	RU-20	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5429	8	2	±0.25	100 ns	Serial	RU-10	10 MHz Bandwidth, 50 MHz Serial
AD5450	8	1	±0.25	100 ns	Serial	RJ-8	10 MHz Bandwidth, 50 MHz Serial
AD5404*	10	2	±0.5	70 ns	Parallel	CP-40	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5411*	10	1	±0.5	110 ns	Serial	RU-16	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5414*	10	2	±0.5	110 ns	Serial	RU-24	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5432	10	1	±0.5	110 ns	Serial	RM-10	10 MHz Bandwidth, 50 MHz Serial
AD5433	10	1	±0.5	70 ns	Parallel	RU-20, CP-20	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5439	10	2	±0.5	110 ns	Serial	RU-16	10 MHz Bandwidth, 50 MHz Serial
AD5440	10	2	±0.5	70 ns	Parallel	RU-24	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5451	10	1	±0.25	110 ns	Serial	RJ-8	10 MHz Bandwidth, 50 MHz Serial
AD5405	12	2	±1	120 ns	Parallel	CP-40	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width, 4-Quadrant Multiplying Resistors
AD5412*	12	1	±1	160 ns	Serial	RU-16	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5415	12	2	±1	160 ns	Serial	RU-24	10 MHz Bandwidth, 50 MHz Serial, 4-Quadrant Multiplying Resistors
AD5443	12	1	±1	160 ns	Serial	RM-10	10 MHz Bandwidth, 50 MHz Serial
AD5445	12	1	±1	120 ns	Parallel	RU-20, CP-20	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5447	12	2	±1	120 ns	Parallel	RU-24	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5449	12	2	±1	160 ns	Serial	RU-16	10 MHz Bandwidth, 17 ns $\overline{CS}$ Pulse Width
AD5452	12	1	±0.5	160 ns	Serial	RJ-8, RM-8	10 MHz Bandwidth, 50 MHz Serial
AD5453	14	1	±2	180 ns	Serial	RJ-8, RM-8	10 MHz Bandwidth, 50 MHz Serial

*Future parts, contact factory for availability

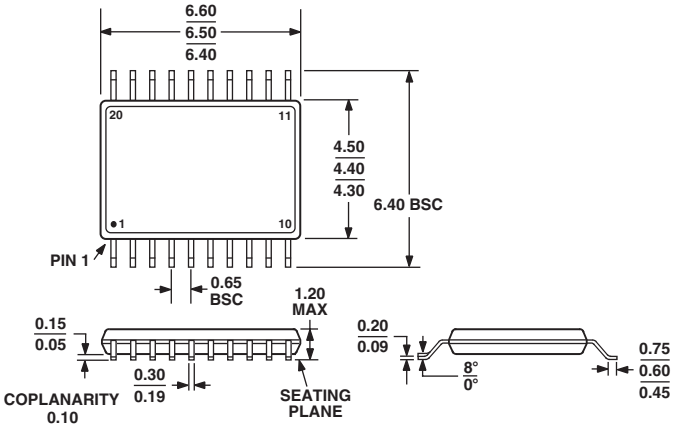
OUTLINE DIMENSIONS

16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



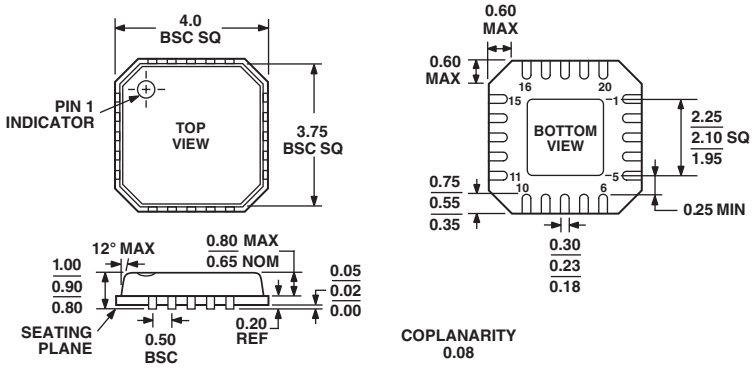
COMPLIANT TO JEDEC STANDARDS MO-153AB

20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AC

20-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

C03160–0–10/03(0)

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