

# DMC56205

## Silicon NPN epitaxial planar type

For digital circuits

### ■ Features

- High forward current transfer ratio  $h_{FE}$  with excellent linearity
- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Halogen-free / RoHS compliant  
(EU RoHS / UL-94 V-0 / MSL: Level 1 compliant)

### ■ Marking Symbol: K3

### ■ Basic Part Number

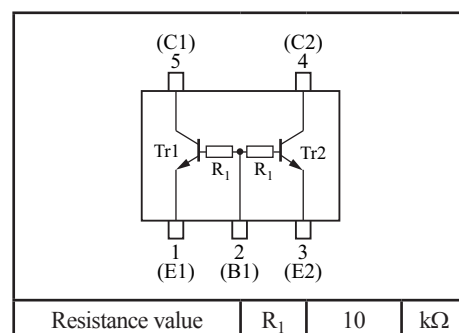
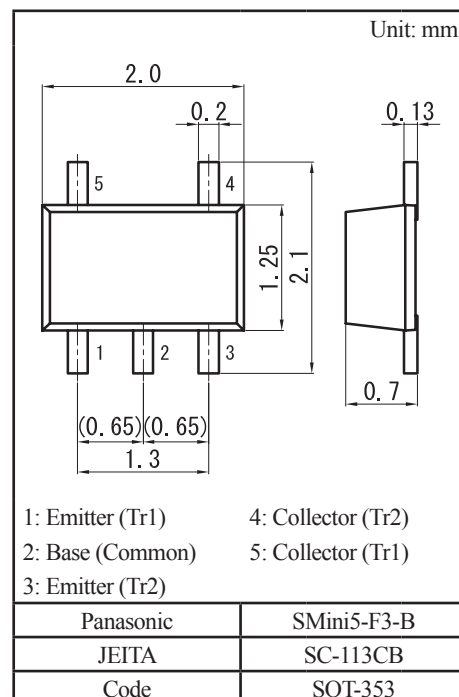
Dual DRC2114T (Common base)

### ■ Packaging

DMC562050R Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter		Symbol	Rating	Unit
Tr1 Tr2	Collector-base voltage (Emitter open)	$V_{CBO}$	50	V
	Collector-emitter voltage (Base open)	$V_{CEO}$	50	V
	Collector current	$I_C$	100	mA
Overall	Total power dissipation	$P_T$	150	mW
	Junction temperature	$T_j$	150	$^\circ\text{C}$
	Operating ambient temperature	$T_{opr}$	-40 to +85	$^\circ\text{C}$
	Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

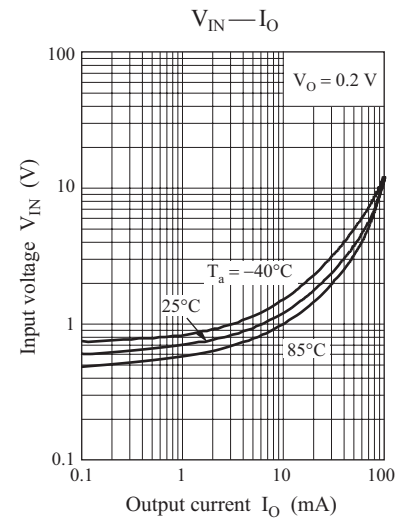
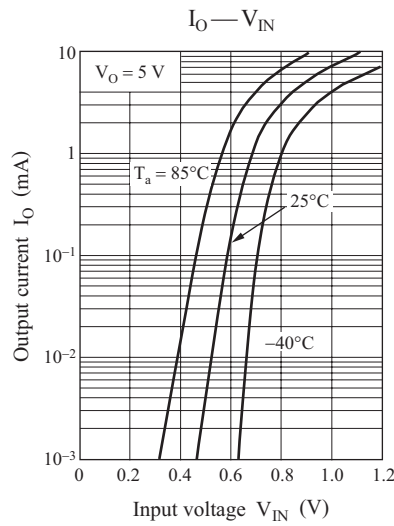
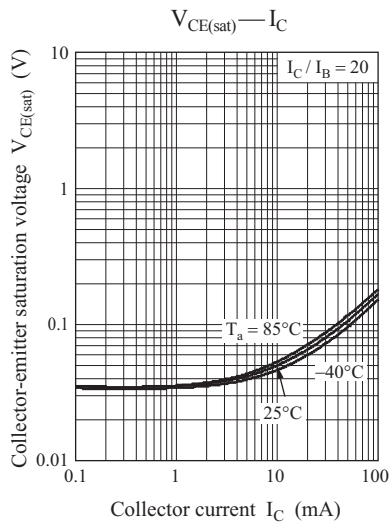
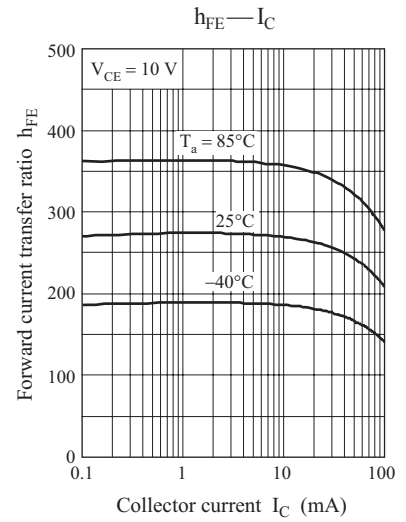
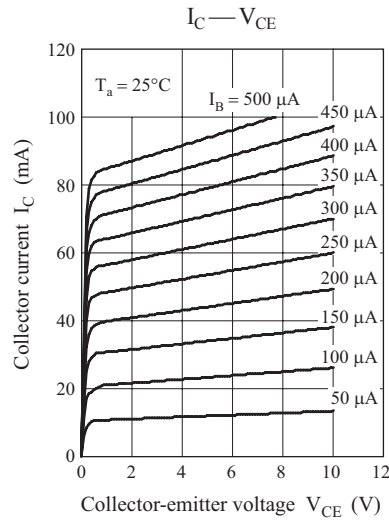
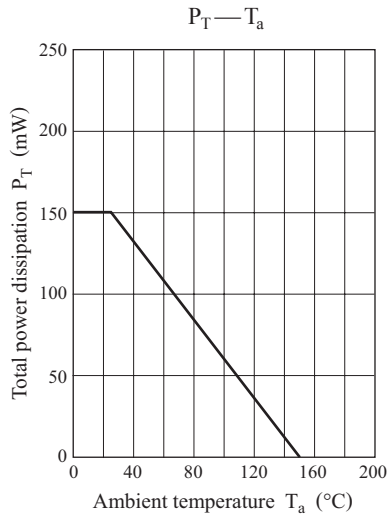


### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = 10 \mu\text{A}, I_E = 0$	50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = 2 \text{ mA}, I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 50 \text{ V}, I_E = 0$			0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = 50 \text{ V}, I_B = 0$			0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = 6 \text{ V}, I_C = 0$			0.01	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = 10 \text{ V}, I_C = 5 \text{ mA}$	160		460	—
$h_{FE}$ ratio *1	$h_{FE}$ (Small/Large)	$V_{CE} = 10 \text{ V}, I_C = 5 \text{ mA}$	0.50	0.99		—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 10 \text{ mA}, I_B = 0.5 \text{ mA}$			0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = 0.2 \text{ V}, I_C = 5 \text{ mA}$	1.2			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = 5 \text{ V}, I_C = 100 \mu\text{A}$			0.4	V
Input resistance	$R_1$		-30%	10	+30%	k $\Omega$

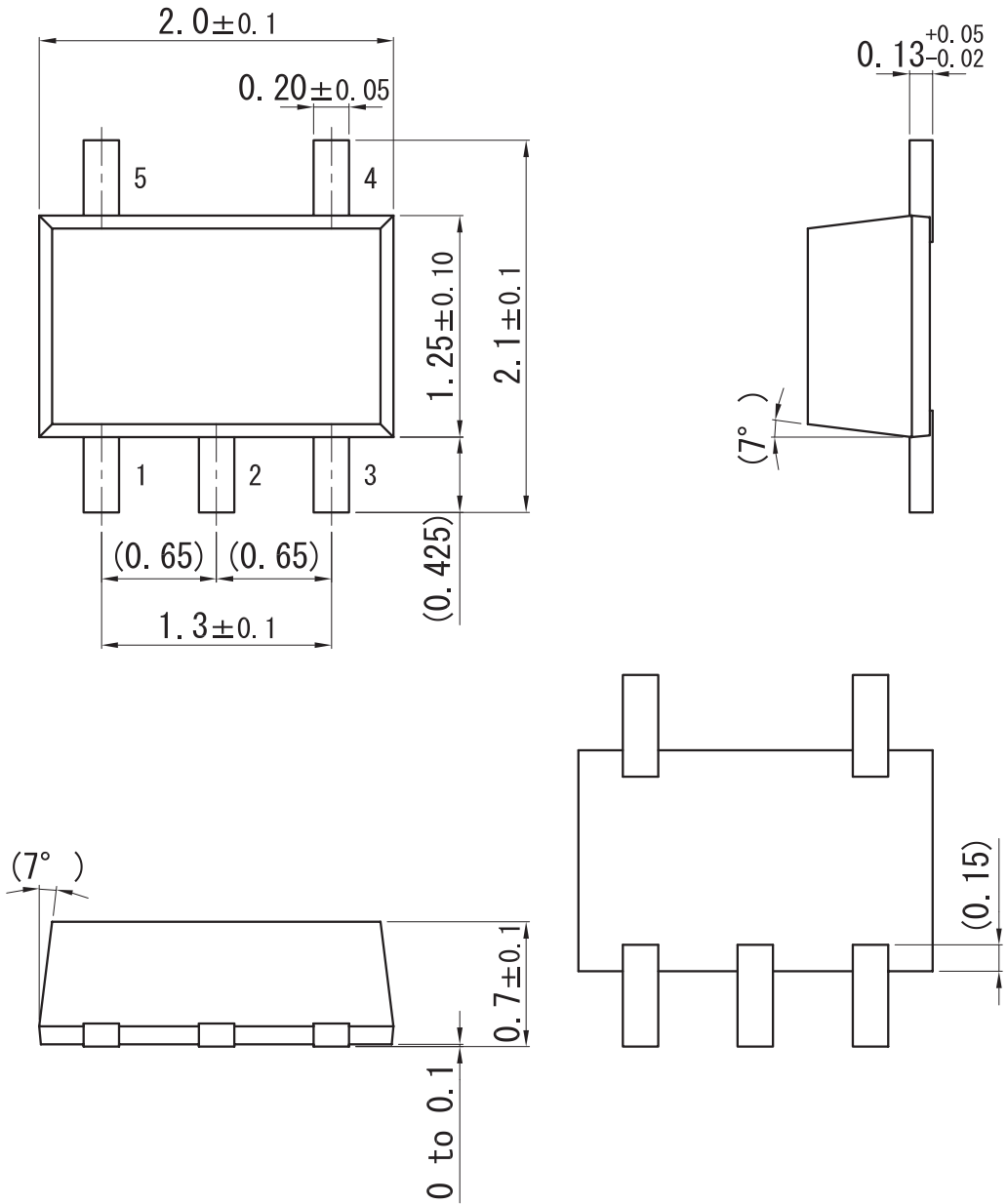
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*1: Ratio between 2 elements

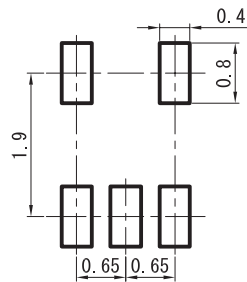


SMini5-F3-B

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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