

# DRA4124T

## Silicon PNP epitaxial planar type

For digital circuits

Complementary to DRC4124T

DRA2124T in NS through hole type package

### ■ Features

- High forward current transfer ratio  $h_{FE}$  with excellent linearity
- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

### ■ Packaging

DRA4124T0A Radial type: 5000 pcs / carton

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	-50	V
Collector-emitter voltage (Base open)	$V_{CEO}$	-50	V
Collector current	$I_C$	-100	mA
Total power dissipation	$P_T$	300	mW
Junction temperature	$T_J$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### ■ Package

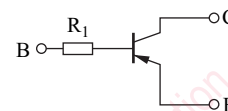
- Code  
NS-B2-B-B  
Package dimension clicks here.→

### ■ Pin Name

- 1: Emitter
- 2: Collector
- 3: Base

### ■ Marking Symbol: LH

### ■ Internal Connection



Resistance value	$R_1$	22	k $\Omega$
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### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = -10 \mu\text{A}, I_E = 0$	-50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -50 \text{ V}, I_E = 0$			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = -50 \text{ V}, I_B = 0$			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -6 \text{ V}, I_C = 0$			-0.01	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = -10 \text{ V}, I_C = -5 \text{ mA}$	160		460	—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10 \text{ mA}, I_B = -0.5 \text{ mA}$			-0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = -0.2 \text{ V}, I_C = -5 \text{ mA}$	-1.8			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = -5 \text{ V}, I_C = -100 \mu\text{A}$			-0.4	V
Input resistance	$R_1$		-30%	22	+30%	k $\Omega$

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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