

# DRAF143Z

## Silicon PNP epitaxial planar type

For digital circuits

Complementary to DRCF143Z

DRA3143Z in ML3 type package

### ■ Features

- High forward current transfer ratio  $h_{FE}$
- Low collector-emitter saturation voltage  $V_{CE(sat)}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

### ■ Packaging

DRAF143Z0L Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	-50	V
Collector-emitter voltage (Base open)	$V_{CEO}$	-50	V
Collector current	$I_C$	-100	mA
Total power dissipation *	$P_T$	100	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Note) \*: Copper plate at the collector is  $5.0\text{ mm}^2$  on substrate at  $10\text{ mm} \times 12\text{ mm} \times 0.8\text{ mm}$ .

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = -10\ \mu\text{A}, I_E = 0$	-50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -2\ \text{mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -50\ \text{V}, I_E = 0$			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = -50\ \text{V}, I_B = 0$			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -6\ \text{V}, I_C = 0$			-0.2	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = -10\ \text{V}, I_C = -5\ \text{mA}$	80		400	—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10\ \text{mA}, I_B = -0.5\ \text{mA}$			-0.25	V
Input voltage (ON)	$V_{I(on)}$	$V_{CE} = -0.2\ \text{V}, I_C = -5\ \text{mA}$	-1.3			V
Input voltage (OFF)	$V_{I(off)}$	$V_{CE} = -5\ \text{V}, I_C = -100\ \mu\text{A}$			-0.4	V
Input resistance	$R_1$		-30%	4.7	+30%	$\text{k}\Omega$
Resistance ratio	$R_1 / R_2$		0.08	0.10	0.12	—

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

### ■ Package

- Code

ML3-N4-B

Package dimension clicks here.→

- Pin Name

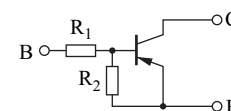
1: Base

2: Emitter

3: Collector

### ■ Marking Symbol: L8

### ■ Internal Connection



Resistance value	$R_1$	4.7	$\text{k}\Omega$
	$R_2$	47	$\text{k}\Omega$

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