

January 1997

## Monolithic PCM Repeater

### Features

- Automatic Line Buildout
- Supply Voltage ..... 5.1V
- Buffered Output

### Applications

- Bipolar Carrier System ..... T1 1.544Mbits/s
- Ternary Carrier System ..... T148 2.37Mbits/s

### Ordering Information

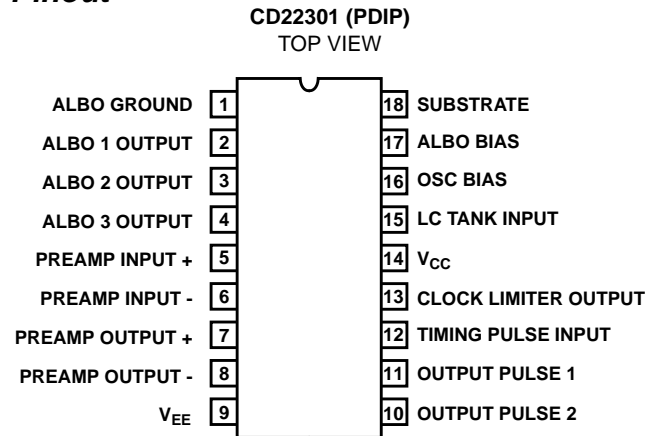
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD22301E	-40 to 85	18 Ld PDIP	E18.3

### Description

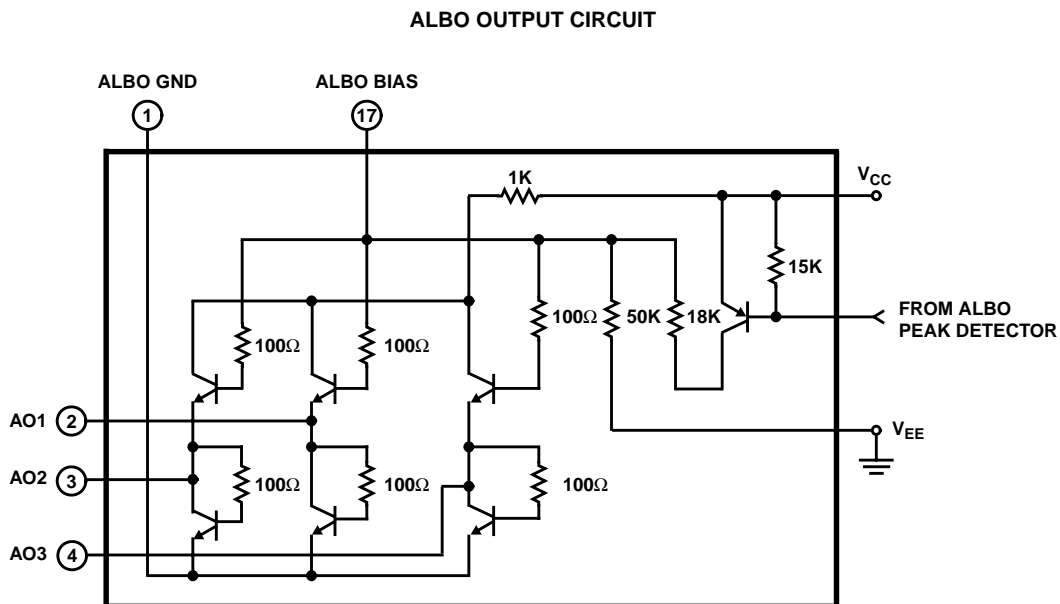
The CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37Mbits/s. The circuit operates from a 5.1V  $\pm 5\%$  externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing and buffered output formation.

### Pinout



### Functional Diagram



# CD22301

## Absolute Maximum Ratings

Supply Voltage . . . . . 10V  
 Input Current (Into Pin 9 or 10) . . . . . 25mA  
 Peak Current (Into Pin 9 or 10) . . . . . 100mA  
 Input Surge Voltage (Between Pins 5 and 6, t = 10ms) . . . . . 50V  
 Output Surge Voltage (Between Pins 10 and 11, t = 1ms) . . . . . 50V  
 Power Dissipation  
     For  $T_A = -40^{\circ}\text{C}$  to  $60^{\circ}\text{C}$  . . . . . 500mW  
     For  $T_A = 60^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  . . . . . Derate Linearly 12mW/ $^{\circ}\text{C}$  to 200mW  
 Device Dissipation per Output Transistor  
     For  $T_A = \text{Full Package Temperature Range (All Types)}$  . . . . . 100mW

## Thermal Information

Maximum Junction Temperature . . . . .  $175^{\circ}\text{C}$   
 Maximum Junction Temperature (Plastic Package) . . . . .  $150^{\circ}\text{C}$   
 Maximum Storage Temperature Range . . . . .  $-65^{\circ}\text{C} \leq T_A \leq 150^{\circ}\text{C}$   
 Maximum Lead Temperature (Soldering 10s) . . . . .  $300^{\circ}\text{C}$

## Operating Conditions

Temperature Range . . . . .  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications $T_A = 25^{\circ}\text{C}$ , $V_{CC} = 5.1\text{V} \pm 5\%$ (See Figure 4)

PARAMETER	MIN	TYP	MAX	UNITS
<b>STATIC DC VOLTAGES</b>				
ALBO Pins (Pins 2, 3, 4 and 17)	-	0	0.1	V
Pre Amp Inputs and Outputs (Pins 5, 6, 7 and 8)	2.4	2.9	3.4	V
Output Pulse 1, 2 (Pins 10 and 11)	-	5.1	-	V
Oscillator/Clock (Pins 12, 13, 15 and 16)	3.1	3.6	4.1	V
<b>STATIC DC CURRENTS</b>				
$I_{CC}$	-	22	30	mA
Output Pulse 1, 2 (Pins 10 and 11)	-	0	100	$\mu\text{A}$

## Electrical Specifications $T_A = 25^{\circ}\text{C}$ , $V_{CC} = 5.1\text{V} \pm 5\%$

PARAMETER	SYMBOL	FIGURE	NOTE	MIN	TYP	MAX	UNITS
<b>DYNAMIC SPECIFICATIONS</b>							
Preamplifier Input Impedance	$Z_{IN}$	7		20	-	-	$\text{k}\Omega$
Preamplifier Output Impedance	$Z_{OUT}$	7		-	-	2	$\text{k}\Omega$
Preamplifier Gain at 2.37MHz	$A_O$	7		47	50	-	dB
Preamplifier Output Offset Voltage	$\Delta V_{OUT}$	7	1	-50	0	50	mV
Clock Limiter Input Impedance	$Z_{IN(CL)}$	5	2	10	-	-	$\text{k}\Omega$
ALBO Off Impedance	$Z_{ALBO(off)}$	5	3	20	-	-	$\text{k}\Omega$
ALBO On Impedance	$Z_{ALBO(on)}$	5	4	-	-	10	$\Omega$
DATA Threshold Voltage	$V_{TH(D)}$	6	5, 8	0.62	0.7	0.78	V
CLOCK Threshold Voltage	$V_{TH(CL)}$	6	6, 8	0.92	1.1	1.28	V
ALBO Threshold	$V_{TH(AL)}$	6	7, 8	1.4	1.5	1.6	V
$V_{TH(D)}$ as % of $V_{TH(AL)}$				44	47	49	%
$V_{TH(CL)}$ as % of $V_{TH(AL)}$				66	73	80	%
Buffer Gate Voltage (low)	$V_{OL}$	4	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	$\Delta V_{OL}$	4	9	-0.15	0	0.15	V
Output Pulse Rise Time	$t_R$	4, 8	9, 10	-	-	40	ns

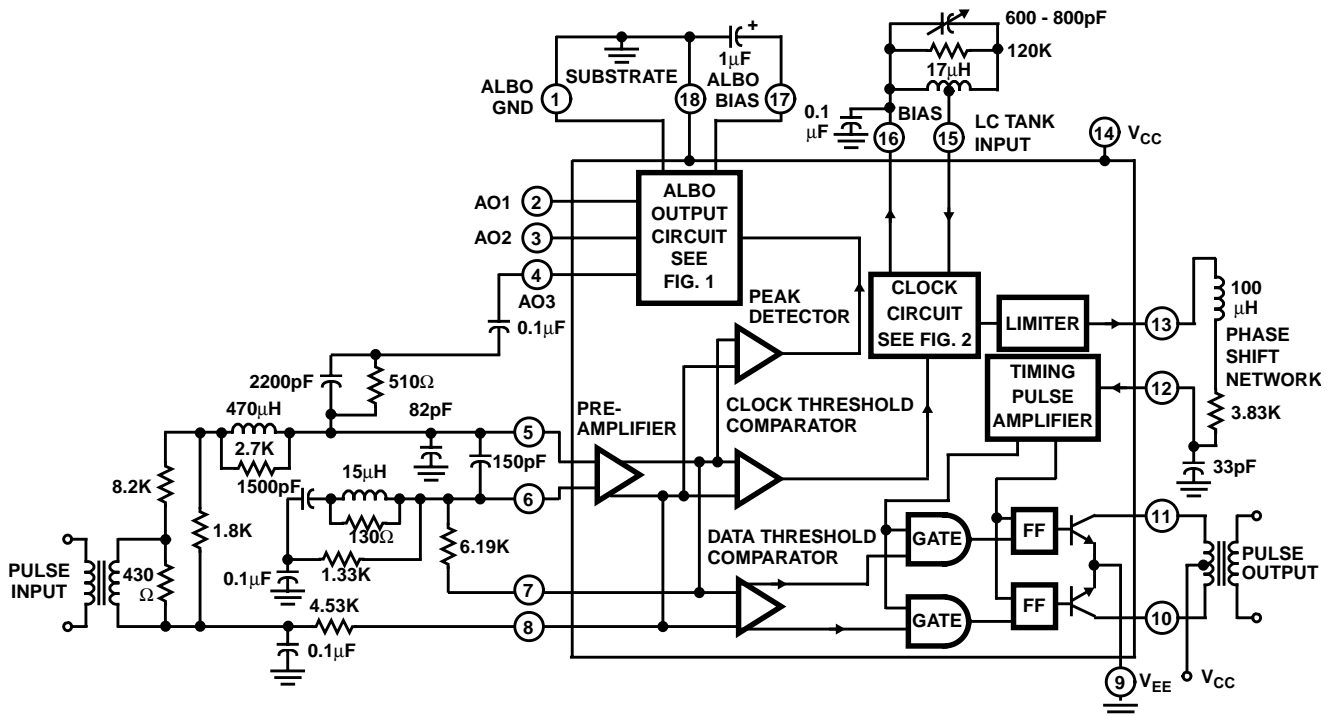
# CD22301

## Electrical Specifications $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.1\text{V} \pm 5\%$ (Continued)

PARAMETER	SYMBOL	FIGURE	NOTE	MIN	TYP	MAX	UNITS
Output Pulse Fall Time	$t_F$	4, 8	9, 10	-	-	40	ns
Output Pulse Width	$t_W$	4, 8	9, 10	290	324	340	ns
Pulse Width Differential	$\Delta t_W$	4, 8	9, 10	-10	0	10	ns
Clock Drive Current	$I_{CL}$			-	2	-	mA

**NOTES:**

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15. See Figure 5.
3. Adjust potentiometer for 0V (See Figure 5). Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2V (See Figure 5). Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for  $\Delta V = 0\text{V}$  (See Figure 6). Then slowly increase  $\Delta V$  in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing  $\Delta V$  until the DC level at the clock terminal drops to 4V (See Figure 6).
7. Continue increasing  $\Delta V$  until the ALBO terminal rises to 1V (See Figure 6).
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set  $e_{IN} = 2.75\text{mV}_{RMS}$  at  $f \approx 1.185\text{MHz}$ . Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by 3dB.



**FIGURE 1. TYPICAL 1.544MHz T1 REPEATER SYSTEM**

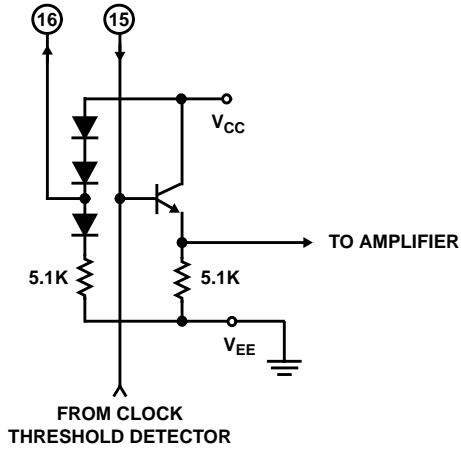


FIGURE 2. CLOCK INTERFACE CIRCUIT

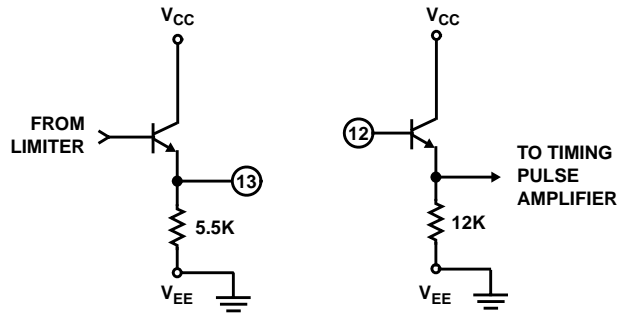


FIGURE 3. PHASE-SHIFT INTERFACE CIRCUITS

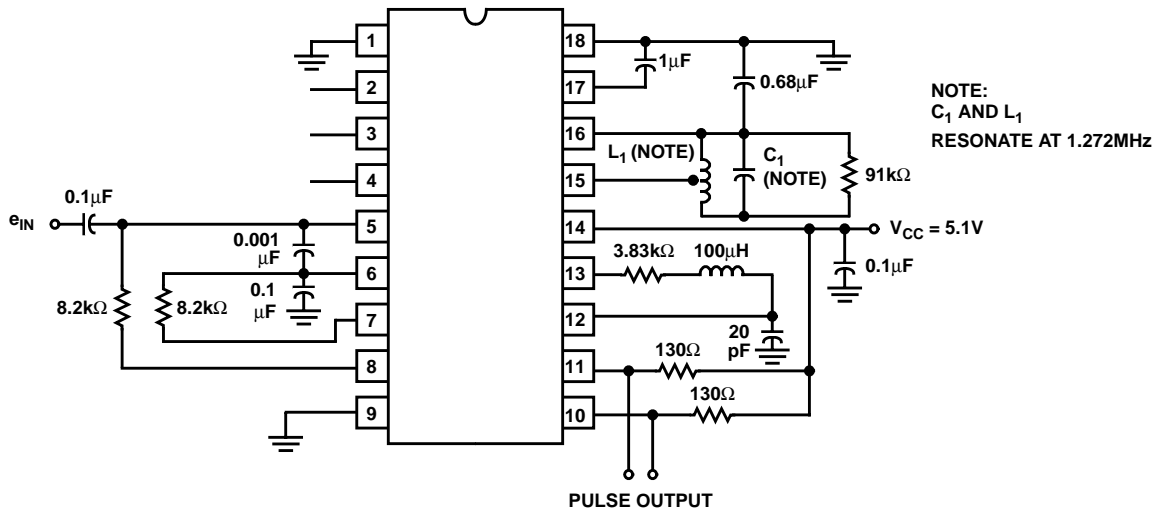


FIGURE 4. DC AND OUTPUT PULSE TEST CIRCUIT

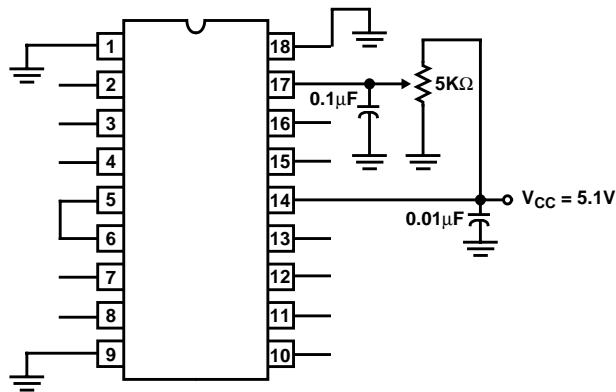


FIGURE 5. TEST CIRCUIT FOR IMPEDANCE MEASUREMENT

# CD22301

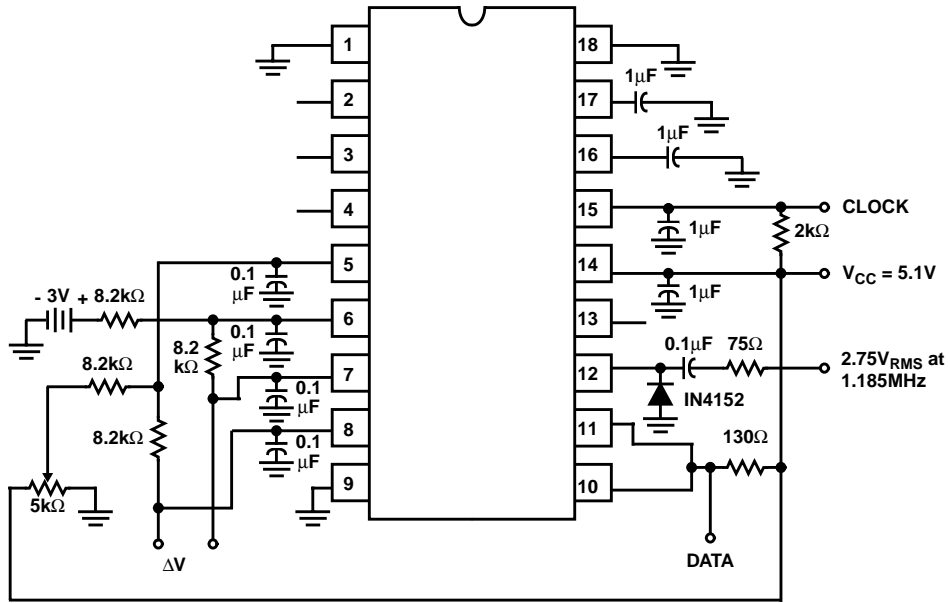


FIGURE 6. TEST CIRCUIT FOR THRESHOLD VOLTAGE MEASUREMENT

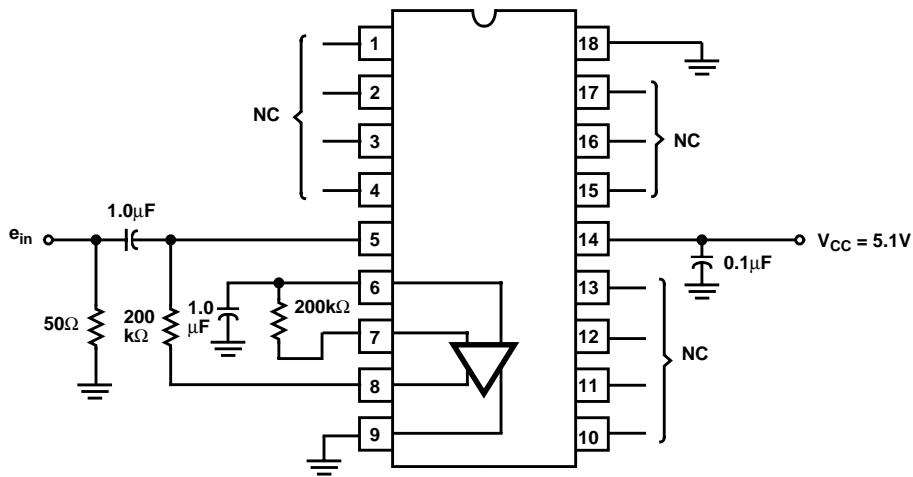


FIGURE 7. PREAMPLIFIER GAIN AND IMPEDANCE MEASUREMENT CIRCUIT

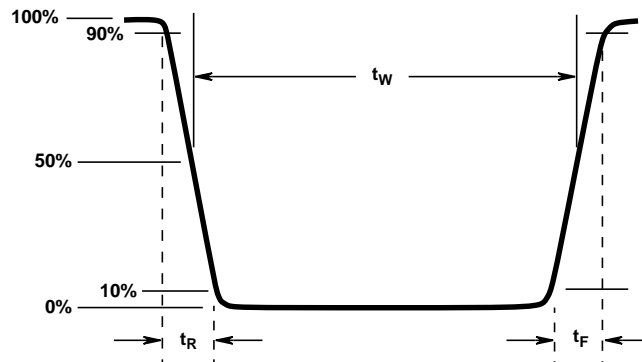


FIGURE 8. OUTPUT PULSE WAVEFORM

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