

**DESCRIPTION**

The HY6264A is a high speed, low power 8,192 words by 8-bit CMOS static RAM fabricated using a twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY6264A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

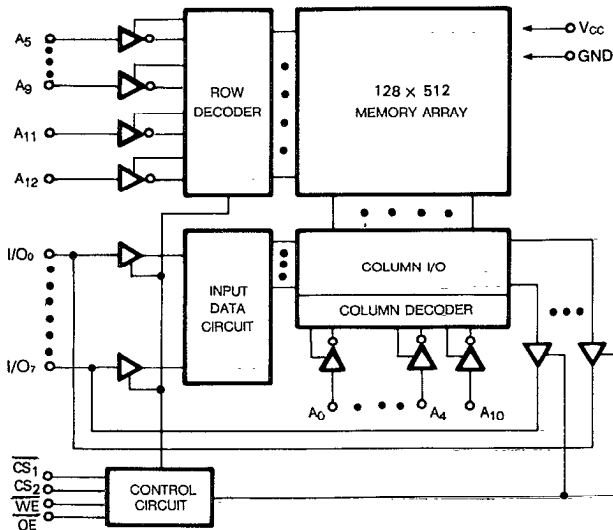
Using CMOS technology, supply voltage from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6264A family.

**FEATURES**

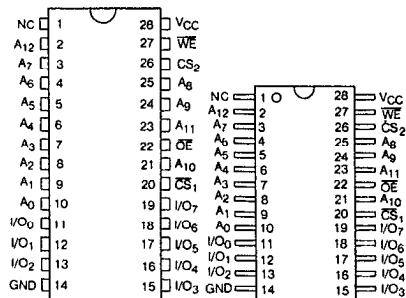
- High speed – 70/85/100/120/150ns (max.)
- Low power consumption
  - 200 mW typical operating
  - 10 μW typical standby (L/LL-version)
- Battery back up (L/LL-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28 pin 600 mil P-DIP and 330 mil SOP

	HY6264A-70	HY6264A-85	HY6264A-100	HY6264A-120	HY6264A-150
Maximum Access Time(ns)	70	85	100	120	150
Maximum Operating Current(mA)	50	50	50	50	50
Maximum Standby Current(mA)		2	2	2	2
	L	0.1	0.1	0.1	0.1
	LL	0.05	0.05	0.05	0.05

**BLOCK DIAGRAM**



**PIN CONNECTIONS**



**DIP**                      **SOP**

**PIN NAMES**

A <sub>0</sub> -A <sub>12</sub>	ADDRESS INPUT
I/O <sub>0</sub> -I/O <sub>7</sub>	DATA INPUT/OUTPUT
CS <sub>1</sub>	CHIP SELECT ONE
CS <sub>2</sub>	CHIP SELECT TWO
WE	WRITE ENABLE
OE	OUTPUT ENABLE
V <sub>CC</sub>	POWER
GND	GROUND

## HY6264A 8,192×8-Bit CMOS SRAM

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

SYMBOL	PARAMETER	RATING	UNIT
V <sub>DD</sub> , V <sub>IN</sub> , V <sub>I/O</sub>	Power Supply, Input, Input/Output Voltage	-0.5 <sup>(2)</sup> to 7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-10 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
P <sub>D</sub>	Power Dissipation	1.0	W
I <sub>OUT</sub>	Data Output Current	50	mA

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. -3.5V for 20ns pulse.

### RECOMMENDED DC OPERATING CONDITIONS

(T<sub>A</sub>=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	3.5	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	0	0.8	V

**NOTES:**

1. -3.5V for 20ns pulse.

### TRUTH TABLE

MODE	$\overline{CS}_1$	CS <sub>2</sub>	$\overline{WE}$	$\overline{OE}$	I/O OPERATION
Standby	H	X	X	X	High-Z
	X	L	X	X	High-Z
Output Disabled	L	H	H	H	High-Z
Read	L	H	H	L	D <sub>OUT</sub>
Write	L	H	L	X	D <sub>IN</sub>

## HY6264A 8,192×8-Bit CMOS SRAM

### DC CHARACTERISTICS

( $V_{CC}=5V \pm 10\%$ ,  $T_A=0^\circ C$  to  $70^\circ C$ )

SYMBOL	PARAMETER	TEST CONDITIONS	HY6264A			UNIT	
			MIN.	TYP. <sup>(1)</sup>	MAX.		
$ I_{LI} $	Input Leakage Current	$V_{IN}=GND$ to $V_{CC}$	—	—	1	$\mu A$	
$ I_{LO} $	Output Leakage Current	$\overline{CS}_1=V_{IH}$ , $CS_2=\overline{V}_{IL}$ or $\overline{OE}=V_{IH}$ , $V_{I/O}=GND$ to $V_{CC}$	—	—	1	$\mu A$	
$I_{CC}$	Operating Power Supply Current	$\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$ , $I_{I/O}=0mA$	—	7	15	mA	
$I_{CC1}$	Average Operating Current	$\overline{CS}_1=V_{IL}$ , $CS_2=V_{IH}$ , Min, Duty Cycle=100%.	70	—	30	50	mA
			85	—	27	50	mA
			100	—	24	50	mA
			120	—	21	50	mA
			150	—	18	50	mA
$I_{SB}$	Standby Power Supply Current	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$	—	0.4	2	mA	
$I_{SB1}^{(2)}$		$\overline{CS}_1 \geq V_{CC}-0.2V$ , $CS_2 \leq 0.2V$ or $\geq V_{CC}-0.2V$	L	—	2	100	$\mu A$
			LL	—	2	50	
$I_{SB2}$		$\overline{CS}_1 \leq 0.2V$ or $\geq V_{CC}-0.2V$ , $CS_2 \leq 0.2V$	L	—	2	100	$\mu A$
	LL		—	2	50		
$V_{OL}$	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V	
$V_{OH}$	Output High Voltage	$I_{OH}=-1.0mA$	2.4	—	—	V	

**NOTES:**

1. Typical values are at  $V_{CC}=5V$ ,  $T_A=25^\circ C$  and specified loading.

2.  $V_{IL\ min}=-0.5V$

### AC CHARACTERISTICS

( $V_{CC}=5V \pm 10\%$ ,  $T_A=0^\circ C$  to  $70^\circ C$ )

#### READ CYCLE

SYMBOL	PARAMETER	HY6264A-70		HY6264A-85		HY6264A-10		HY6264A-12		HY6264A-15		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$t_{RC}$	Read Cycle Time	70	—	85	—	100	—	120	—	150	—	ns	
$t_{AA}$	Address Access Time	—	70	—	85	—	100	—	120	—	150	ns	
$t_{ACS1}$	Chip Select Access Time	$\overline{CS}_1$	—	70	—	85	—	100	—	120	—	150	ns
$t_{ACS2}$		$CS_2$	—	70	—	85	—	100	—	120	—	150	ns
$t_{OE}$	Output Enable to Output Valid	—	45	—	50	—	55	—	60	—	70	ns	
$t_{CLZ1}$	Chip Select to Output in Low-Z	$\overline{CS}_1$	10	—	10	—	10	—	10	—	15	—	ns
$t_{CLZ2}$		$CS_2$	10	—	10	—	10	—	10	—	15	—	ns
$t_{OLZ}$	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns	
$t_{CHZ1}$	Chip Deselect to Output in High-Z	$\overline{CS}_1$	0	30	0	35	0	35	0	40	0	50	ns
$t_{CHZ2}$		$CS_2$	0	30	0	35	0	35	0	40	0	50	ns
$t_{OHZ}$	Output Disable to Output in High-Z	0	30	0	35	0	35	0	40	0	50	ns	
$t_{OH}$	Output Hold from Address Change	5	—	5	—	10	—	10	—	10	—	ns	

# HY6264A 8,192×8-Bit CMOS SRAM

## WRITE CYCLE

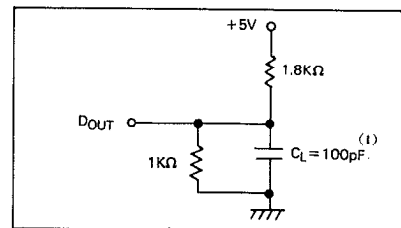
SYMBOL	PARAMETER	HY6264A-70		HY6264A-85		HY6264A-10		HY6264A-12		HY6264A-15		UNIT	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t <sub>WC</sub>	Write Cycle Time	70	—	85	—	100	—	120	—	150	—	ns	
t <sub>cw</sub>	Chip Select to End of Write	55	—	60	—	70	—	85	—	100	—	ns	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
t <sub>AW</sub>	Address Valid to End of Write	55	—	60	—	70	—	85	—	100	—	ns	
t <sub>WP</sub>	Write Pulse Width	50	—	55	—	60	—	70	—	90	—	ns	
t <sub>WR1</sub>	Write Recovery Time	CS <sub>1</sub> , WE	0	—	0	—	0	—	0	—	0	—	ns
t <sub>WR2</sub>		CS <sub>2</sub>	0	—	0	—	0	—	0	—	0	—	ns
t <sub>WHZ</sub>	Write to Output in High-Z	0	30	0	35	0	35	0	40	0	50	ns	
t <sub>DW</sub>	Data to Write Time Overlap	35	—	35	—	40	—	50	—	60	—	ns	
t <sub>DH</sub>	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns	
t <sub>OHZ</sub>	Output Disable to Output in High-Z	0	30	0	35	0	35	0	40	0	50	ns	
t <sub>OW</sub>	Output Active from End of Write	5	—	5	—	5	—	5	—	10	—	ns	

## AC TEST CONDITIONS

(T<sub>A</sub>=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

## OUTPUT LOAD



NOTE:  
1. Including scope and the jig.

## CAPACITANCE<sup>(1)</sup>

(T<sub>A</sub>=25°C, f=1.0MHz)

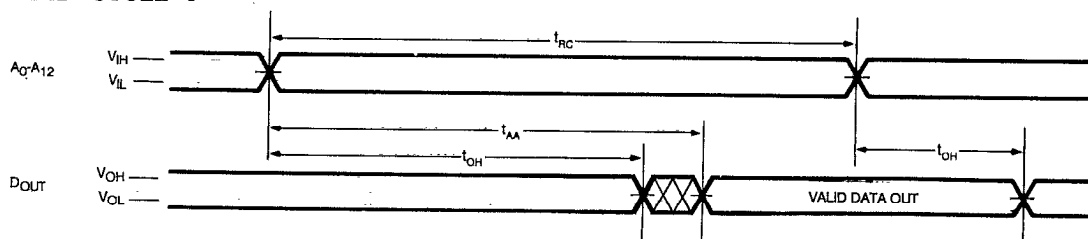
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	6	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> =0V	8	pF

NOTE:

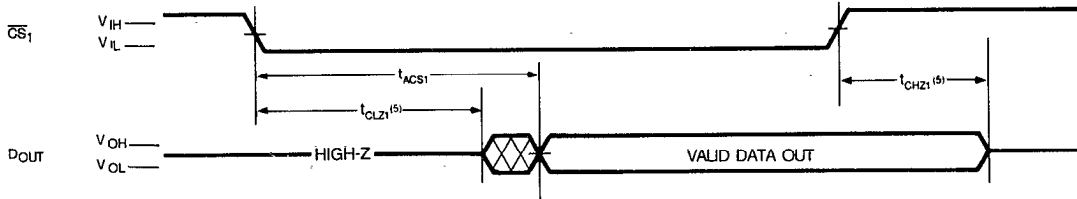
1. This parameter is sampled and not 100% tested.

## TIMING DIAGRAMS

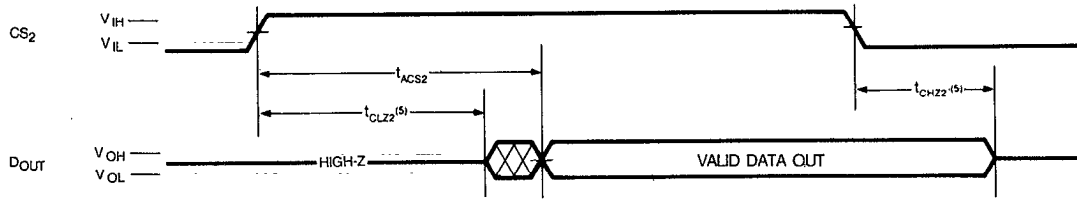
### READ CYCLE<sup>1(1,2,4)</sup>



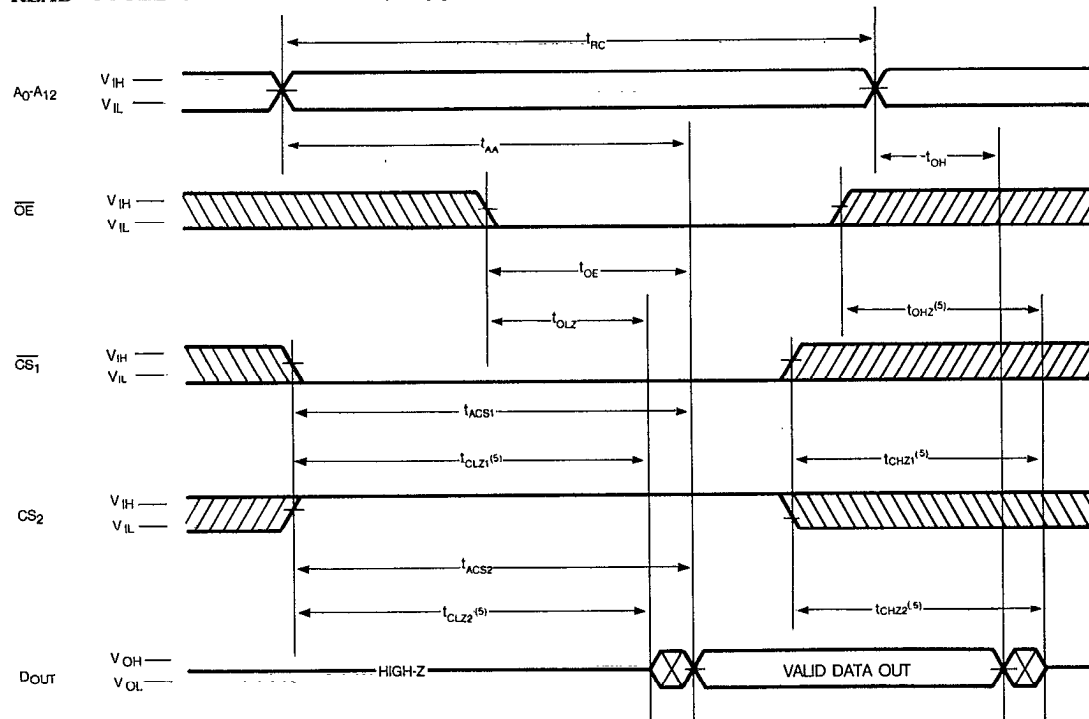
READ CYCLE 2<sup>(1,3,4,6)</sup>



READ CYCLE 3<sup>(1,4,7)</sup>



READ CYCLE 4<sup>(1,2)</sup>

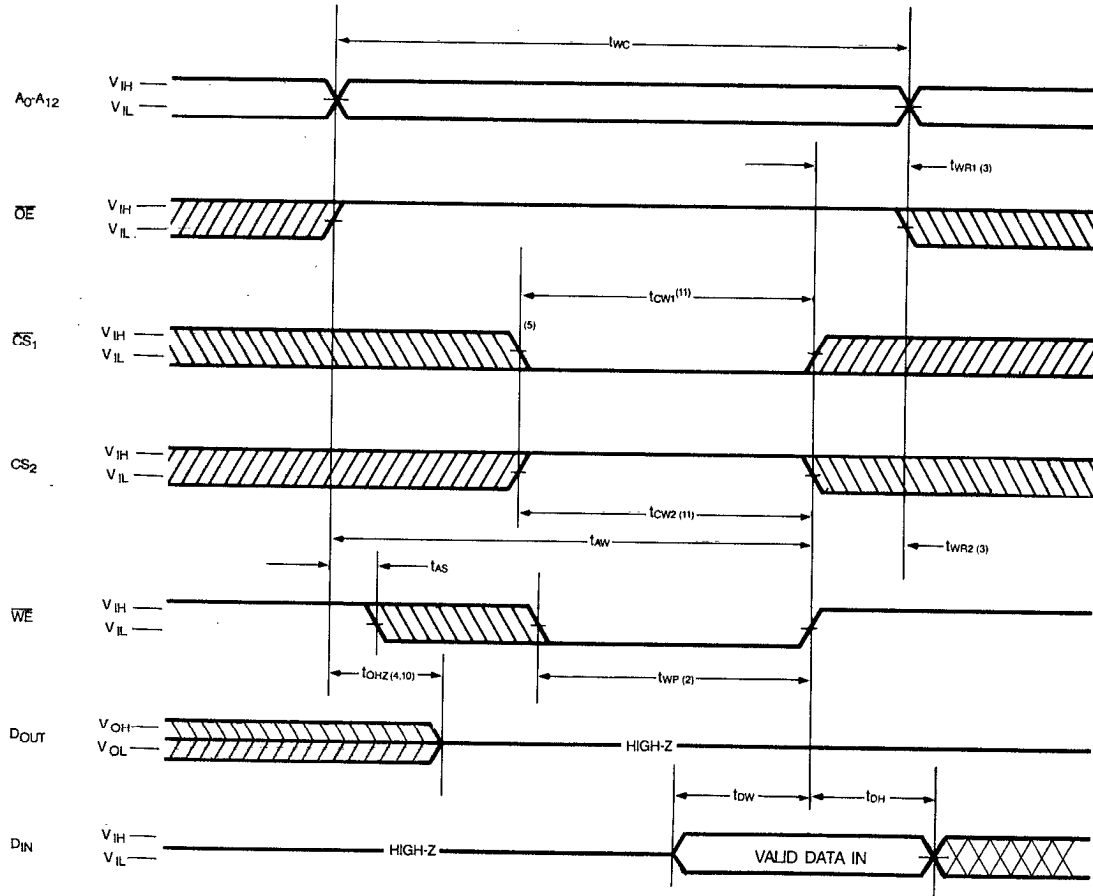


NOTES :

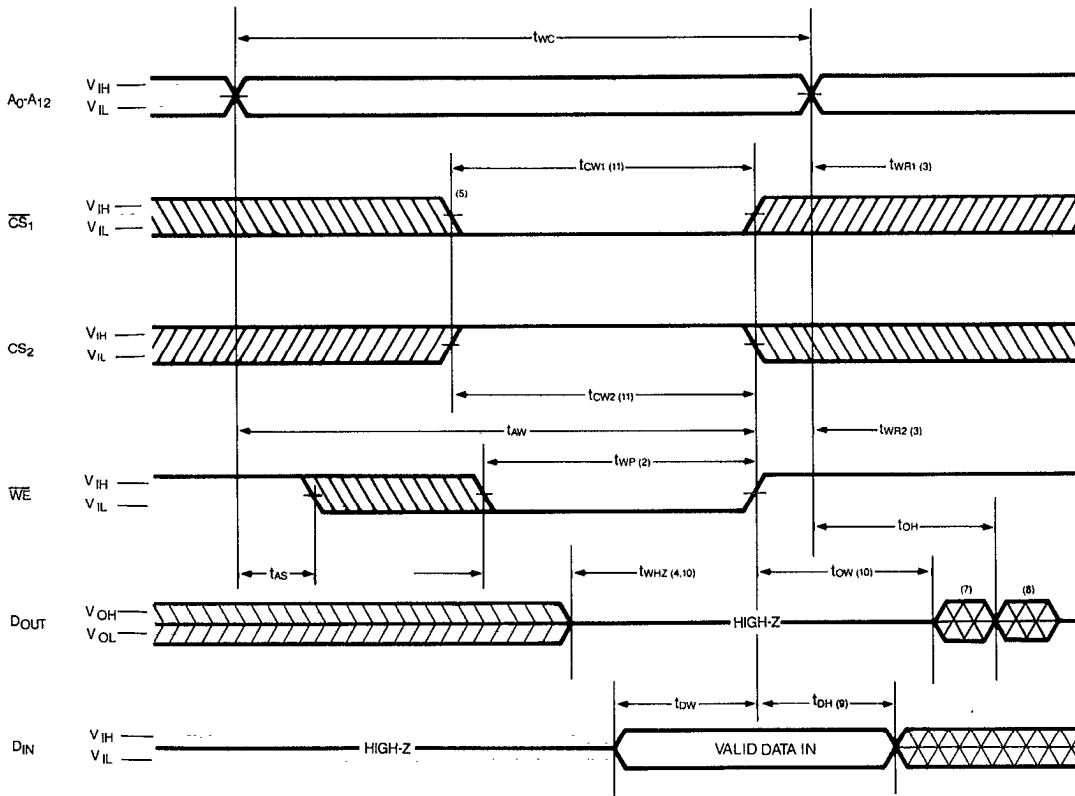
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected  $\overline{CS}_1 = V_{IL}$  and  $\overline{CS}_2 = V_{IH}$ .
3. Addresses are valid prior to or coincident with  $\overline{CS}_1$  transition low.
4.  $\overline{OE} = V_{IL}$ .
5. Transition is measured  $\pm 500mV$  from steady state. This parameter is sampled and not 100% tested.
6.  $\overline{CS}_2$  is high.
7.  $\overline{CS}_1$  is low.

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## WRITE CYCLE 1<sup>(1)</sup>



WRITE CYCLE 2<sup>(1,6)</sup>



NOTES :

1.  $\overline{WE}$  must be high during address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of low  $\overline{CS_1}$ , high  $CS_2$  and low  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS_1}$  or  $\overline{WE}$  going high or  $CS_2$  going low to the end of write cycle.
4. During this period, I/O pins are in output state so that the input signals of opposite phase to the output must not be applied.
5. If the  $\overline{CS_1}$  low transition or the  $CS_2$  high transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
7.  $D_{OUT}$  is the same phase of write data of this write cycle.
8.  $D_{OUT}$  is the read data of next address.
9. If  $\overline{CS_1}$  is low and  $CS_2$  is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured  $\pm 500mV$  from steady state.
11.  $t_{CW}$  is measured from the later of  $\overline{CS_1}$  going low or  $CS_2$  going high to the end of write.

**DATA RETENTION CHARACTERISTICS<sup>(1)</sup>**

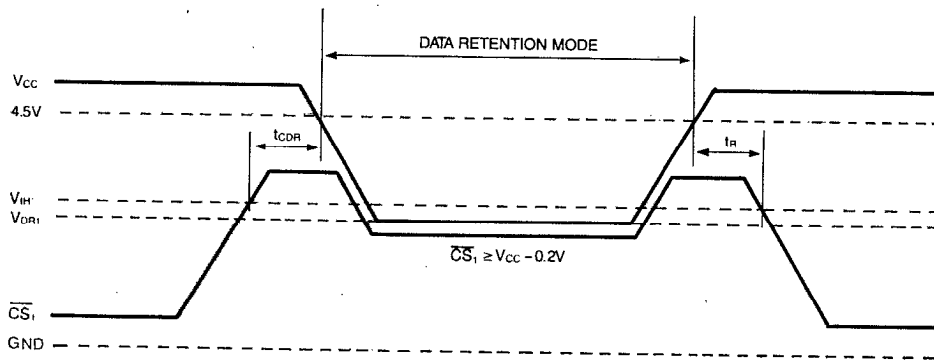
( $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
$V_{DR1}$	Data Retention	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	2.0	-	-	V	
$V_{DR2}$	Supply Voltage	$CS_2 \leq 0.2\text{V}$ , $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ or $\overline{CS}_1 \leq 0.2\text{V}$	2.0	-	-	V	
$I_{CCDR1}$	Data Retention Current	$V_{CC}=3\text{V}$ , $V_{IN}=0\text{V}$ to $V_{CC}$ $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	L	-	1	50	$\mu\text{A}$
			LL	-	1	5 <sup>(2)</sup>	
$I_{CCDR2}$	Data Retention Current	$V_{CC}=3\text{V}$ , $V_{IN}=0\text{V}$ to $V_{CC}$ $CS_2 \leq 0.2\text{V}$ , $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ or $\overline{CS}_1 \leq 0.2\text{V}$	L	-	1	50	$\mu\text{A}$
			LL	-	1	5 <sup>(2)</sup>	
$t_{CDR}$	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns	
$t_R$	Operation Recovery Time		$t_{RC}^{(3)}$	-	-	ns	

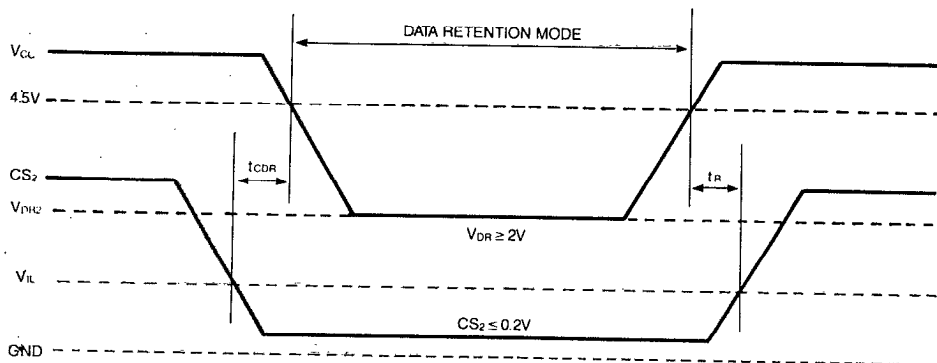
NOTES :

1. These characteristics are guaranteed for L and LL-version.
2.  $3\mu\text{A}$  max. at  $T_A=0^{\circ}\text{C}$  to  $40^{\circ}\text{C}$
3.  $t_{RC}$ =Read Cycle Time

**DATA RETENTION TIMING DIAGRAM 1 ( $\overline{CS}_1$  Controlled)**



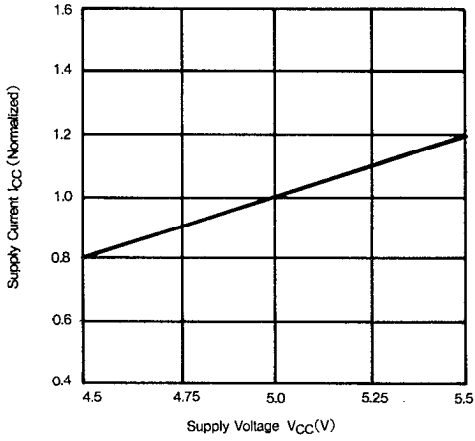
**DATA RETENTION TIMING DIAGRAM 2 ( $CS_2$  Controlled)**



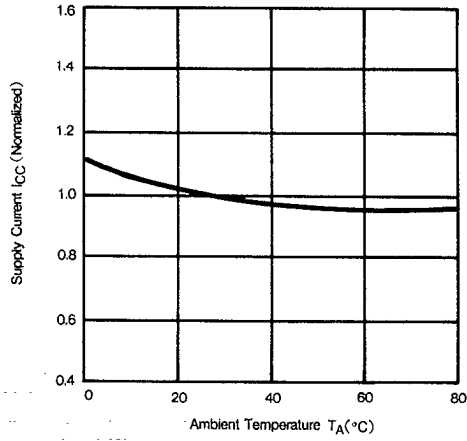
**ELECTRICAL CHARACTERISTIC CURVES**

( $V_{CC}=5V$ ,  $T_A=25^{\circ}C$ , unless otherwise noted)

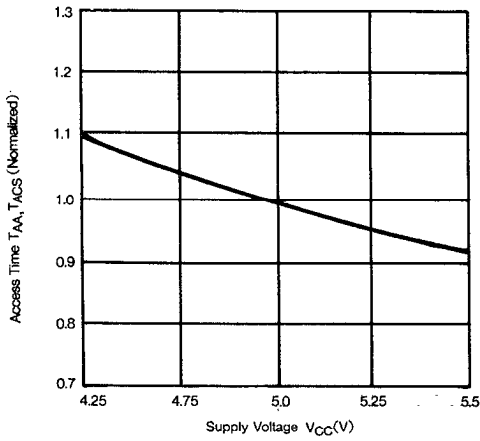
SUPPLY CURRENT vs. SUPPLY VOLTAGE



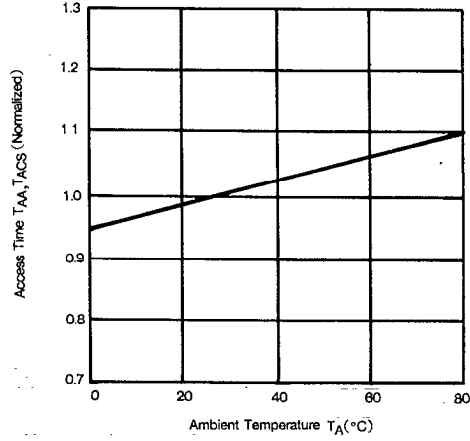
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



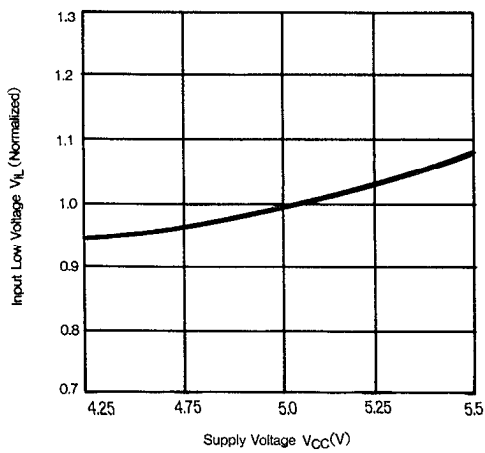
ACCESS TIME vs. SUPPLY VOLTAGE



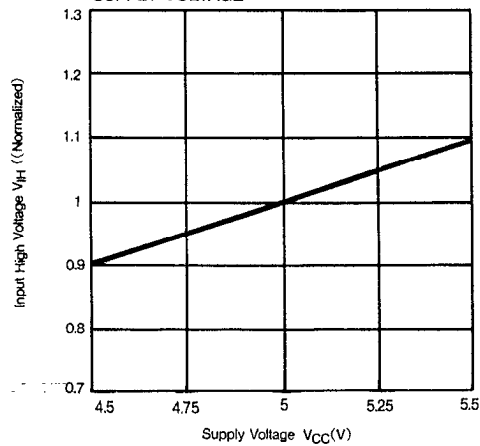
ACCESS TIME vs. AMBIENT TEMPERATURE



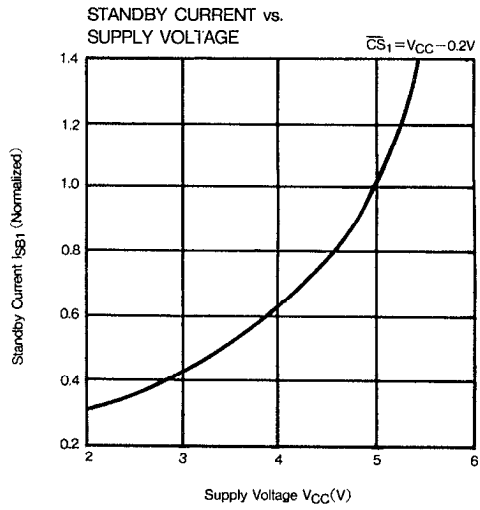
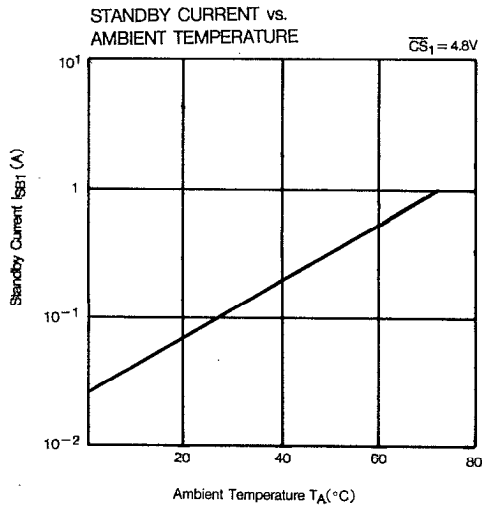
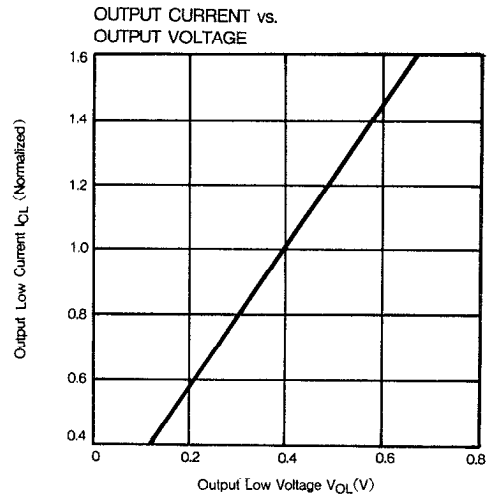
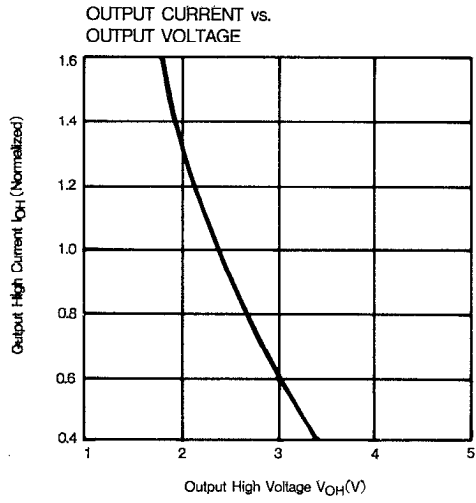
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE

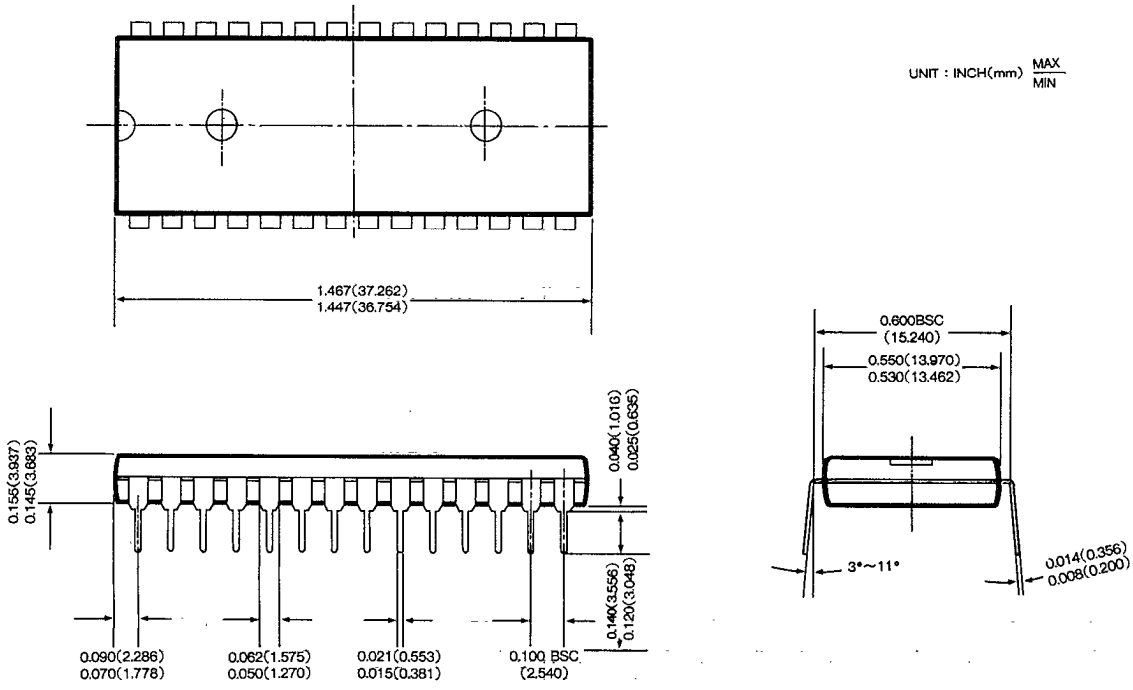


# HY6264A 8,192×8-Bit CMOS SRAM

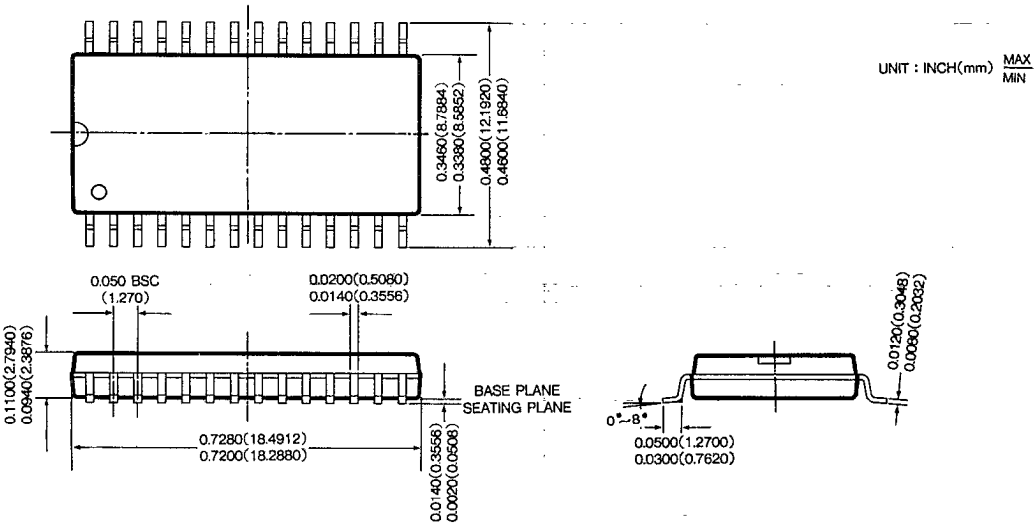


PACKAGE INFORMATION

• 28 PIN PLASTIC DUAL IN LINE PACKAGE—600MIL



• 28 PIN SMALL OUTLINE PACKAGE—330MIL





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