

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40374B

MSI

Octal D-type flip-flop with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Octal D-type flip-flop with 3-state outputs

HEF40374B MSI

DESCRIPTION

The HEF40374B is an octal D-type flip-flop with 3-state buffered outputs with a common clock input (CP). The device is used primarily as an 8-bit positive edge-triggered storage register for interfacing with a 3-state bus. Data on the D-inputs is transferred to storage during the LOW-to-HIGH transition of the clock (CP) input. The 3-state output buffers are controlled by an active LOW output enable input (\overline{EO}). A HIGH on \overline{EO} forces the eight outputs to a high impedance OFF-state. When \overline{EO} is LOW, the data in the register appears at the outputs.

The output stages have high current output capability suitable for driving highly capacitive loads. The device features hysteresis on the CP input to improve noise rejection. Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40374B is pin and functionally compatible with the TTL '374' device.

Supply voltage range: 3 to 15 V.

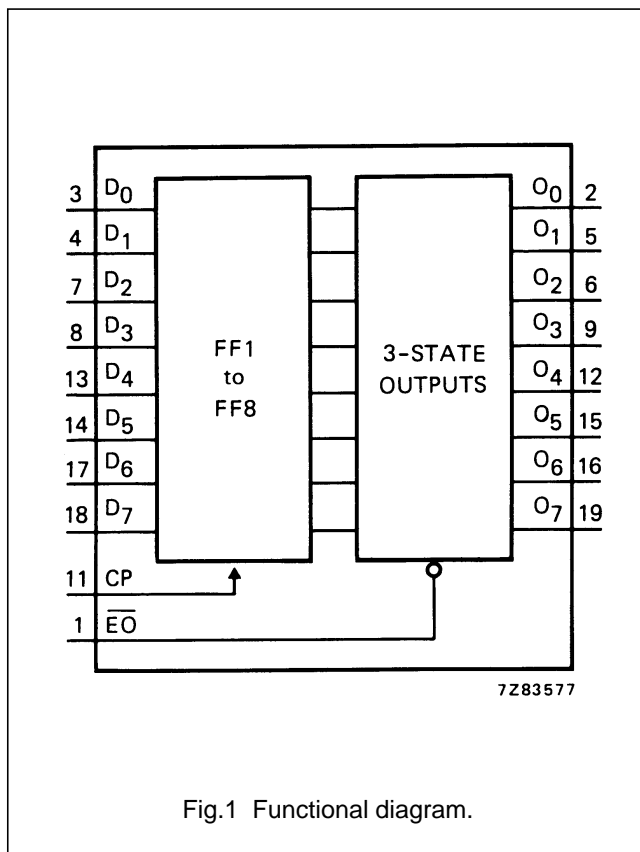


Fig.1 Functional diagram.

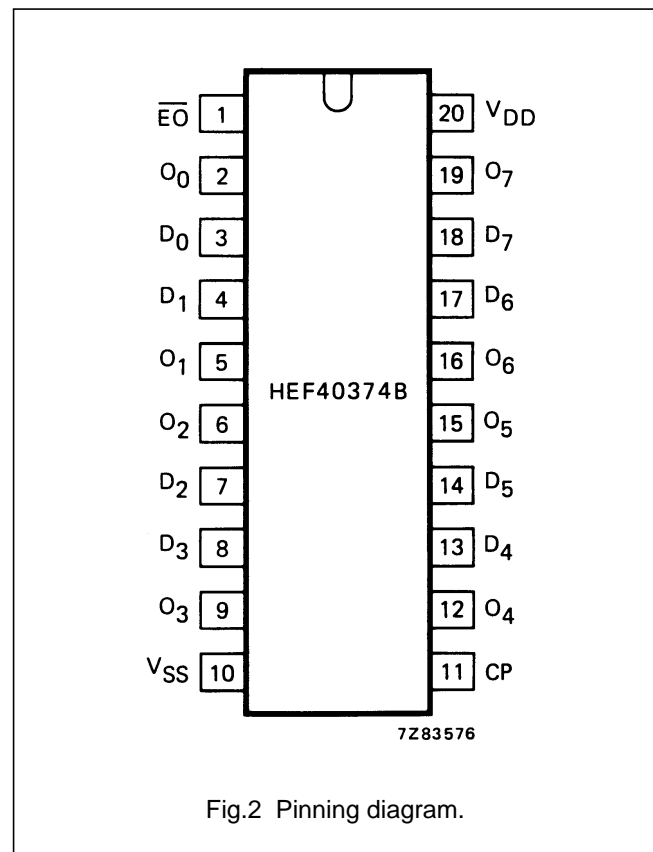


Fig.2 Pinning diagram.

- HEF40374BP(N): 20-lead DIL; plastic (SOT146-1)
- HEF40374BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
- HEF40374BT(D): 20-lead SO; plastic (SOT163-1)
- (): Package Designator North America

PINNING

- D₀ to D₇ data inputs
- CP clock input
- \overline{EO} output enable input (active LOW)
- O₀ to O₇ 3-state buffered outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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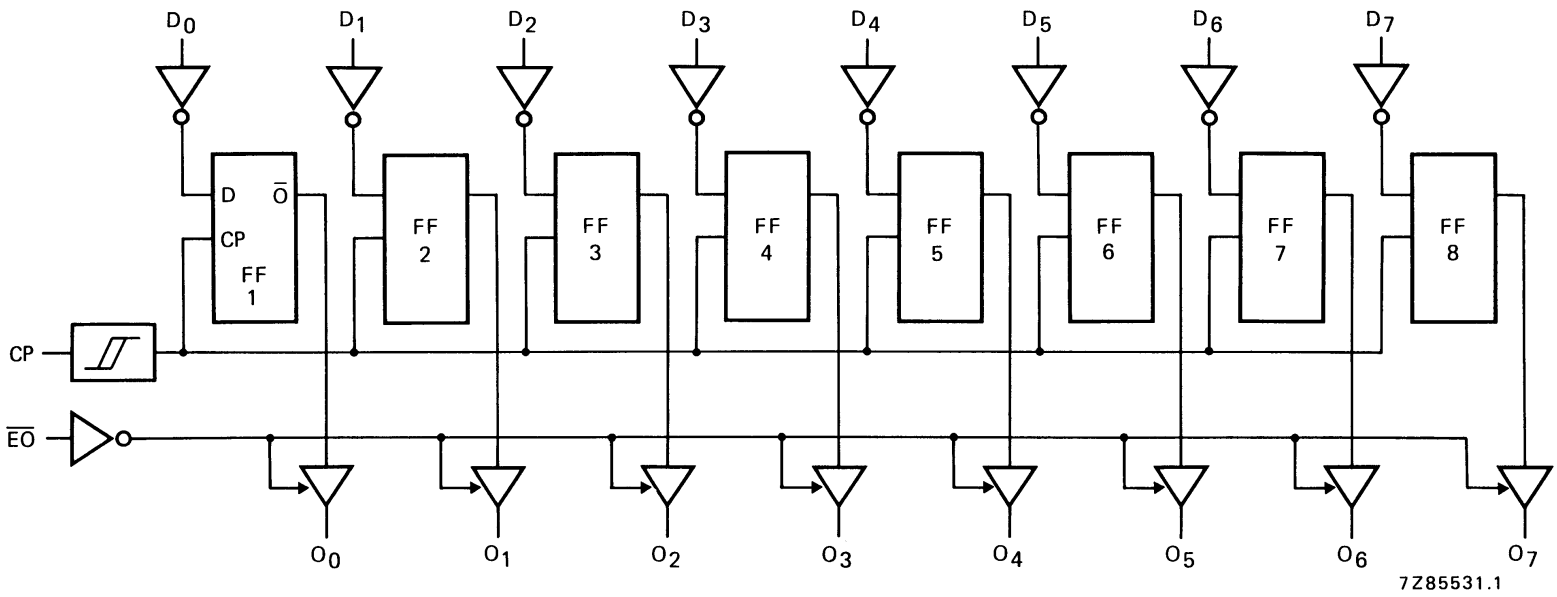






Fig.3 Logic diagram.


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FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS O ₀ TO O ₇
	\overline{EO}	CP	D _n		
load & read register	L		l	L	L
	L		h	H	H
load register & disable outputs	H		l	L	Z
	H		h	H	Z

Notes

- H = HIGH state (the more positive voltage)
 h = HIGH state (one set-up time prior to the LOW-to-HIGH clock transition)
 L = LOW state (the less positive voltage)
 l = LOW state (one set-up time prior to the LOW-to-HIGH clock transition)
 Z = high impedance OFF-state
 = LOW-to-HIGH clock transition

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

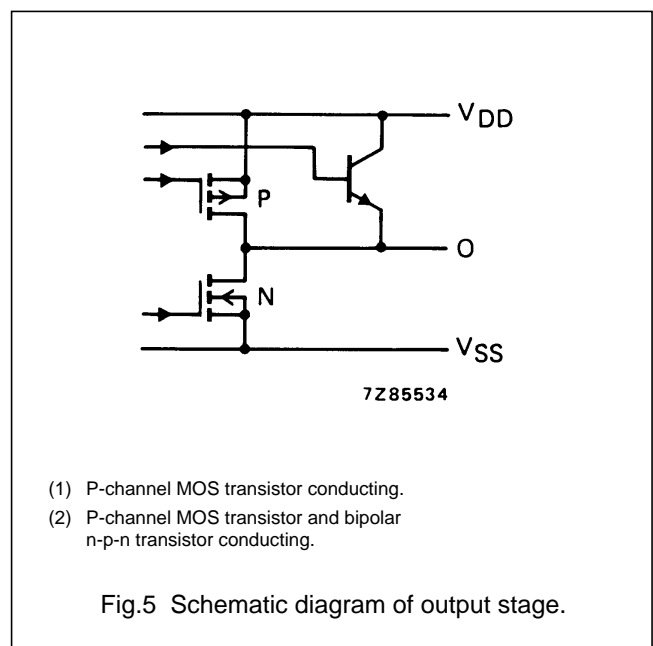
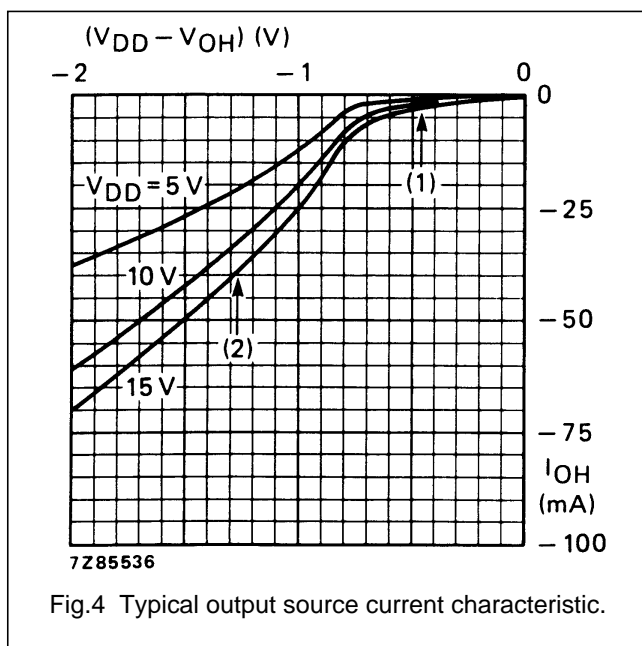
See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C. source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

DC CHARACTERISTICS

$V_{SS} = 0 V$

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	$T_{amb} (°C)$					
					-40		+25		+85	
					MIN.	TYP.	MIN.	TYP.	MIN.	TYP.
Output current HIGH	5	4,6		$-I_{OH}$	0,75	0,6	1,2	0,45	mA	
	10	9,5			1,85	1,5	3,0	1,1		
	15	13,5			14,5	15	50	15,5		
Output current HIGH	5	3,6		$-I_{OH}$	9,3	10	24	10,7	mA	
	10	8,4			14,4	15	46	15,0		
	15	13,2			19,5	20	62	19,8		
Output current LOW	5		0,4	I_{OL}	2,9	2,3	5,4	1,75	mA	
	10		0,5		9,5	7,6	17	5,50		
	15		1,5		30,0	25	45	19,0		
Hysteresis voltage at clock input (CP)	5			V_H			220		mV	
	10						250			
	15						320			



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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays CP \rightarrow O_n HIGH to LOW	5	t_{PHL}		125	250	ns	113 ns + (0,24 ns/pF) C_L	
	10		55	110	ns	54 ns + (0,01 ns/pF) C_L		
	15		40	80	ns	36 ns + (0,07 ns/pF) C_L		
	CP \rightarrow O_n LOW to HIGH	5	t_{PLH}		125	250	ns	122 ns + (0,06 ns/pF) C_L
		10		55	110	ns	53 ns + (0,03 ns/pF) C_L	
		15		40	80	ns	39 ns + (0,02 ns/pF) C_L	
Output transition times HIGH to LOW	5	t_{THL}		40	80	ns	see Fig.6	
	10		20	40	ns			
	15		15	30	ns			
	LOW to HIGH	5	t_{TLH}		30	60		ns
		10		20	40	ns		
		15		15	30	ns		
3-state propagation delays Output disable times $\overline{EO} \rightarrow O_n$ HIGH	5	t_{PHZ}		60	120	ns		
	10		30	60	ns			
	15		24	48	ns			
	LOW	5	t_{PLZ}		70	140	ns	
		10		35	70	ns		
		15		30	60	ns		
Output enable times $\overline{EO} \rightarrow O_n$ HIGH	5	t_{PZH}		65	130	ns		
	10		30	60	ns			
	15		24	48	ns			
	LOW	5	t_{PZL}		85	170	ns	
		10		35	70	ns		
		15		25	50	ns		
Set-up time $D_n \rightarrow CP$	5	t_{su}	20	0		ns		
	10		20	2		ns		
	15		20	5		ns		
Hold time $D_n \rightarrow CP$	5	t_{hold}	20	10		ns		
	10		15	2		ns		
	15		10	0		ns		

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; LOW	5	t _{WCPL}	50	25	ns	
	10		25	12	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f _{max}	25	5	MHz	
	10		6	12	MHz	
	15		8	17	MHz	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	3 775 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	15 700 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	40 575 f _i + ∑ (f _o C _L) × V _{DD} ²	

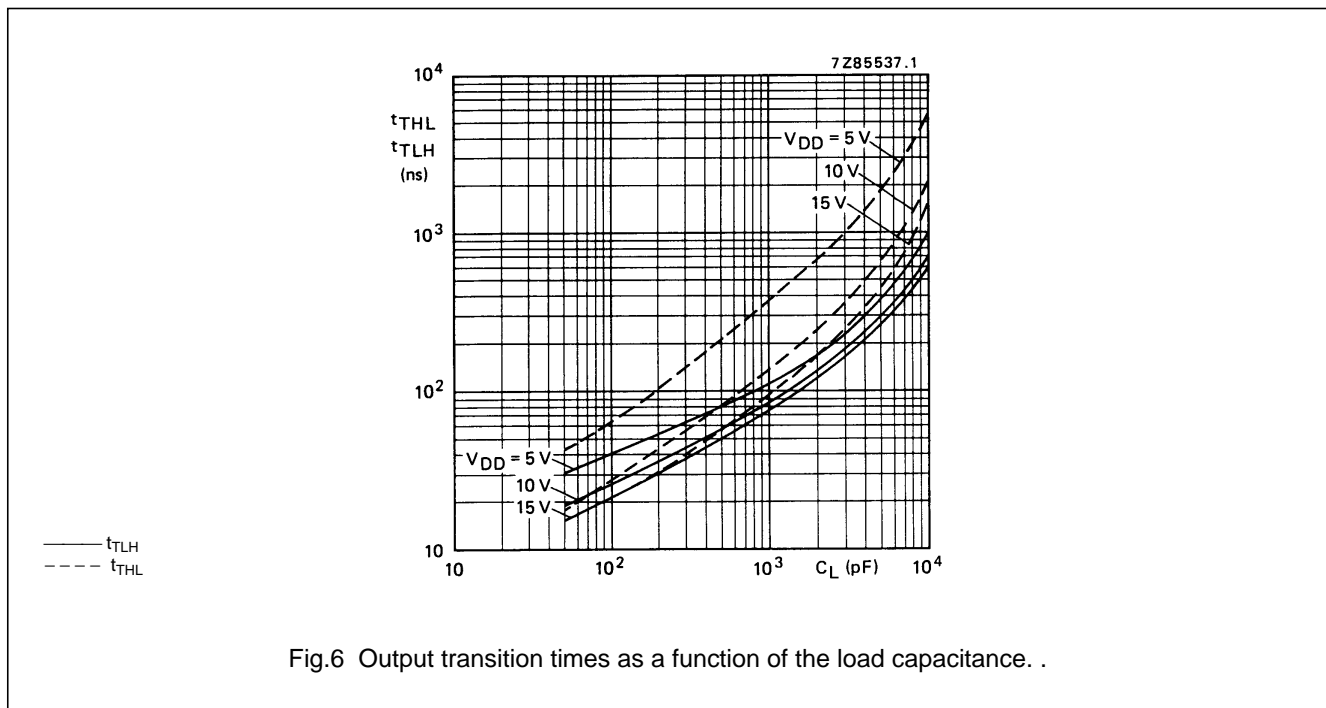


Fig.6 Output transition times as a function of the load capacitance. .



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