FAIRCHILD SEMICONDUCTOR®

April 2013

FDP5N50NZ / FDPF5N50NZ

N-Channel UniFET™ II MOSFET

500 V, 4.5 A, 1.5 Ω

Features

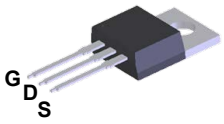
- $R_{DS(on)}$ = 1.38 Ω (Typ.) @ V_{GS} = 10 V, I_D = 2.25 A
- Low Gate Charge (Typ. 9 nC)
- Low Crss (Typ. 4 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Imoroved Capability
- RoHS Compliant

Applications

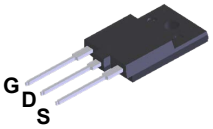
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

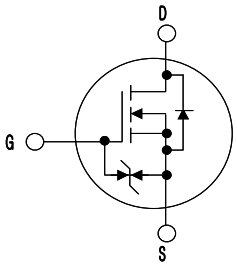
UniFET™ II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220



TO-220F



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDP5N50NZ	FDPF5N50NZ	Unit
V_{DSS}	Drain to Source Voltage			500		V
V_{GSS}	Gate to Source Voltage			±25		V
I_D	Drain Current	-Continuous (T_C = 25°C)		4.5	4.5*	A
		-Continuous (T_C = 100°C)		2.7	2.7*	
I_{DM}	Drain Current	- Pulsed	(Note 1)	18	18*	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	160		mJ
I_{AR}	Avalanche Current		(Note 1)	4.5		A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	7.8		mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	10		V/ns
P_D	Power Dissipation	(T_C = 25°C)		78	30	W
		- Derate above 25°C		0.62	0.24	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300		°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP5N50NZ	FDPF5N50NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.6	4.1	°C/W
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ.	-	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP5N50NZ	FDP5N50NZ	TO-220	-	-	50
FDPF5N50NZ	FDPF5N50NZ	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_C = 25°C	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 400V, V_{GS} = 0V, T_C = 125°C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25V, V_{DS} = 0V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 2.25A	-	1.38	1.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 2.25A (Note 4)	-	3.54	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	330	440	pF
C_{oss}	Output Capacitance		-	50	70	pF
C_{rss}	Reverse Transfer Capacitance		-	4	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400V I_D = 4.5A, V_{GS} = 10V (Note 4,5)	-	9	12	nC
Q_{gs}	Gate to Source Gate Charge		-	2	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 4.5A, V_{GS} = 10V, R_{GEN} = 25Ω (Note 4,5)	-	12	35	ns
t_r	Turn-On Rise Time		-	22	55	ns
$t_{d(off)}$	Turn-Off Delay Time		-	28	65	ns
t_f	Turn-Off Fall Time		-	21	50	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 4.5A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 4.5A, dI_F/dt = 100A/μs (Note 4)	-	210	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.1	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 15.8mH, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 2.8A, di/dt ≤ 200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

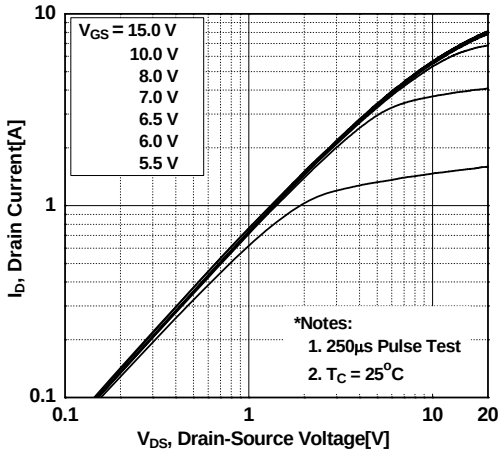


Figure 2. Transfer Characteristics

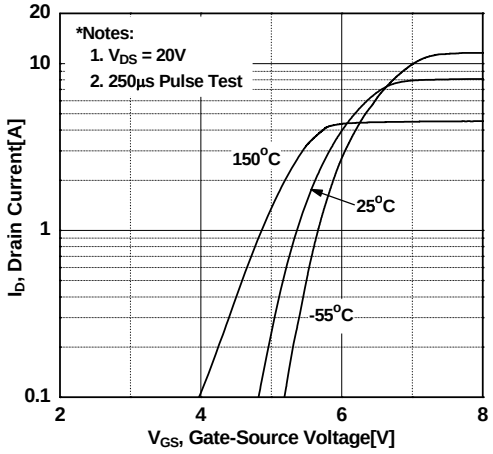


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

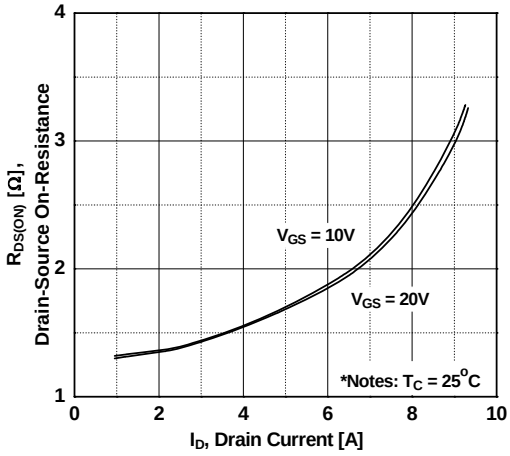


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

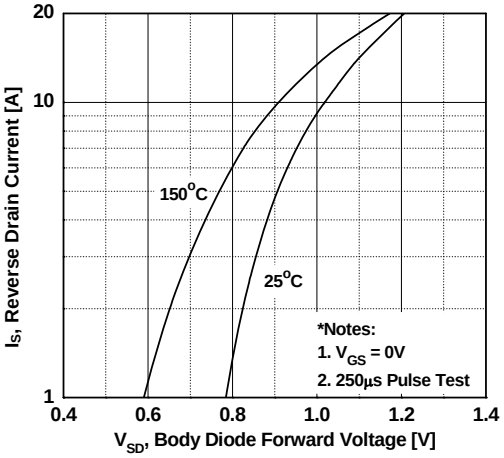


Figure 5. Capacitance Characteristics

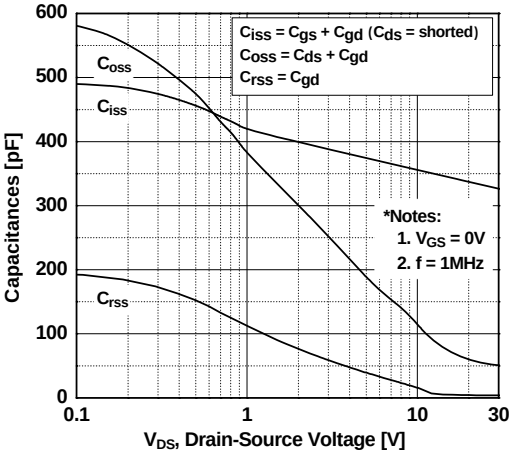
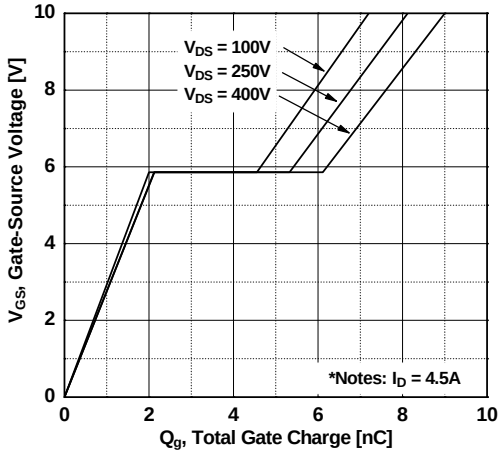


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

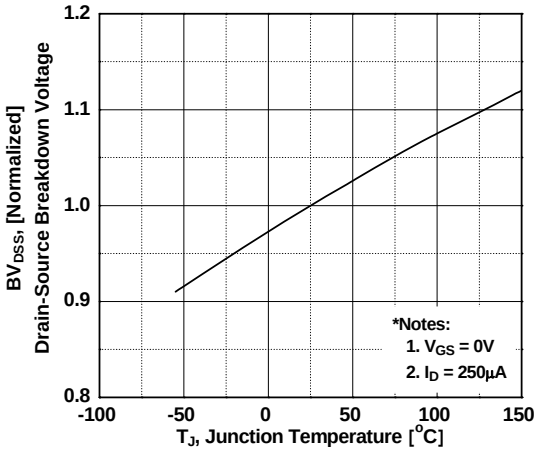


Figure 8. On-Resistance Variation vs. Temperature

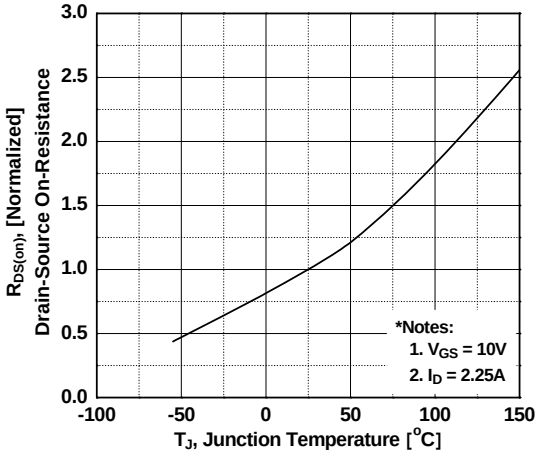


Figure 9. Maximum Safe Operating Area vs. Case Temperature-FDP5N50NZ

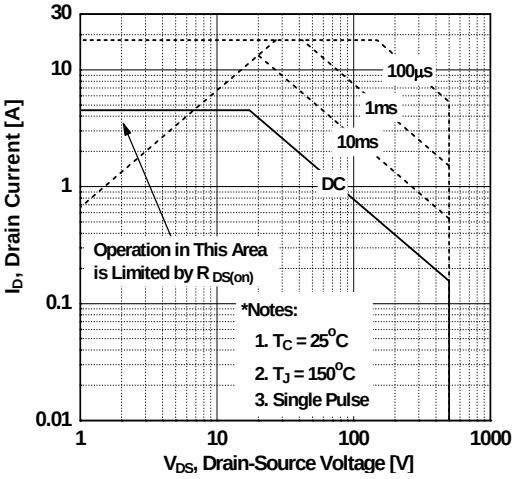


Figure 10. Maximum Safe Operating Area vs. Case Temperature-FDPF5N50NZ

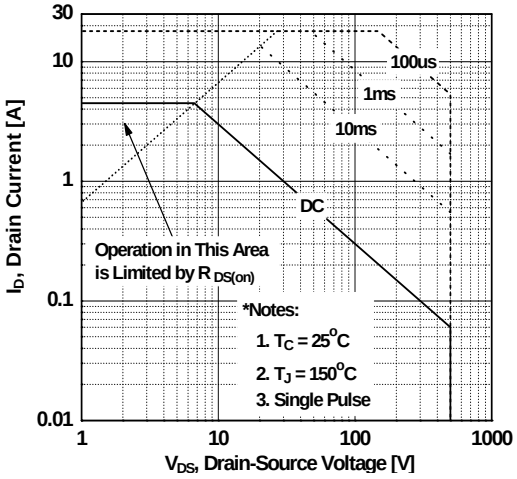
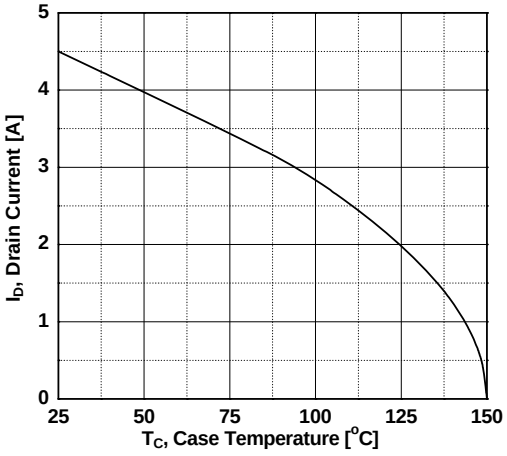


Figure 11. Maximum Drain Current



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve-FDP5N50NZ

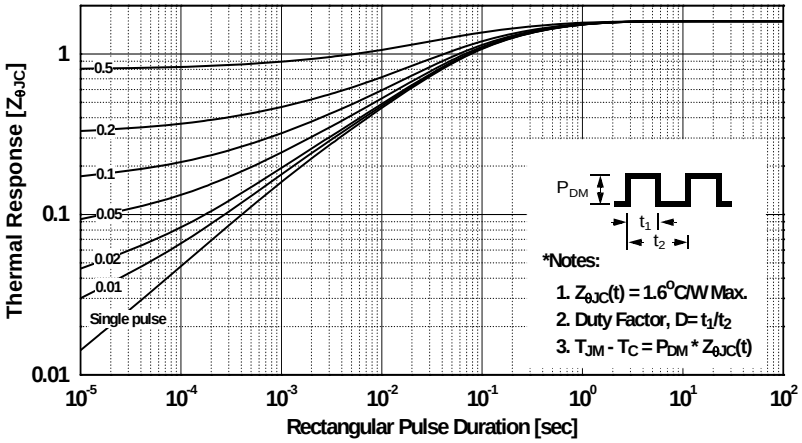
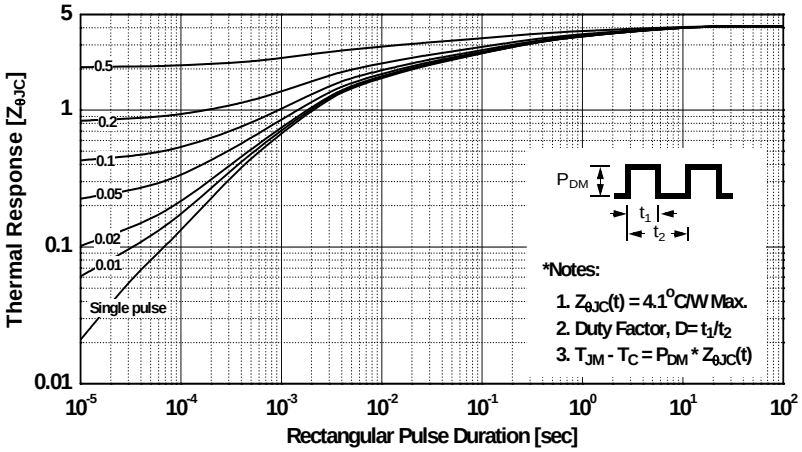
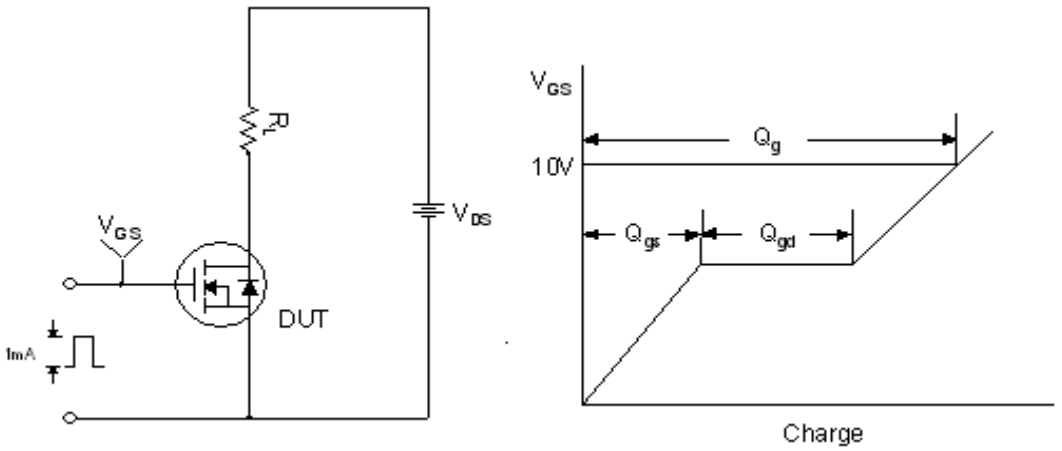


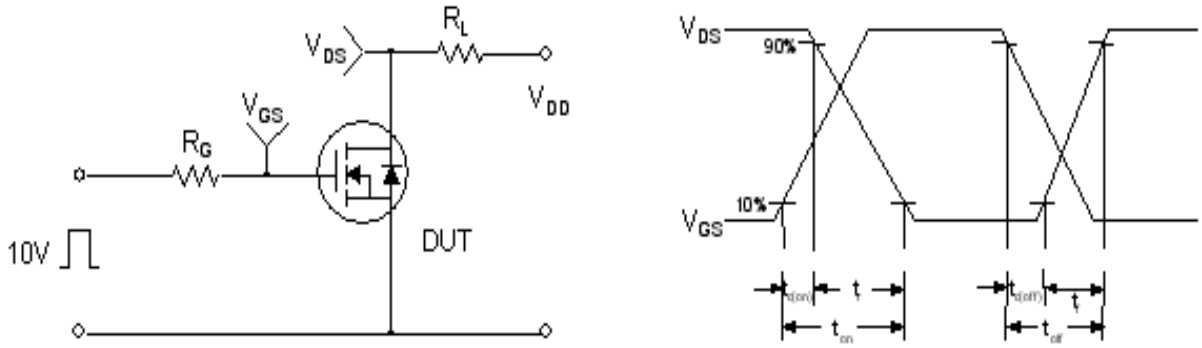
Figure 13. Transient Thermal Response Curve-FDPF5N50NZ



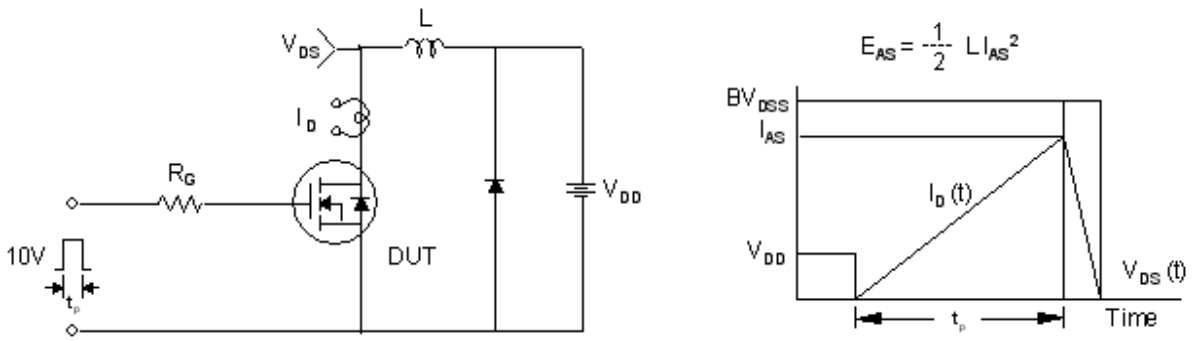
Gate Charge Test Circuit & Waveform



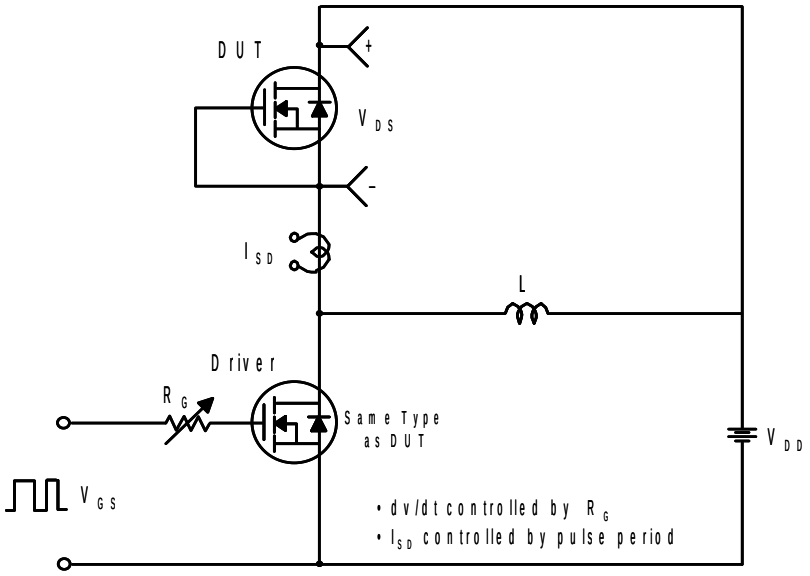
Resistive Switching Test Circuit & Waveforms

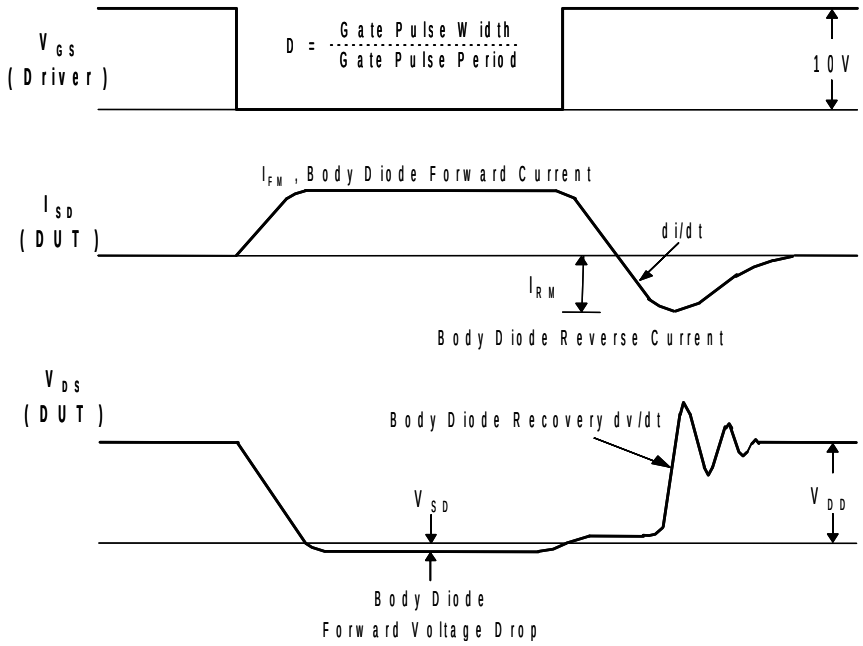


Unclamped Inductive Switching Test Circuit & Waveforms



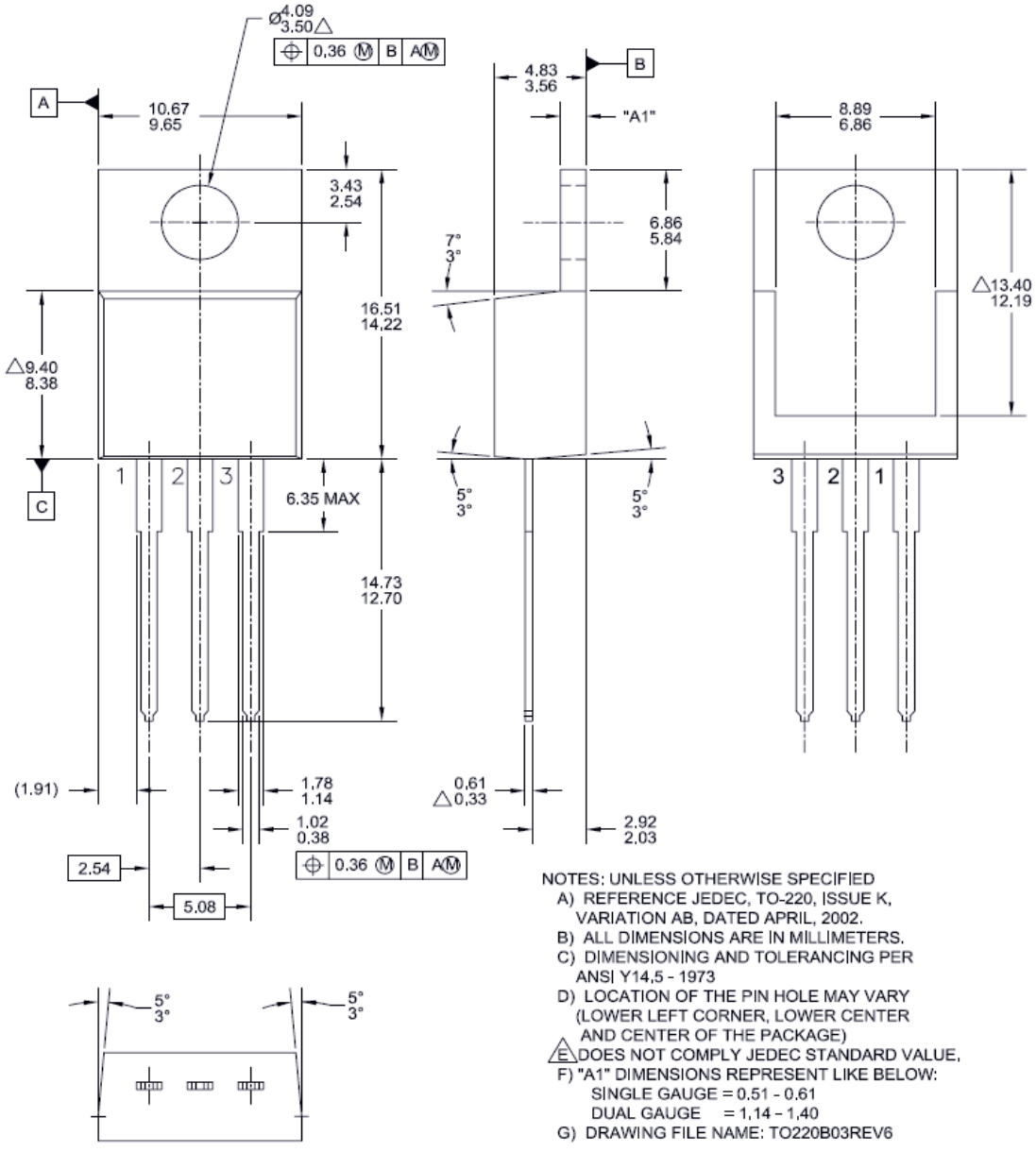
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

TO-220B03

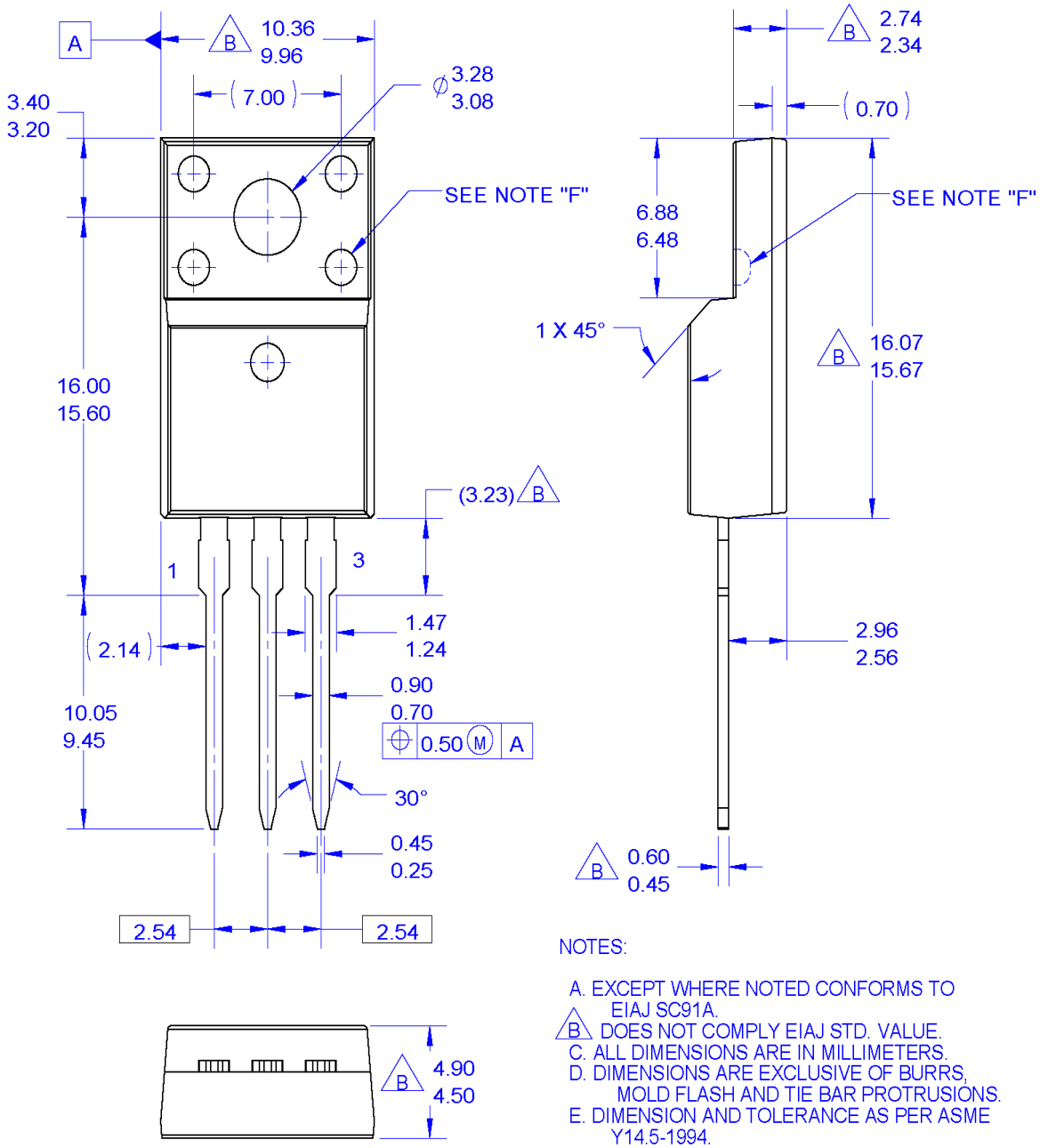


NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1,14 – 1,40
G) DRAWING FILE NAME: TO220B03REV6

Dimensions in Millimeters

Mechanical Dimensions

TO-220M03



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV3

Dimensions in Millimeters

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

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