

FDD18N20LZ

N-Channel UniFET™ MOSFET

200 V, 16 A, 125 mΩ

Features

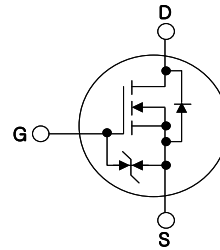
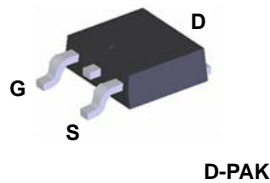
- $R_{DS(on)} = 125 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 8 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{rss} (Typ. 25 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

- LED TV
- Consumer Appliances
- Uninterruptible Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDD18N20LZ	Unit
V_{DSS}	Drain to Source Voltage	200	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	16
		-Continuous ($T_C = 100^\circ\text{C}$)	9.6
I_{DM}	Drain Current	- Pulsed (Note 1)	64
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	320
I_{AR}	Avalanche Current	(Note 1)	16
E_{AR}	Repetitive Avalanche Energy	(Note 1)	8.9
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	89
		- Derate above 25°C	0.7
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDD18N20LZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD18N20LZ	FDD18N20LZ	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	200	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.2	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = 160\text{V}$, $T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 8\text{A}$ $V_{GS} = 5\text{V}$, $I_D = 8\text{A}$	-	0.10 0.11	0.125 0.13	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}$, $I_D = 2\text{A}$ (Note 4)	-	11	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1185	1575	pF
C_{oss}	Output Capacitance		-	190	255	pF
C_{riss}	Reverse Transfer Capacitance		-	25	40	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 200\text{V}$, $I_D = 16\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	30	40	nC
Q_{gs}	Gate to Source Gate Charge		-	3.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	8.5	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{V}$, $I_D = 16\text{A}$ $V_{GS} = 10\text{V}$, $R_G = 25\Omega$ (Note 4, 5)	-	15	40	ns
t_r	Turn-On Rise Time		-	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	135	280	ns
t_f	Turn-Off Fall Time		-	50	110	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	16	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	64	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_{SD} = 4\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}$, $I_{SD} = 4\text{A}$	-	105	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	0.4	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 2.5\text{mH}$, $I_{AS} = 16\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 16\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

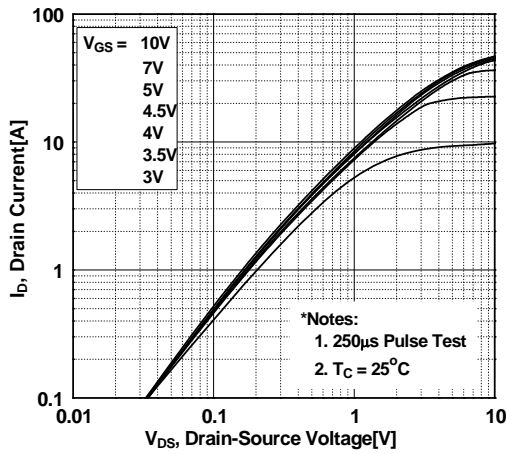


Figure 2. Transfer Characteristics

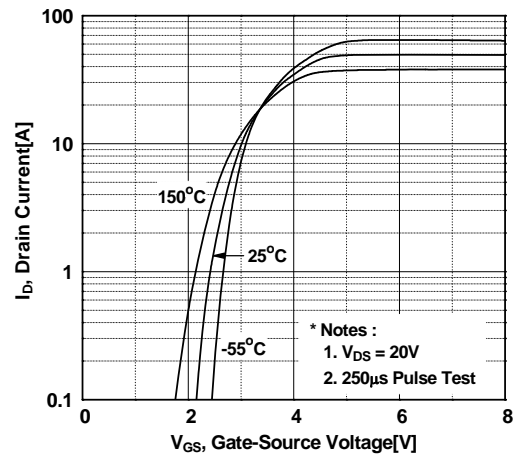


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

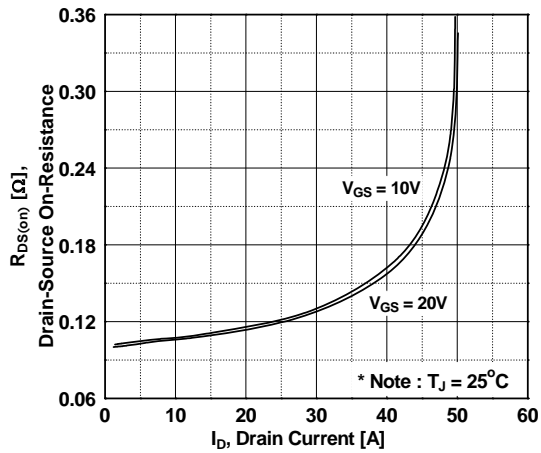


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

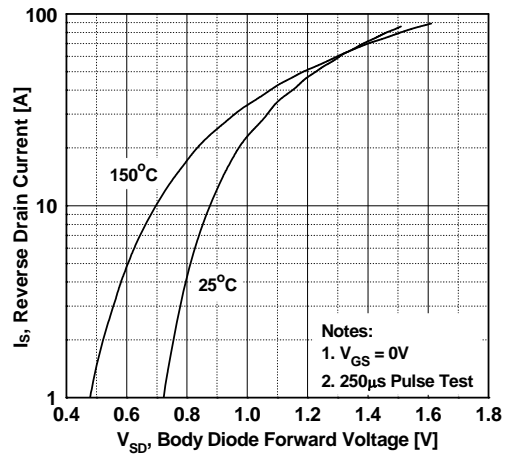


Figure 5. Capacitance Characteristics

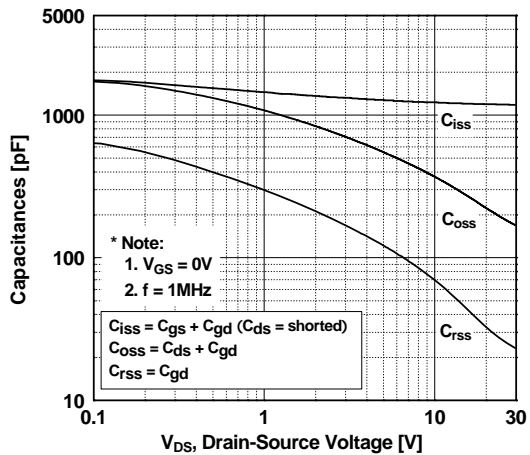
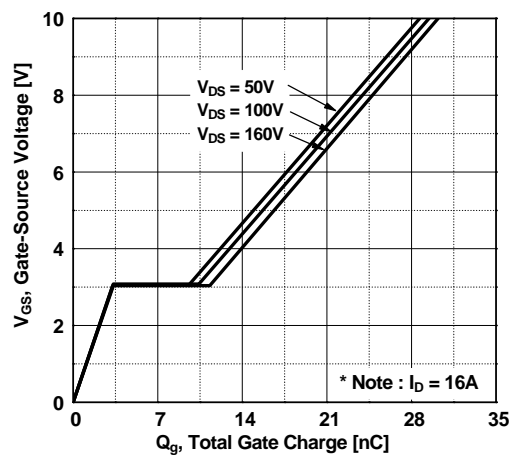


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

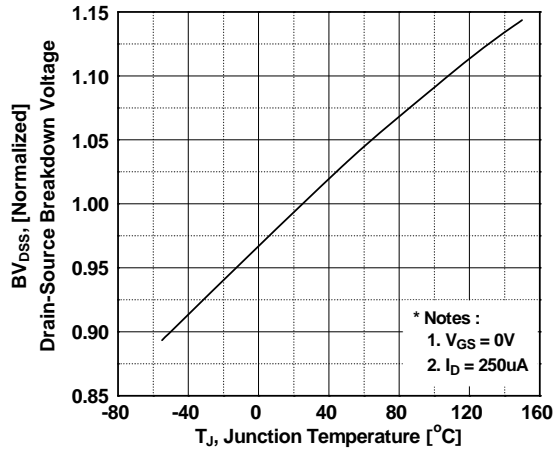


Figure 8. On-Resistance Variation vs. Temperature

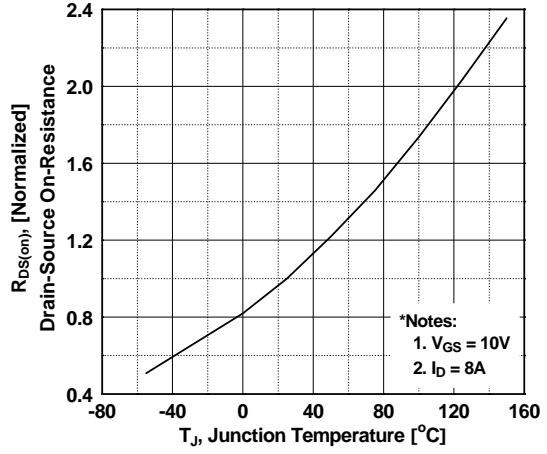


Figure 9. Maximum Safe Operating Area

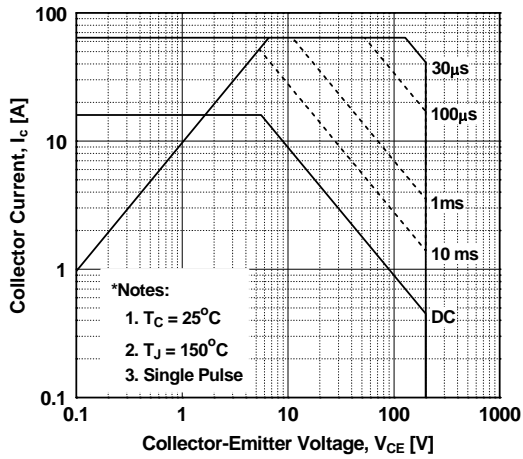


Figure 10. Maximum Drain Current vs. Case Temperature

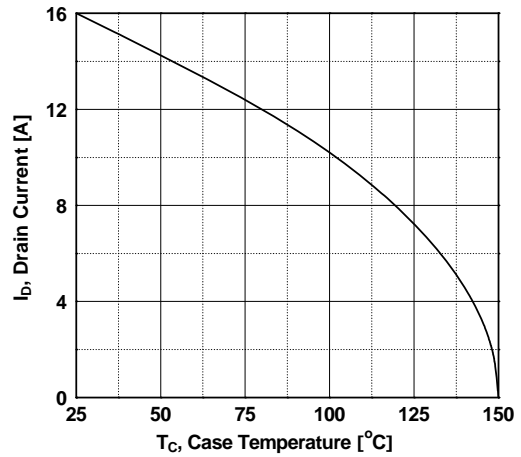
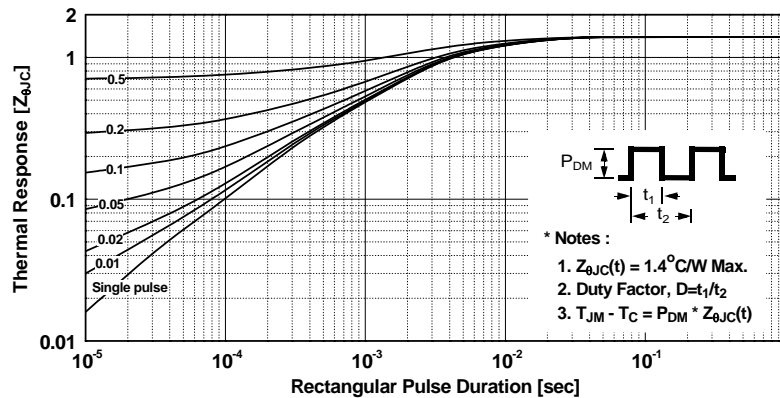
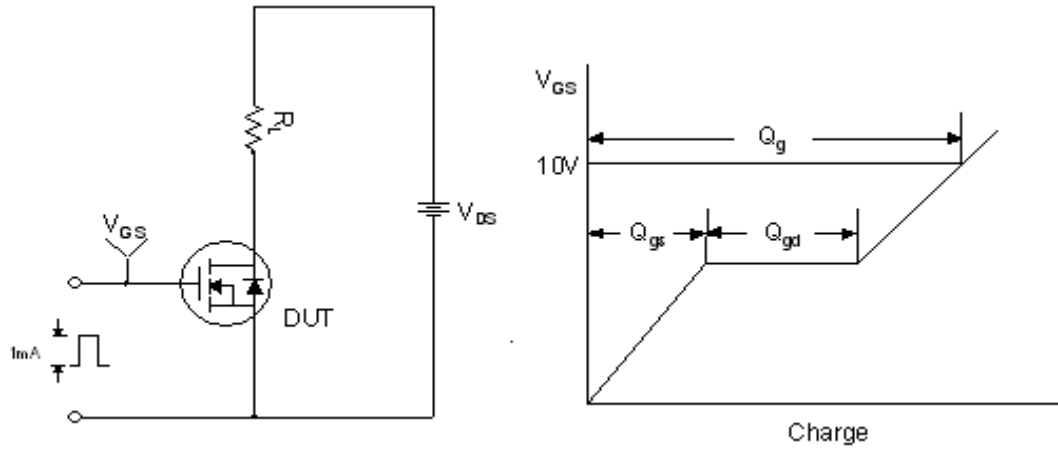


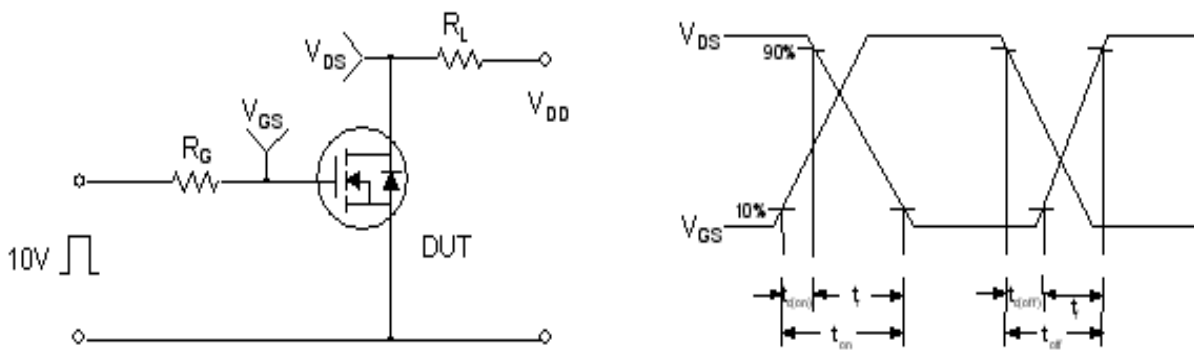
Figure 11. Transient Thermal Response Curve



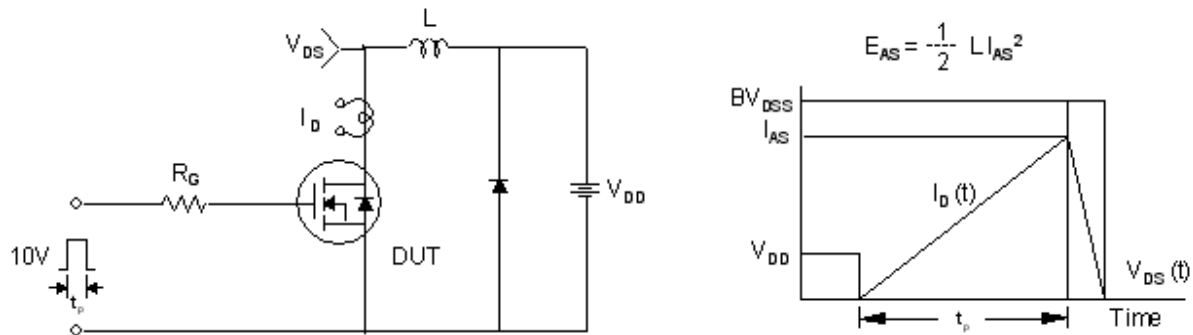
Gate Charge Test Circuit & Waveform



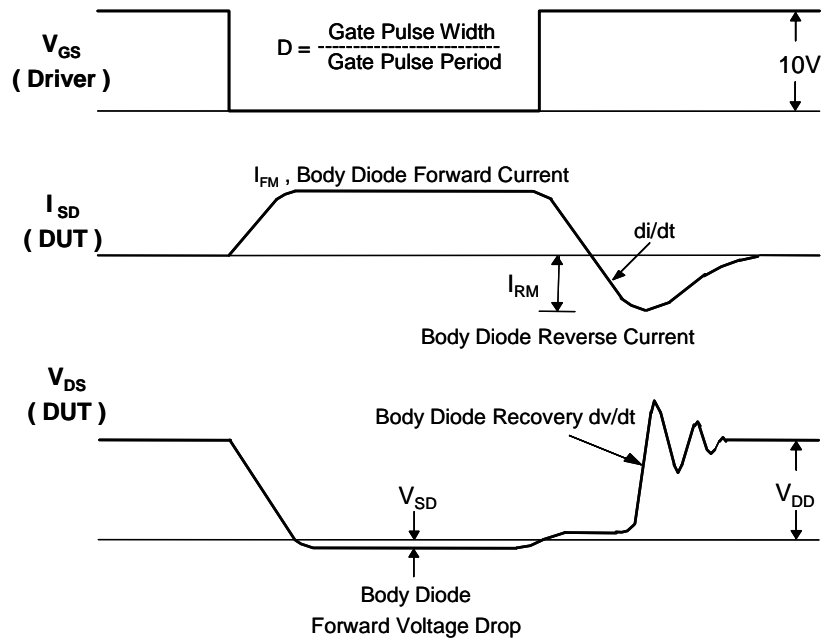
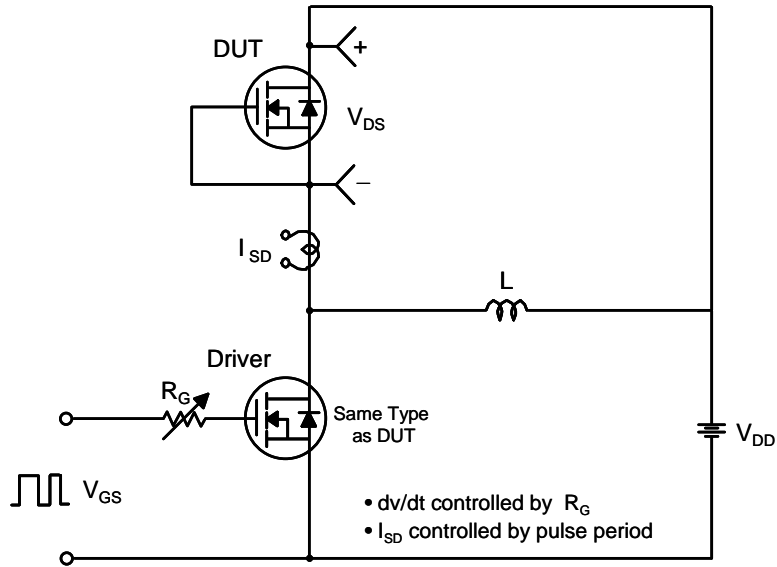
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

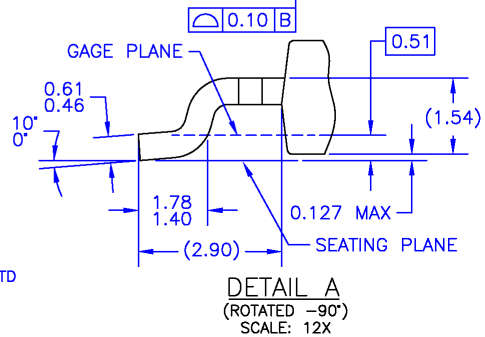
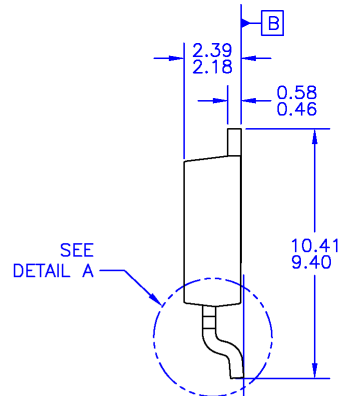
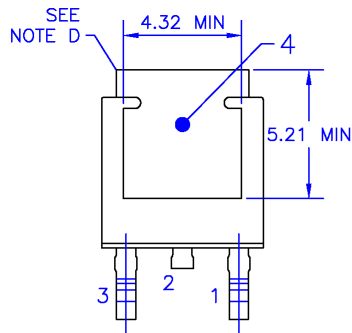
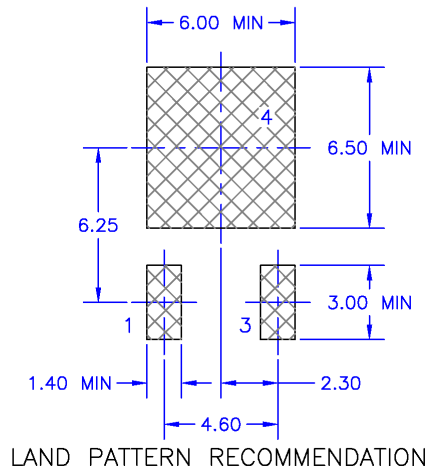
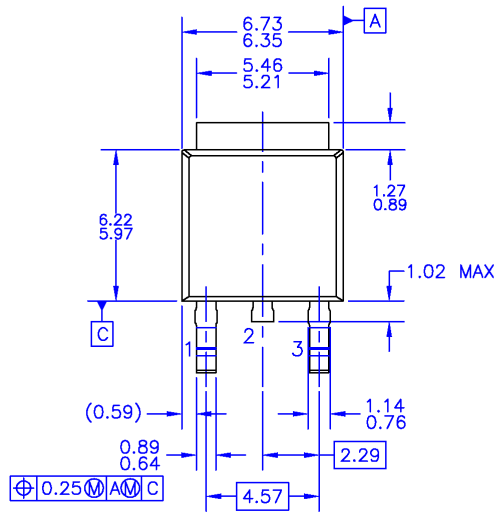


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D-PAK




- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
 - H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV8

Dimensions in Millimeters



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| AccuPower™ | F-PFST™ | PowerXS™ | SYSTEM GENERAL®* |
| AX-CAP®* | FRFET® | Programmable Active Droop™ | TinyBoost™ |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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