FAIRCHILD SEMICONDUCTOR®

June 2011

FDMS7608S

Dual N-Channel PowerTrench® MOSFET
Q1: 30 V, 22 A, 10.0 mΩ Q2: 30 V, 30 A, 6.3 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 10.0 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 13.6 mΩ at V_{GS} = 4.5 V, I_D = 10 A

Q2: N-Channel

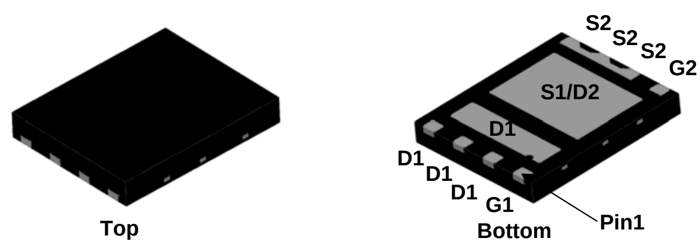
- Max $r_{DS(on)}$ = 6.3 mΩ at V_{GS} = 10 V, I_D = 15 A
- Max $r_{DS(on)}$ = 7.2 mΩ at V_{GS} = 4.5 V, I_D = 13 A
- RoHS Compliant

General Description

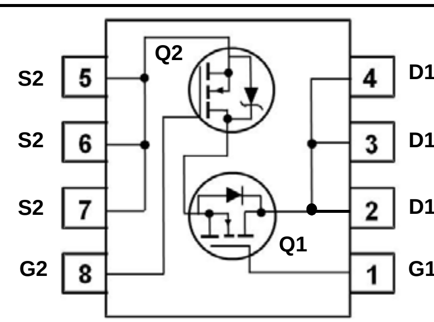
This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE



Power 56



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C	22	30	A
	-Continuous (Silicon limited)	T_C = 25 °C	46	60	
	-Continuous	T_A = 25 °C	12[1a]	15[1b]	
	-Pulsed		50	60	
E_{AS}	Single Pulse Avalanche Energy	(Note 4)	29	33	mJ
P_D	Power Dissipation for Single Operation	T_A = 25°C	2.2[1a]	2.5[1b]	W
	Power Dissipation for Single Operation	T_A = 25°C	1.0[1c]	1.0[1d]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57[1a]	50[1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125[1c]	120[1d]	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.0	3.2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7608S	FDMS7608S	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		13 19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2			1 500	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V	Q1 Q2			100 100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 µA $V_{GS} = V_{DS}$, I_D = 1 mA	Q1 Q2	1.2 1.2	1.9 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2		-6 -4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 12 A, T_J = 125°C	Q1		7.4 10.0 10.3	10.0 13.6 13.9	mΩ
		V_{GS} = 10 V, I_D = 15 A V_{GS} = 4.5 V, I_D = 13 A V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	Q2		4.8 6.0 6.6	6.3 7.2 8.6	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 12 A V_{DD} = 5 V, I_D = 15 A	Q1 Q2		54 76		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1135 1380	1510 1835	pF
C_{oss}	Output Capacitance		Q1 Q2		390 478	520 635	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		42 60	65 90	pF
R_g	Gate Resistance		Q1 Q2	0.2 0.2	1.6 0.5	3.2 2.0	Ω

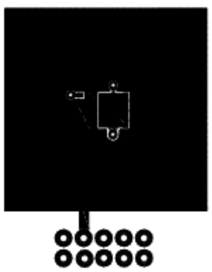
Switching Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 12 A, R_{GEN} = 6 Ω Q2 V_{DD} = 15 V, I_D = 15 A, R_{GEN} = 6 Ω	Q1 Q2		7 7	14 14	ns
t_r	Rise Time		Q1 Q2		3 3	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		19 20	35 36	ns
t_f	Fall Time		Q1 Q2		3 2	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 10 V; Q1: V_{DD} = 15 V, I_D = 12 A; Q2: V_{DD} = 15 V, I_D = 15 A	Q1 Q2		18 21	24 30	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 5 V; Q1: V_{DD} = 15 V, I_D = 12 A; Q2: V_{DD} = 15 V, I_D = 15 A	Q1 Q2		9 12	14 16	nC
Q_{gs}	Gate to Source Charge	Q1: V_{DD} = 15 V, I_D = 12 A; Q2: V_{DD} = 15 V, I_D = 15 A	Q1 Q2		3.6 3.5		nC
Q_{gd}	Gate to Drain "Miller" Charge	Q1: V_{DD} = 15 V, I_D = 12 A; Q2: V_{DD} = 15 V, I_D = 15 A	Q1 Q2		2.5 3.0		nC

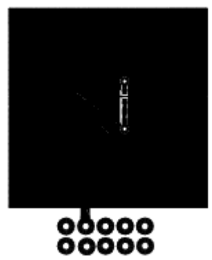
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)	Q1		0.75	1.1	V
		V_{GS} = 0 V, I_S = 12 A (Note 2)	Q1		0.84	1.2	
		V_{GS} = 0 V, I_S = 2 A (Note 2)	Q2		0.63	0.8	
		V_{GS} = 0 V, I_S = 15 A (Note 2)	Q2		0.80	1.2	
t_{rr}	Reverse Recovery Time	Q1 I_F = 12 A, di/dt = 100 A/μs	Q1		25	40	ns
			Q2		21	34	
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 15 A, di/dt = 300 A/μs	Q1		9	18	nC
			Q2		19	33	

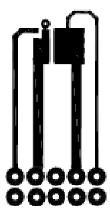
Notes:
1.$R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



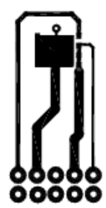
a. 57 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4. Q1: E_{AS} of 29 mJ is based on starting T_J = 25 °C; N-ch: L = 0.3 mH, I_{AS} = 14 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 3.75 A.

   Q2: E_{AS} of 33 mJ is based on starting T_J = 25 °C; N-ch: L = 0.3 mH, I_{AS} = 15 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% tested at L = 3 mH, I_{AS} = 3.9 A.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

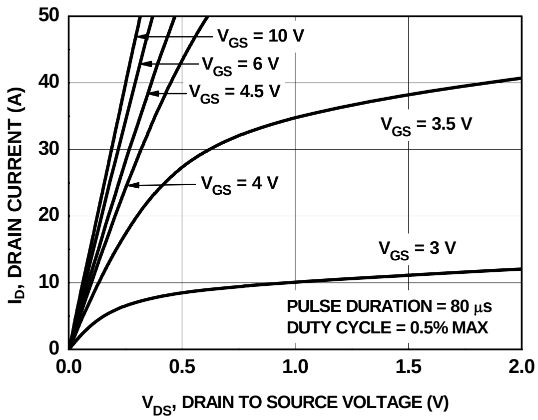


Figure 1. On Region Characteristics

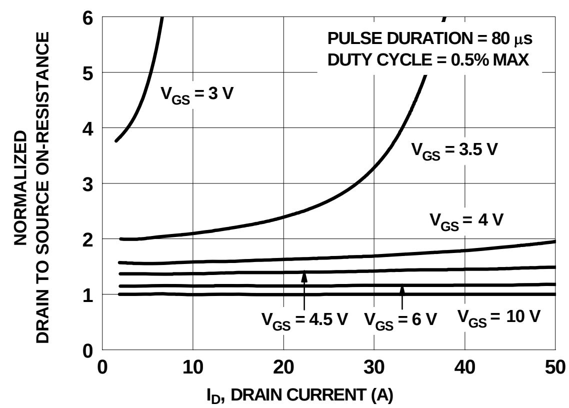


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

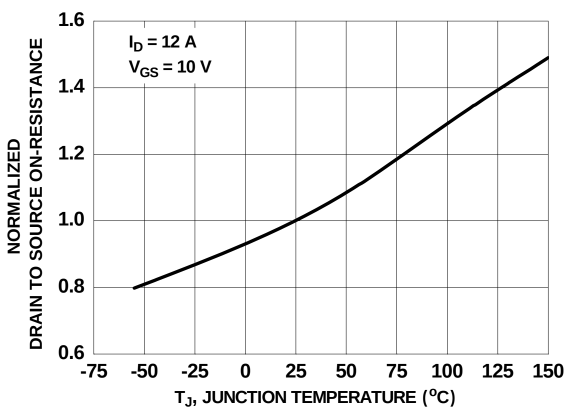


Figure 3. Normalized On Resistance vs Junction Temperature

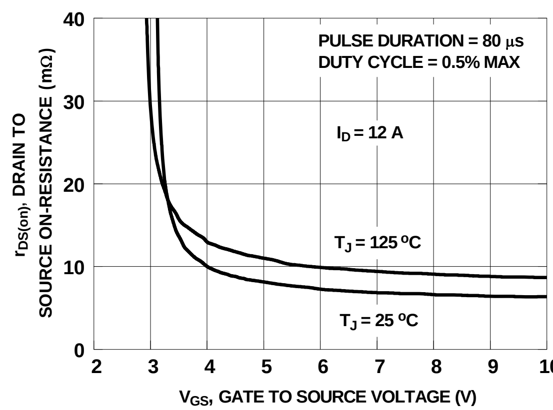


Figure 4. On-Resistance vs Gate to Source Voltage

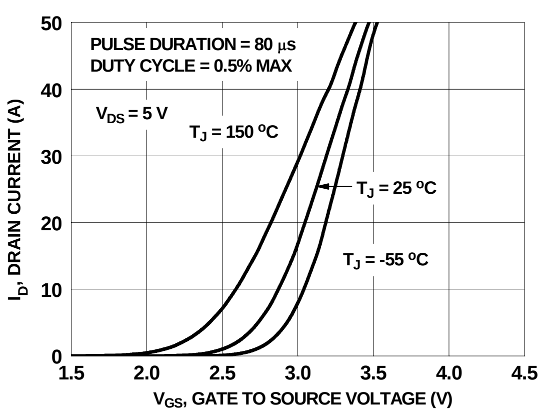


Figure 5. Transfer Characteristics

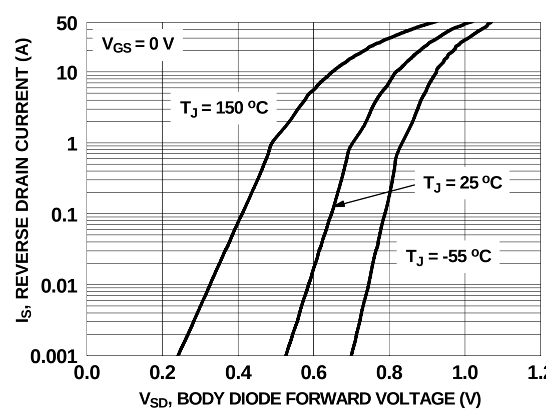


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

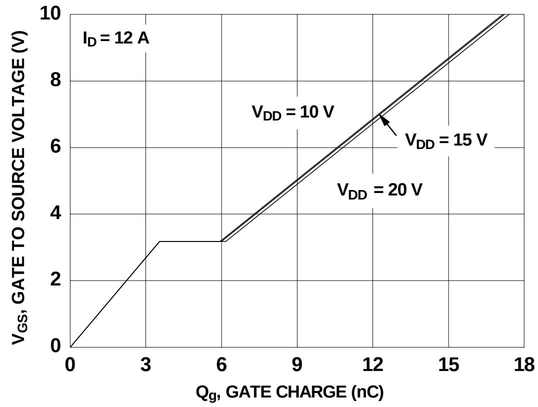


Figure 7. Gate Charge Characteristics

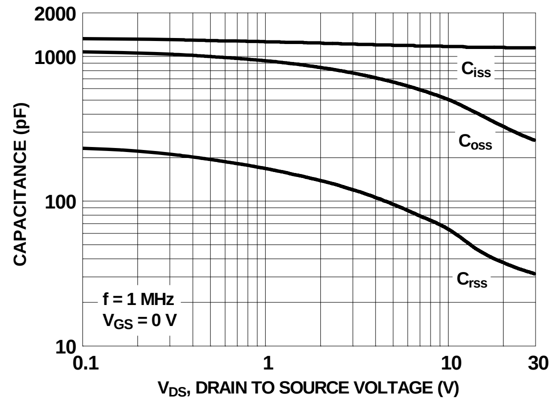


Figure 8. Capacitance vs Drain to Source Voltage

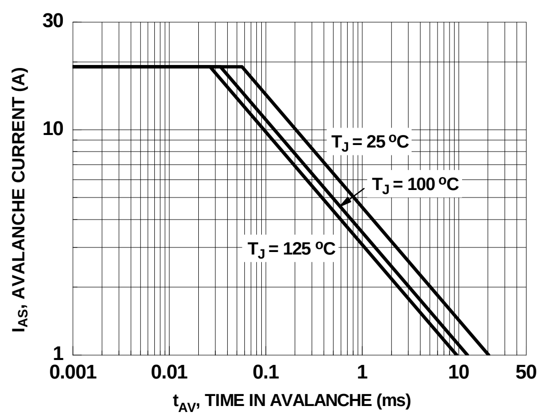


Figure 9. Unclamped Inductive Switching Capability

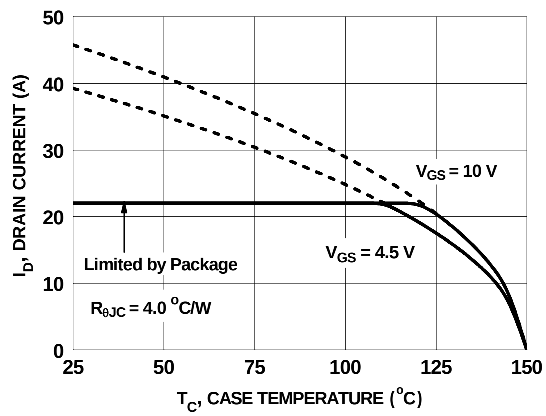


Figure 10. Maximum Continuous Drain Current vs Case Temperature

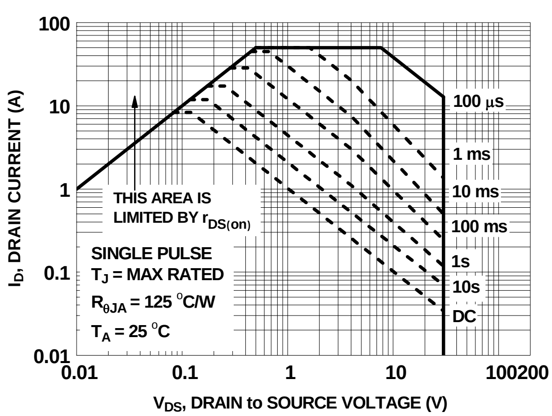


Figure 11. Forward Bias Safe Operating Area

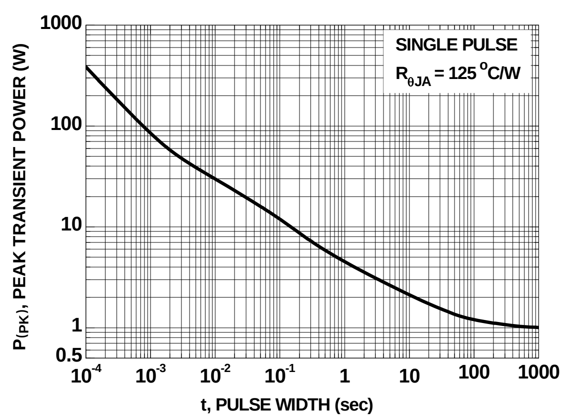


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

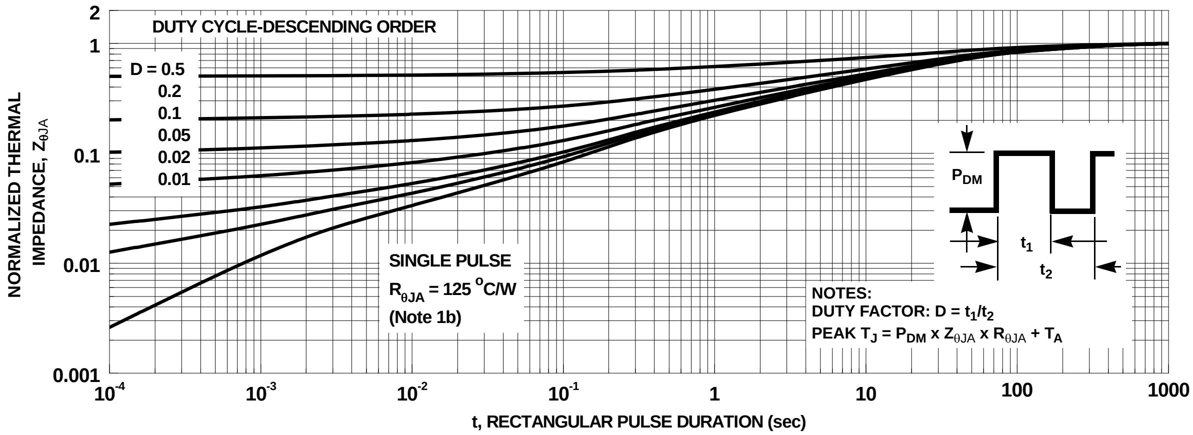


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

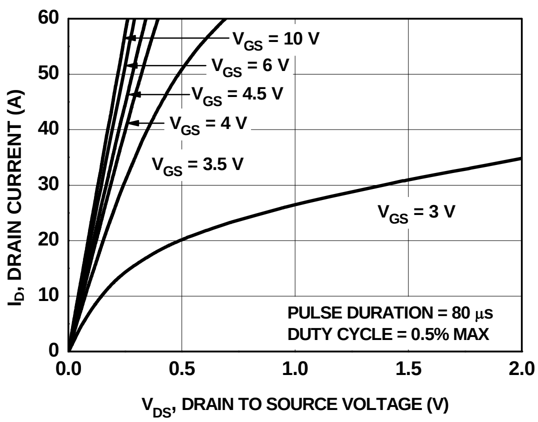


Figure 14. On-Region Characteristics

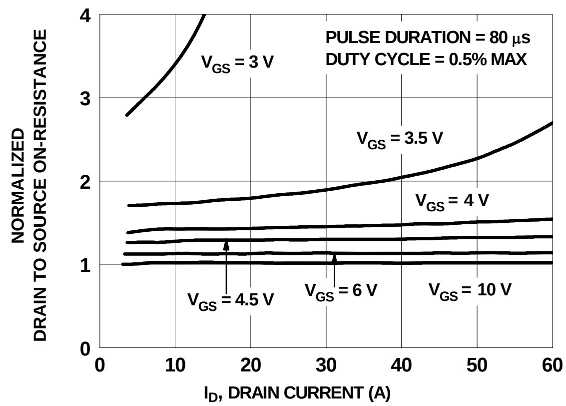


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

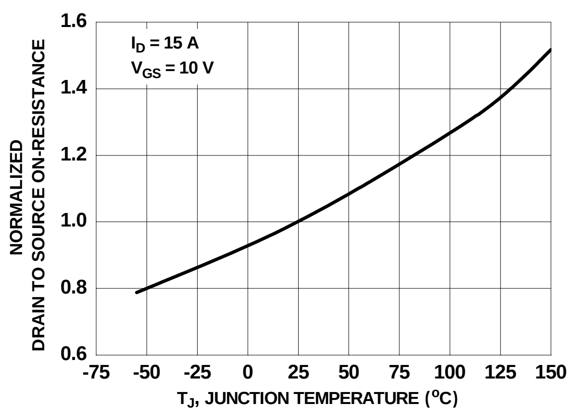


Figure 16. Normalized On-Resistance vs Junction Temperature

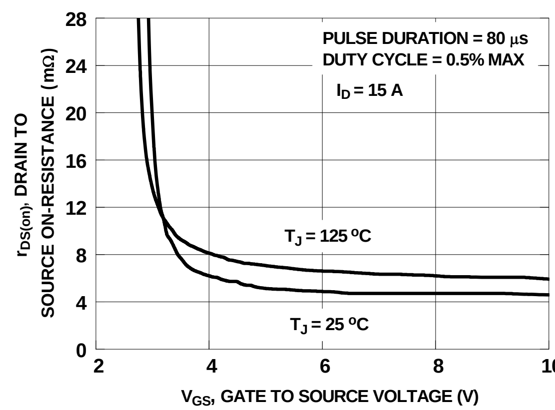


Figure 17. On-Resistance vs Gate to Source Voltage

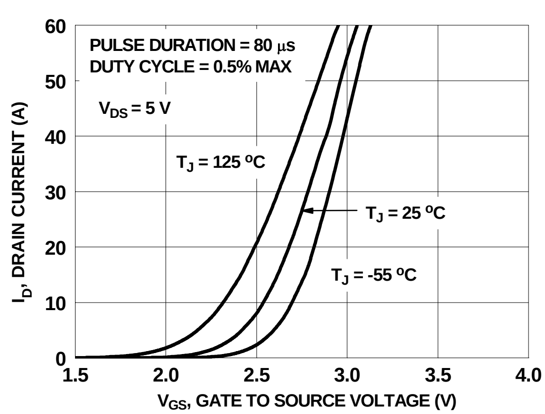


Figure 18. Transfer Characteristics

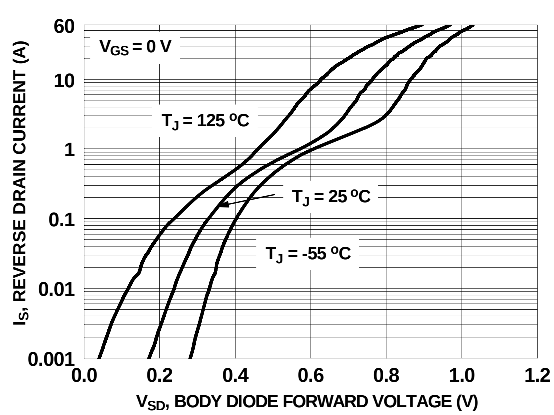


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) T_J = 25°C unless otherwise noted

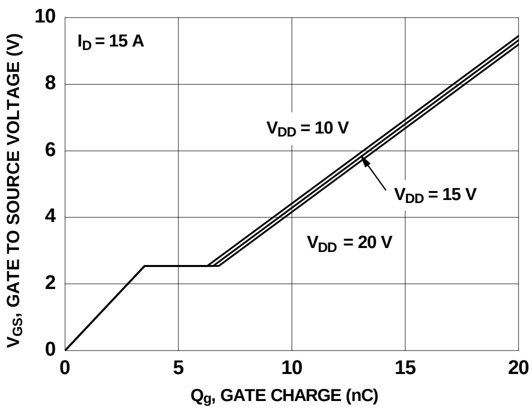


Figure 20. Gate Charge Characteristics

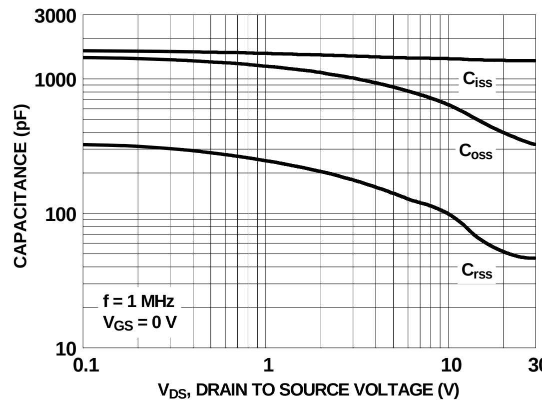


Figure 21. Capacitance vs Drain to Source Voltage

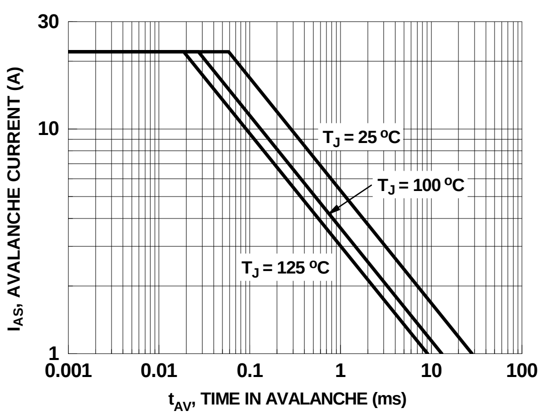


Figure 22. Unclamped Inductive Switching Capability

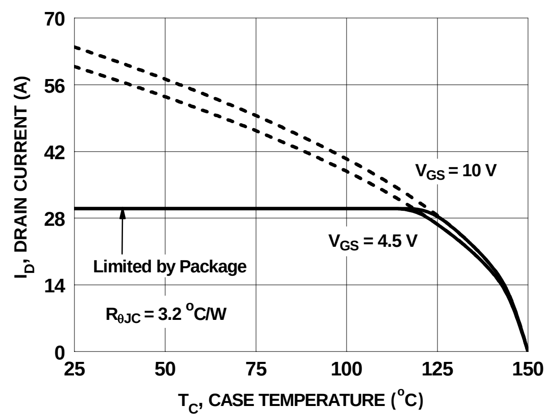


Figure 23. Maximum Continuous Drain Current vs Case Temperature

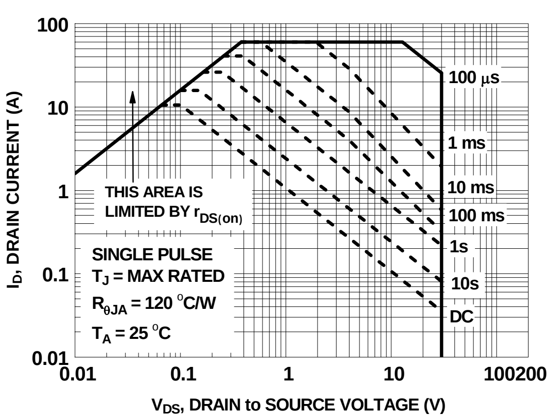


Figure 24. Forward Bias Safe Operating Area

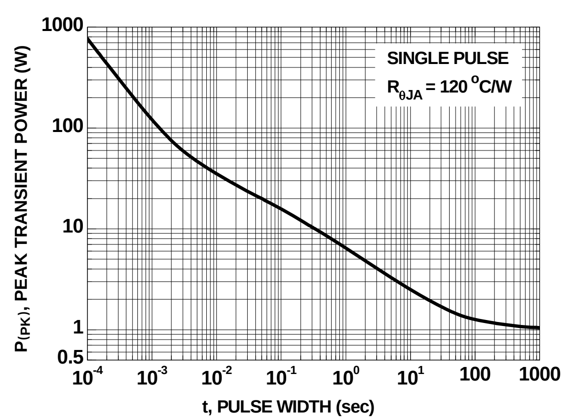


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

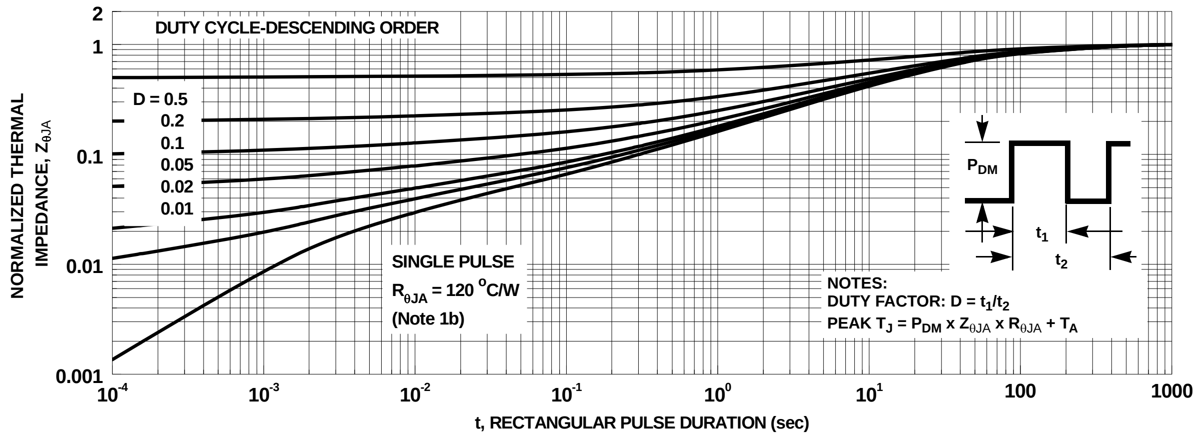


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS7608S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

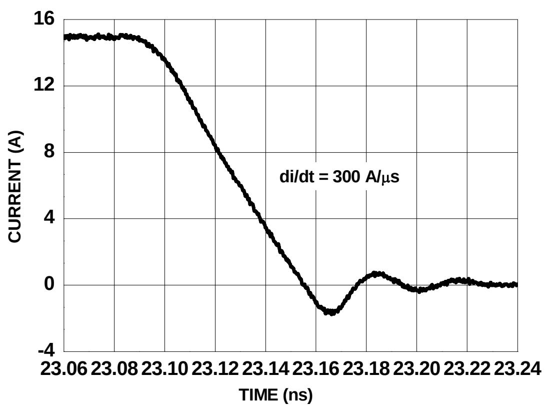


Figure 27. FDMS7608S SyncFET body diode reverse recovery characteristic

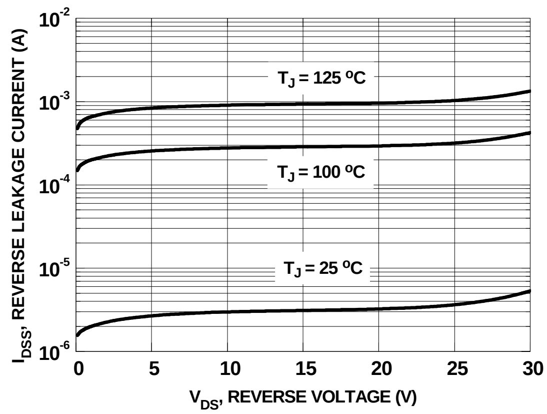
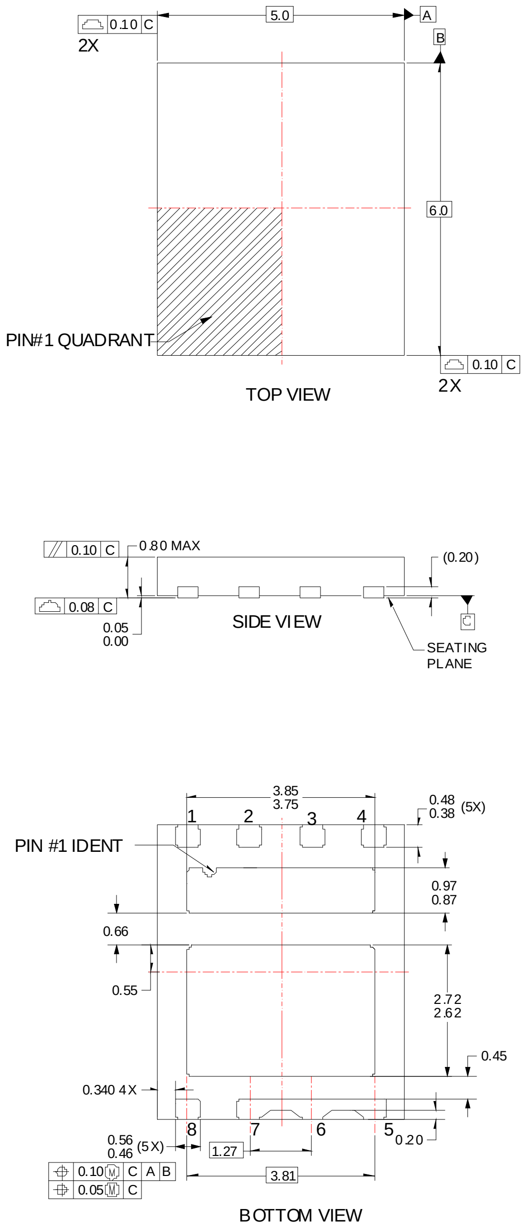
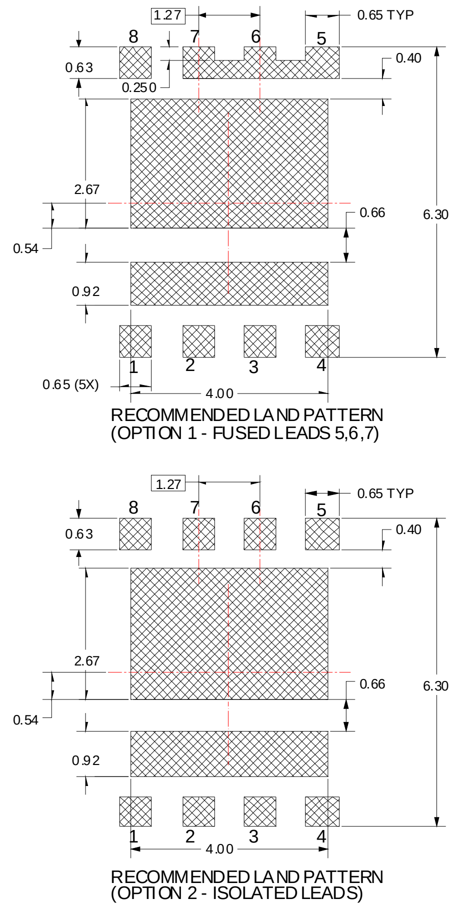


Figure 28. SyncFET body diode reverse leakage versus drain-source voltage

Dimensional Outline and Pad Layout





NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY

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MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
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OPTOLOGIC®
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PDP SPM™
Power-SPM™
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QS™
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RapidConfigure™
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SPM®
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SuperFET®
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SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
The Power Franchise®
The Right Technology for Your Success™
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
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PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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