



FDP12N60NZ / FDPF12N60NZ

N-Channel UniFET™ II MOSFET

600 V, 12 A, 650 mΩ

Features

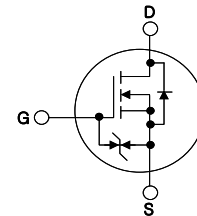
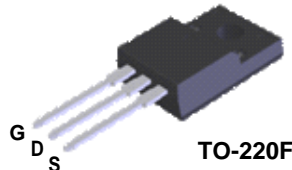
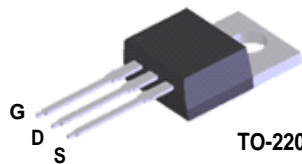
- $R_{DS(on)} = 530 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$
- Low Gate Charge (Typ. 26 nC)
- Low C_{rss} (Typ. 12 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Description

UniFET™ II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDP12N60NZ	FDPF12N60NZ	Unit	
V_{DSS}	Drain to Source Voltage	600		V	
V_{GSS}	Gate to Source Voltage	±30		V	
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	12	12*	A
		- Continuous ($T_C = 100^\circ\text{C}$)	7.2	7.2*	
I_{DM}	Drain Current	- Pulsed (Note 1)	48	48*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	565		mJ	
I_{AR}	Avalanche Current (Note 1)	12		A	
E_{AR}	Repetitive Avalanche Energy (Note 1)	24		mJ	
dv/dt	MOSFET dv/dt Ruggedness	20		V/ns	
	Peak Diode Recovery dv/dt (Note 3)	10		V/ns	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	240	39	W
		- Derate above 25°C	2.0	0.3	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$	
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$	

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP12N60NZ	FDPF12N60NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.52	3.2	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP12N60NZ	FDP12N60NZ	TO-220	-	-	50
FDPF12N60NZ	FDPF12N60NZ	TO-220F	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.6	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 480\text{V}, T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 6\text{A}$	-	0.53	0.65	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 6\text{A}$	-	13.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1260	1676	pF
C_{oss}	Output Capacitance		-	150	200	pF
C_{rss}	Reverse Transfer Capacitance		-	12	18	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\text{V}, I_D = 12\text{A}$ $V_{GS} = 10\text{V}$	-	26	34	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	10	-	nC

(Note 4)

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{V}, I_D = 12\text{A}$ $R_G = 25\Omega$	-	25	60	ns
t_r	Turn-On Rise Time		-	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		-	80	170	ns
t_f	Turn-Off Fall Time		-	60	130	ns

(Note 4)

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	12	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	48	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 12\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 12\text{A}$	-	350	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	2.2	-	μC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 7.85\text{mH}, I_{AS} = 12\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 12\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

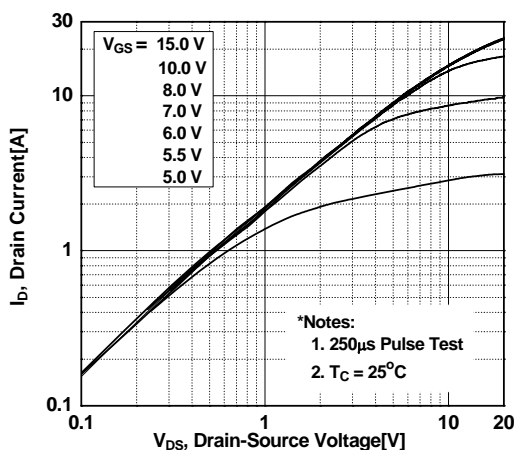


Figure 2. Transfer Characteristics

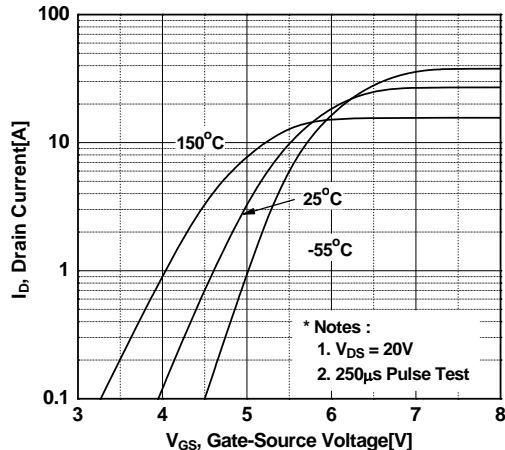


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

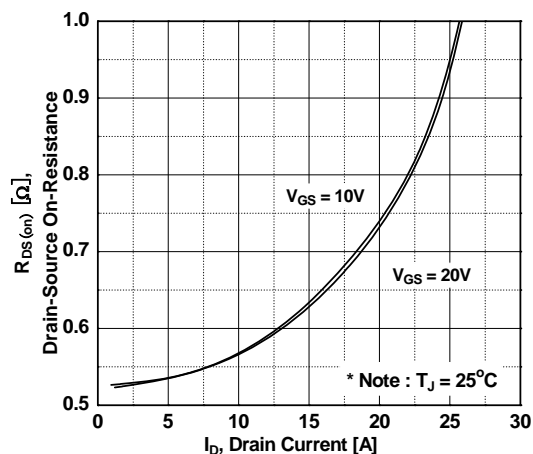


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

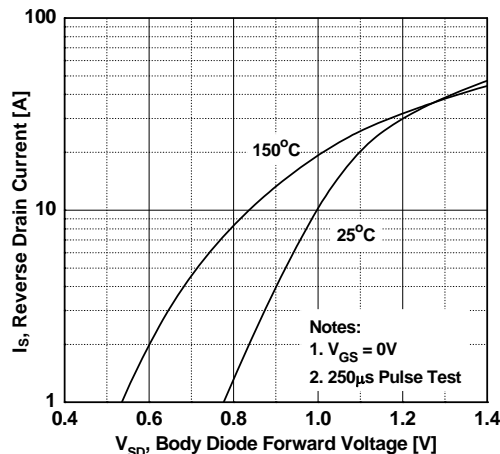


Figure 5. Capacitance Characteristics

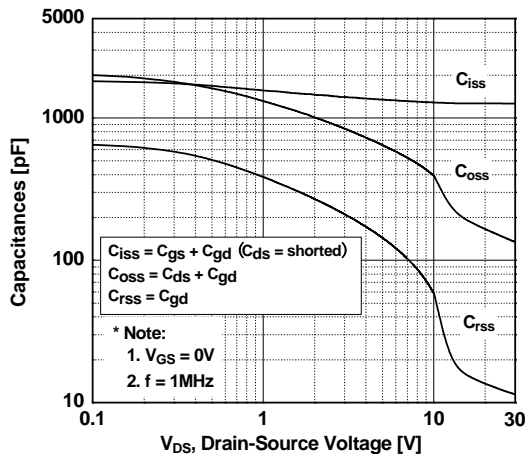
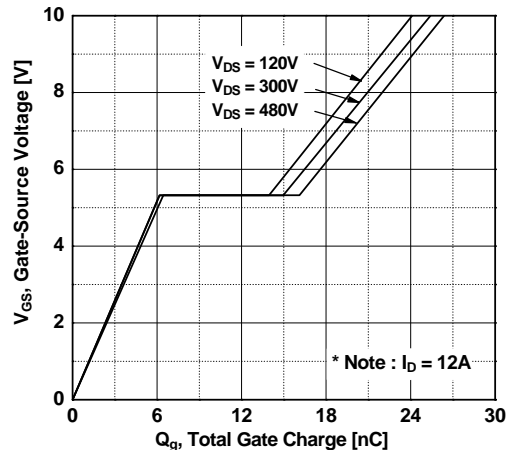


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

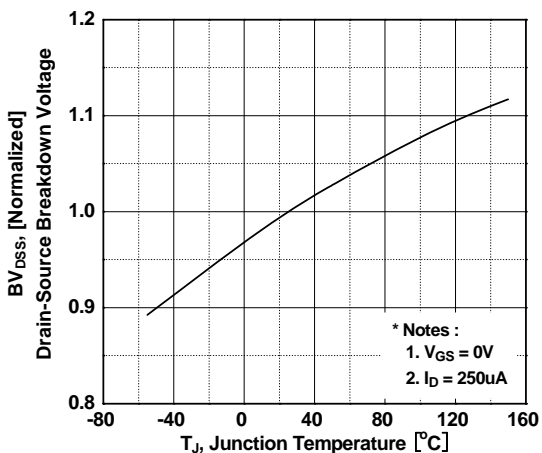


Figure 8. On-Resistance Variation vs Temperature

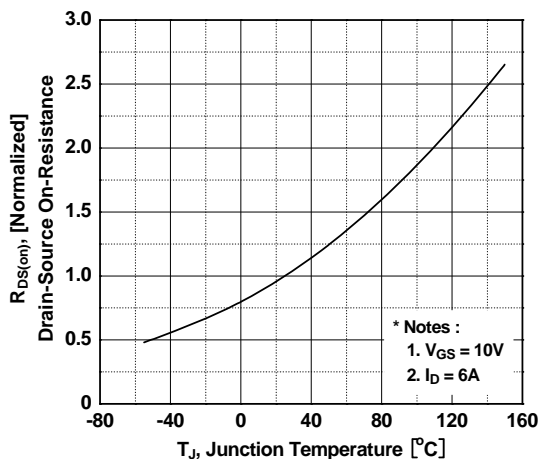


Figure 9. Maximum Safe Operating Area -FDPF12N60NZ

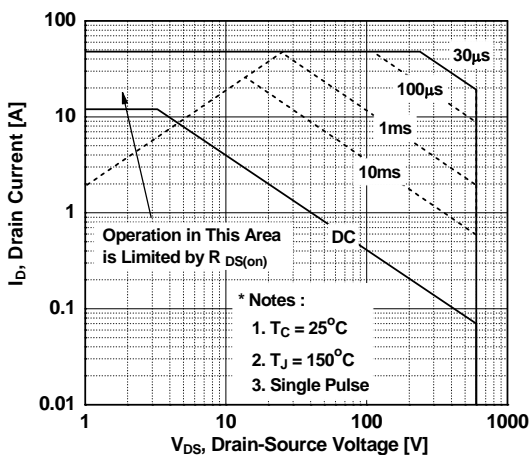


Figure 10. Maximum Safe Operating Area -FDP12N60NZ

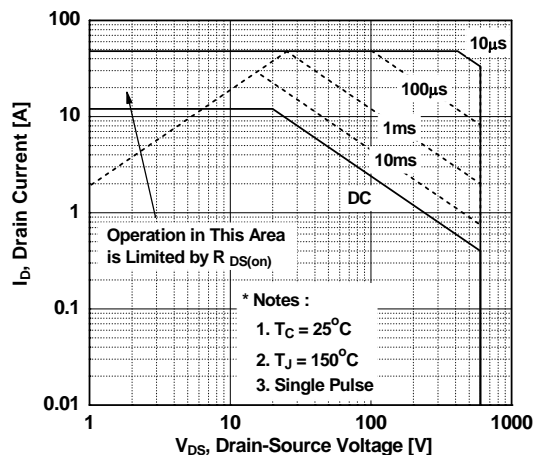


Figure 11. Maximum Drain Current vs Case Temperature

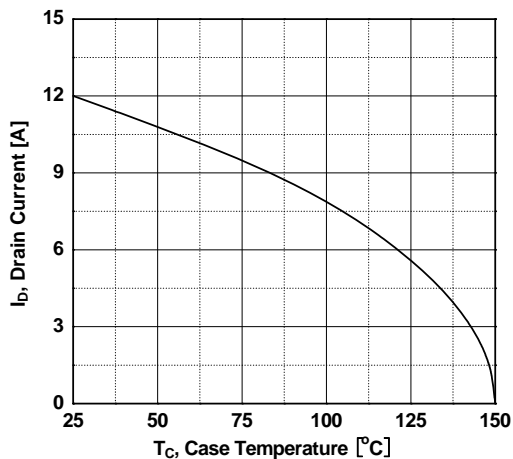


Figure 12. Transient Thermal Response Curve
-FDPF12N60NZ

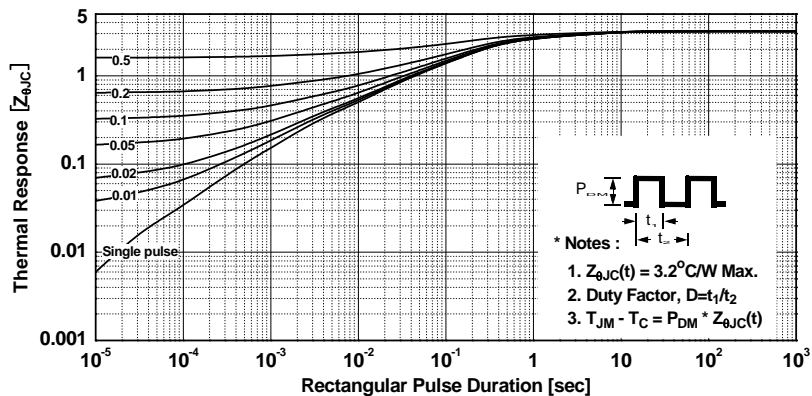
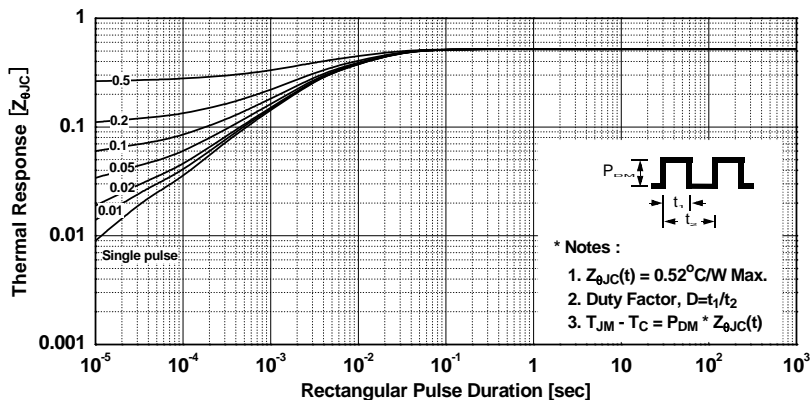
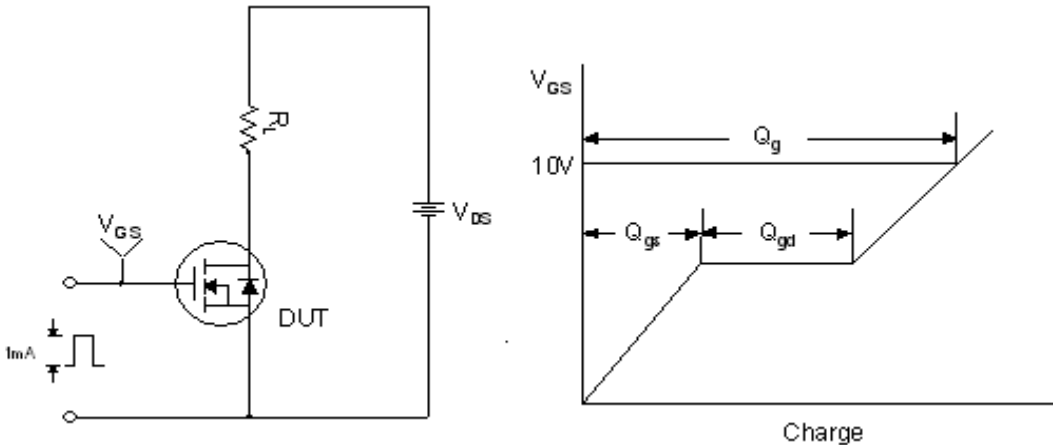


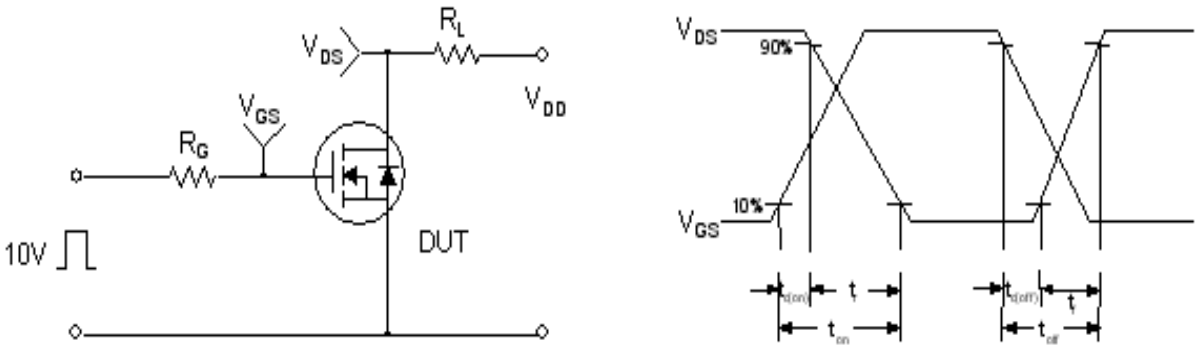
Figure 13. Transient Thermal Response Curve
-FDP12N60NZ



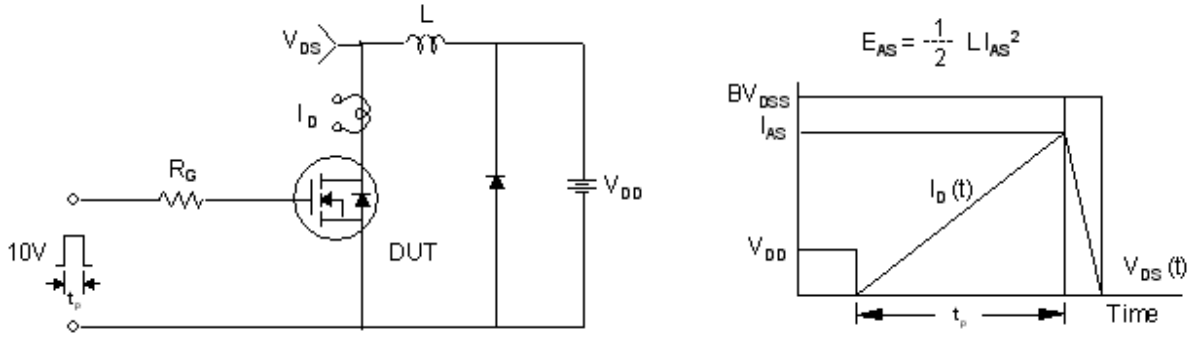
Gate Charge Test Circuit & Waveform



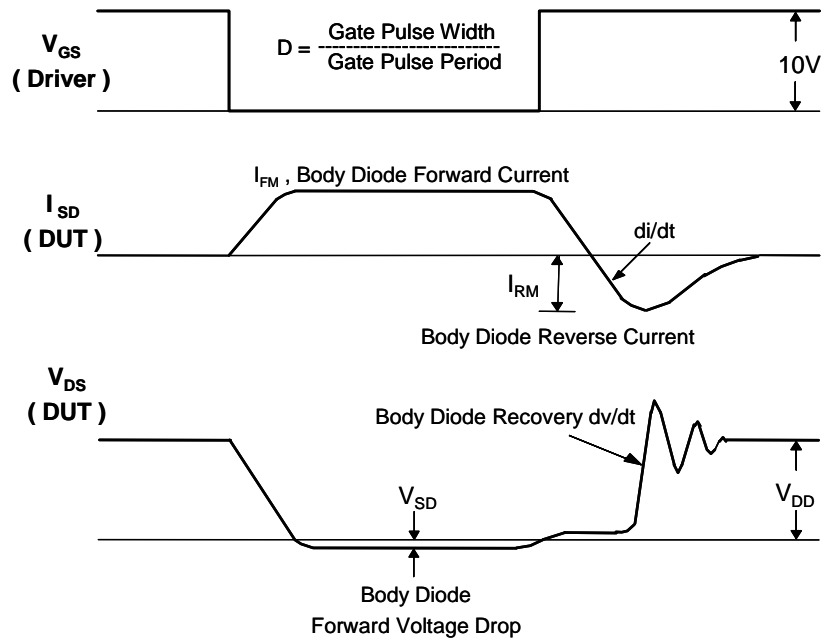
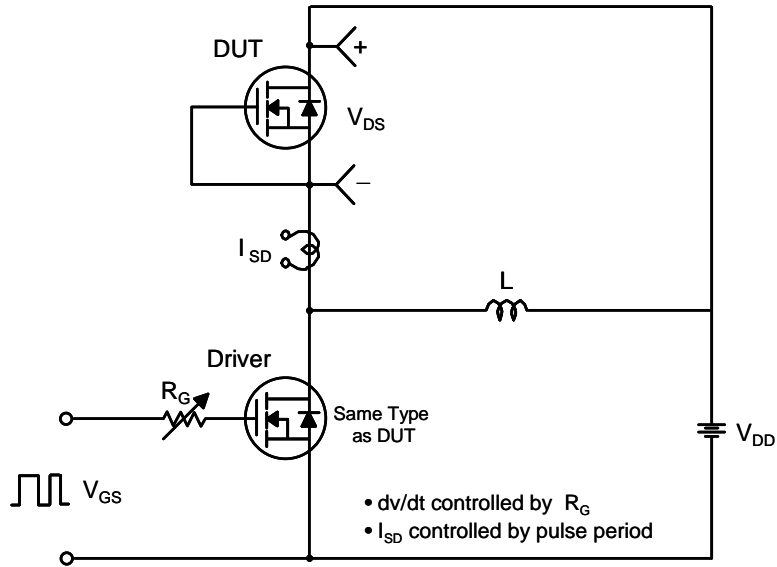
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

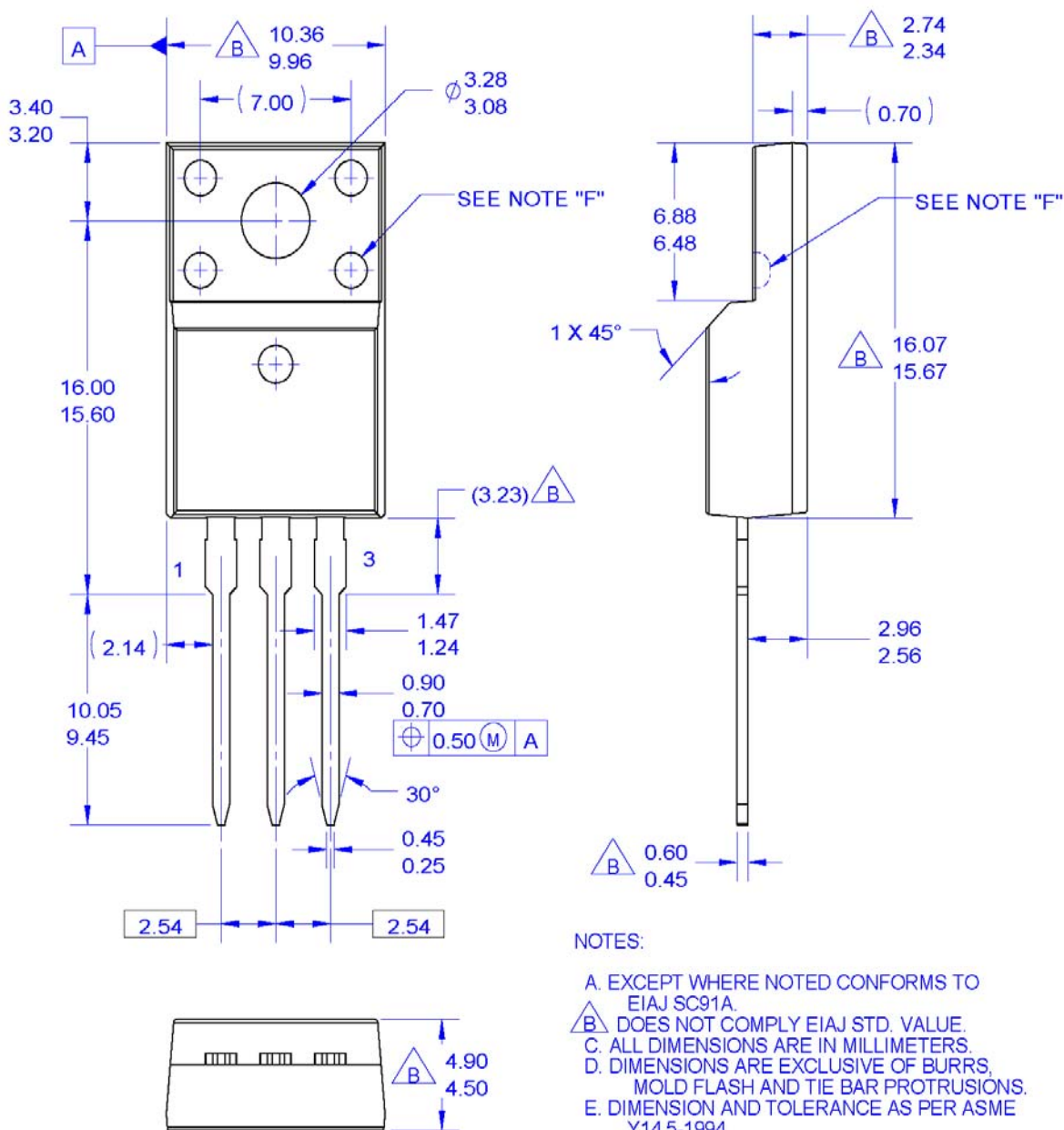


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions (Continued)

TO-220M03



NOTES:





- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- $\triangle B$ DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Dimensions in Millimeters



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| BitSiC™ | Global Power Resource SM | QFET® | TinyBuck™ |
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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