

FCD600N60Z

N-Channel SuperFET® II MOSFET

600 V, 7.4 A, 600 mΩ

Features

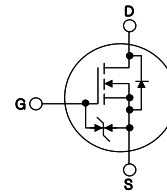
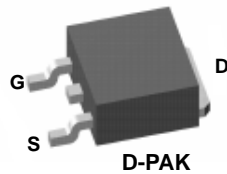
- 650 V @ $T_J = 150^\circ\text{C}$
- Max. $R_{DS(on)} = 600\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 20\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss,eff} = 74\text{ pF}$)
- 100% Avalanche Tested
- ESD Improved Capacity

Applications

- LCD / LED / PDP TV and Monitor Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FCD600N60Z	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate to Source Voltage	-DC	± 20
		-AC ($f > 1\text{ Hz}$)	± 30
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	7.4
		-Continuous ($T_C = 100^\circ\text{C}$)	4.7
I_{DM}	Drain Current - Pulsed (Note 1)	22.2	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	135	mJ
I_{AR}	Avalanche Current (Note 1)	1.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.89	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
	MOSFET dv/dt	100	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	89
		- Derate above 25°C	0.71
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCD600N60Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD600N60Z	FCD600N60Z	D-PAK	380 mm	16 mm	2500

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	650	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.67	-	$\text{V}/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 7.4\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}$	-	-	5	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	20	
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.7\text{ A}$	-	0.51	0.6	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 3.7\text{ A}$	-	6.7	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	840	1120	pF
C_{oss}	Output Capacitance		-	630	840	pF
C_{rss}	Reverse Transfer Capacitance		-	30	45	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	16.5	-	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	74	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 3.7\text{ A}$ $V_{GS} = 10\text{ V}$	-	20	26	nC
Q_{gs}	Gate to Source Gate Charge		-	3.4	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	7.5	-
ESR	Equivalent Series Resistance	Drain open	-	2.89	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 3.7\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 4.7\ \Omega$	-	13	36	ns
t_r	Turn-On Rise Time		-	7	24	ns
$t_{d(off)}$	Turn-Off Delay Time		-	39	88	ns
t_f	Turn-Off Fall Time		(Note 4)	-	9	28

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	7.4	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	22.2	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 3.7\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 3.7\text{ A}$	-	200	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	2.3	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 1.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3.7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

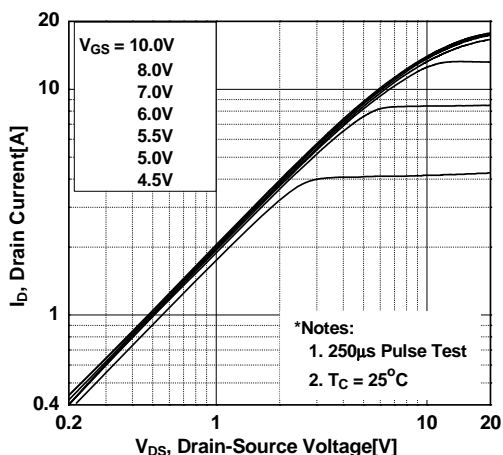


Figure 2. Transfer Characteristics

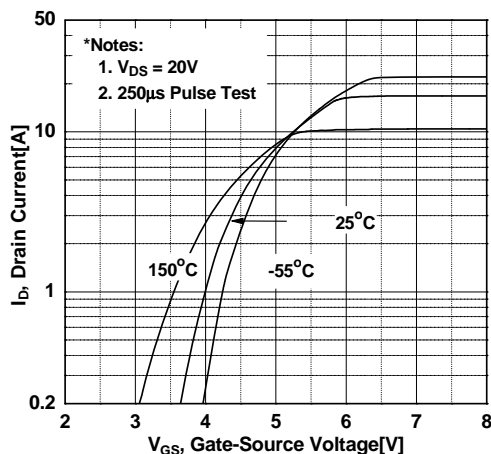


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

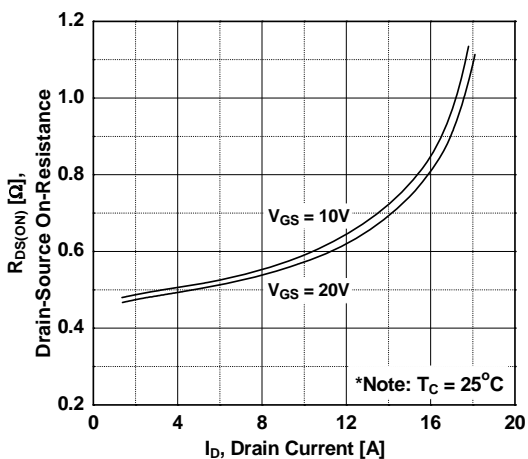


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

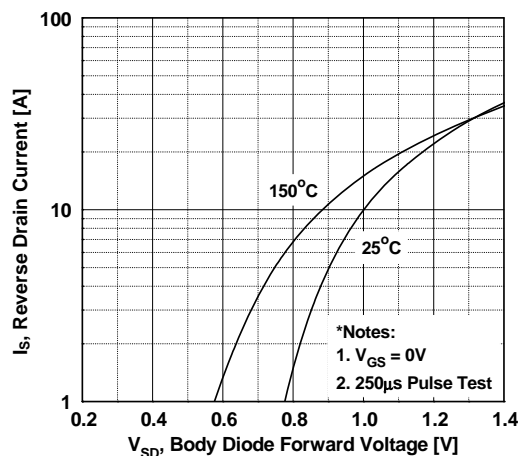


Figure 5. Capacitance Characteristics

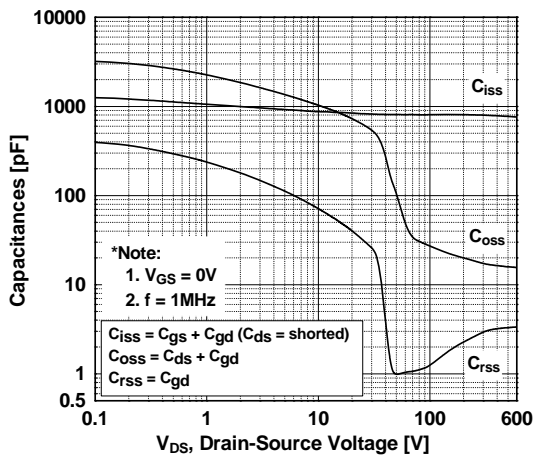
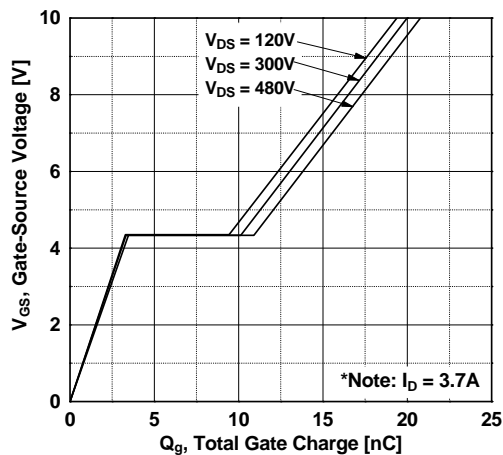


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

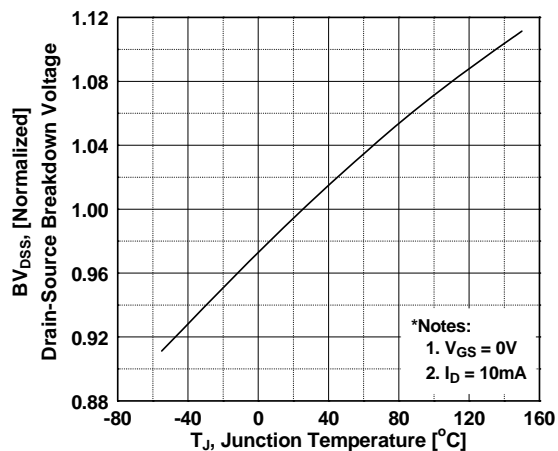


Figure 8. On-Resistance Variation vs. Temperature

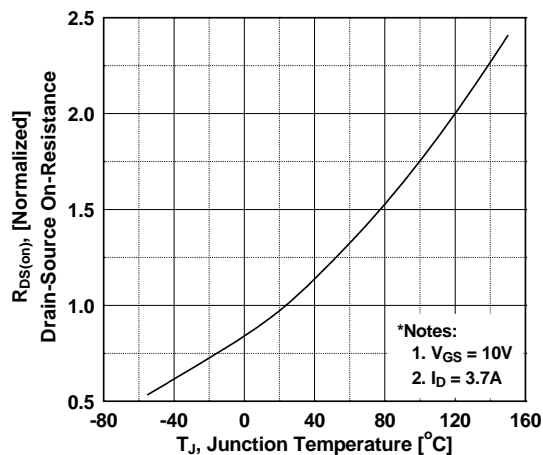


Figure 9. Maximum Safe Operating Area vs. Case Temperature

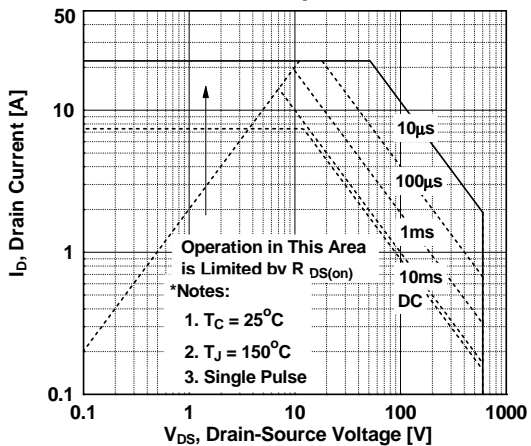


Figure 10. Maximum Drain Current

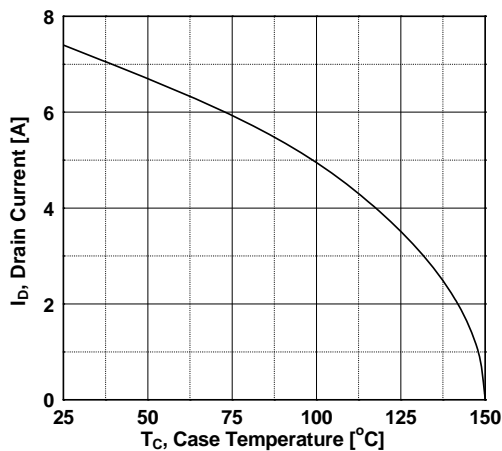
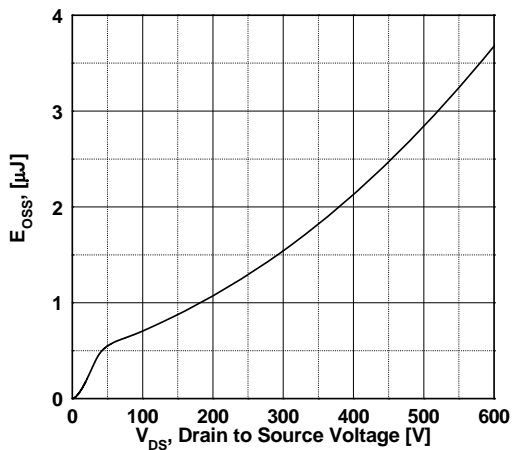
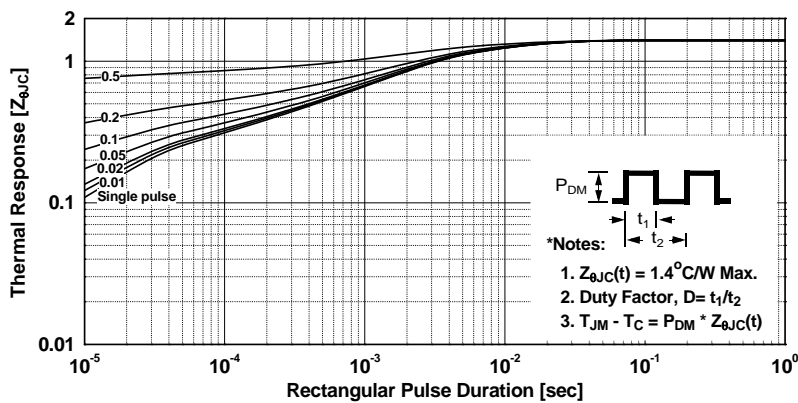


Figure 11. E_oss vs. Drain to Source Voltage

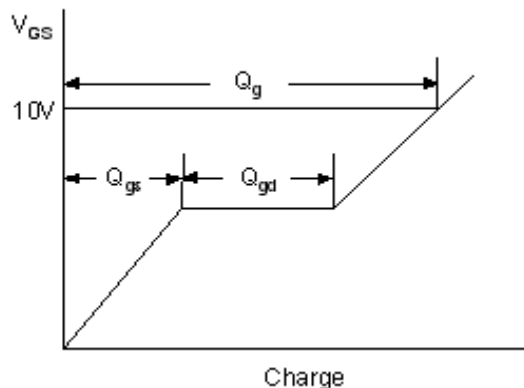
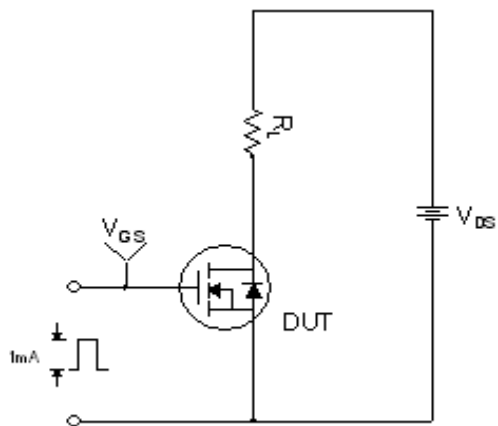


Typical Performance Characteristics (Continued)

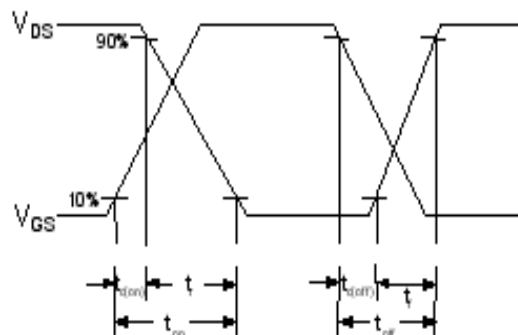
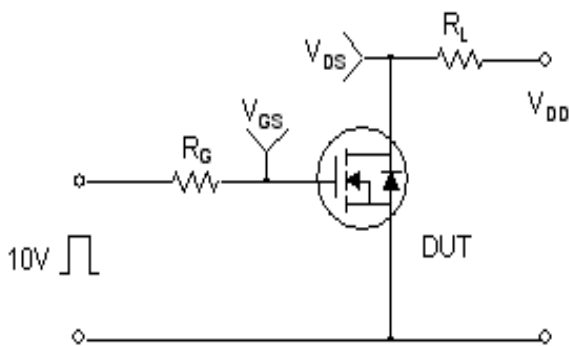
Figure 12. Transient Thermal Response Curve



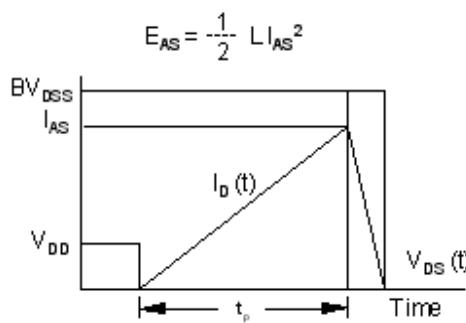
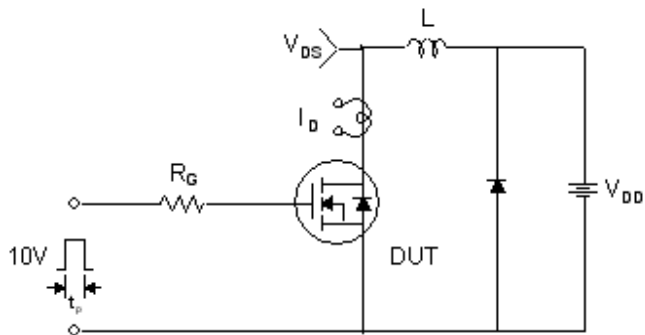
Gate Charge Test Circuit & Waveform



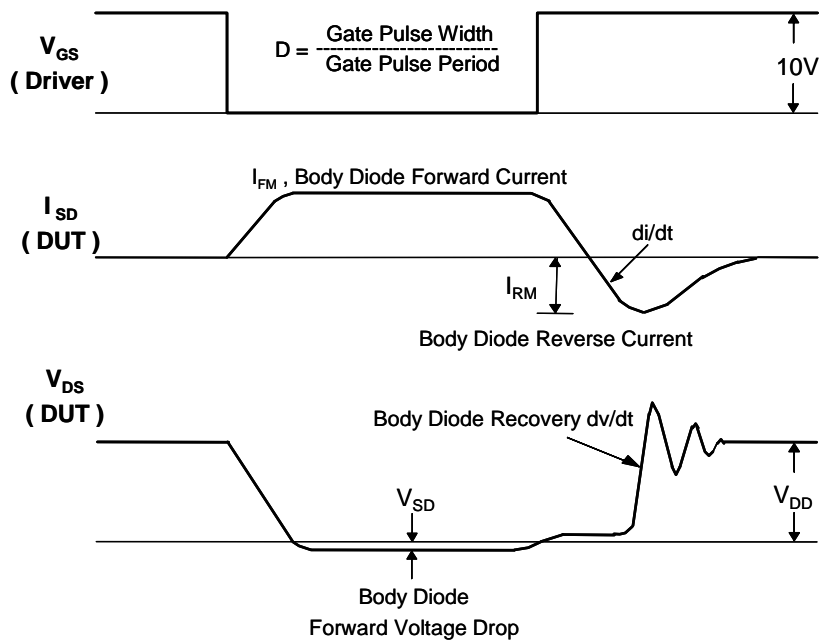
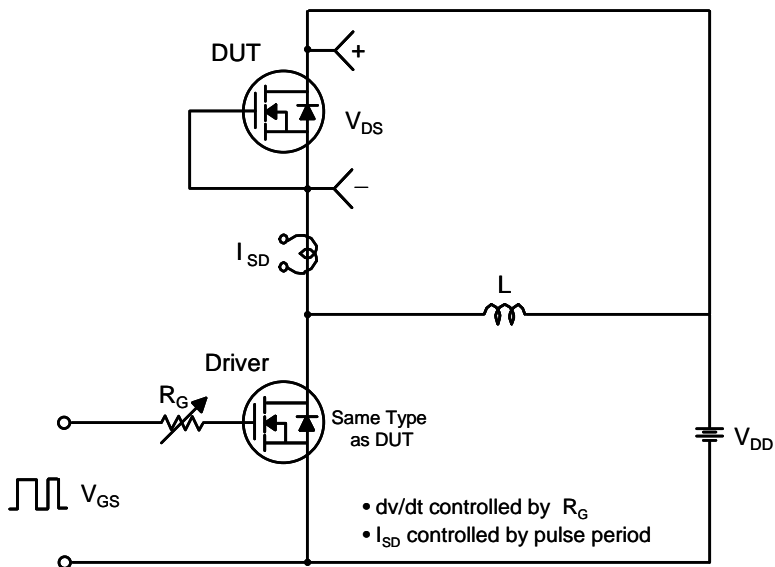
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

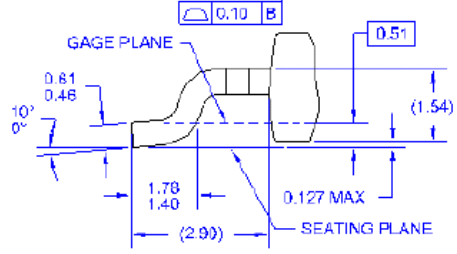
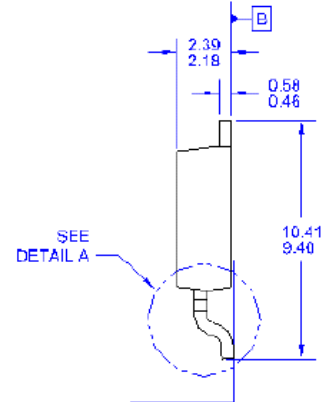
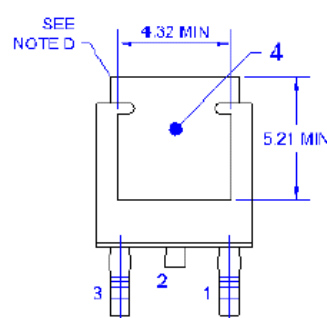
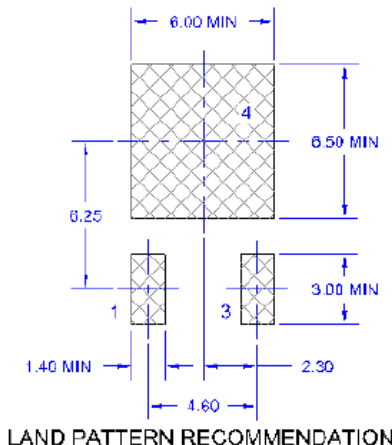
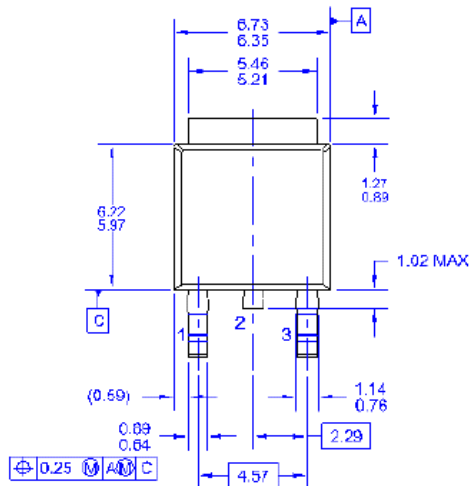


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D-PAK





- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003K235-3N.
 H) DRAWING NUMBER AND REVISION: WMT-T0252A03HEVB

Dimensions in Millimeters



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- | | | | |
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| AX-CAP®* | FRFET® | Programmable Active Droop™ | TinyBoost™ |
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| Build it Now™ | Green Bridge™ | QS™ | TinyCalc™ |
| CorePLUS™ | Green FPS™ | Quiet Series™ | TinyLogic® |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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