

74AHC1G07; 74AHCT1G07

Buffer with open-drain output

Rev. 06 — 7 June 2007

Product data sheet

1. General description

74AHC1G07 and 74AHCT1G07 are high-speed Si-gate CMOS devices. They provide a non-inverting buffer.

The output of these devices is open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH-level.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features

- High noise immunity
- Low power dissipation
- SOT353-1 and SOT753 package options
- ESD protection:
 - ◆ HBM JESD22-A114E: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101C: exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

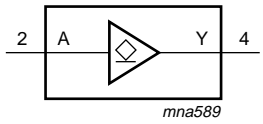
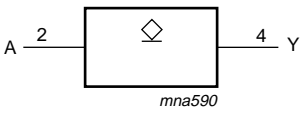
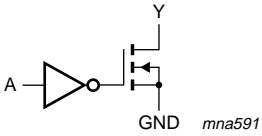
Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G07GW 74AHCT1G07GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G07GV 74AHCT1G07GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753

4. Marking

Table 2. Marking codes

Type number	Marking
74AHC1G07GW	AS
74AHC1G07GV	A07
74AHCT1G07GW	CS
74AHCT1G07GV	C07

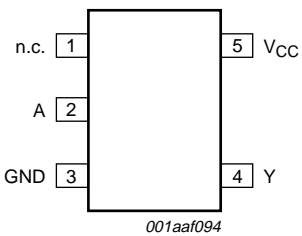
5. Functional diagram

 <p><i>mna589</i></p>	 <p><i>mna590</i></p>	 <p><i>mna591</i></p>
Fig 1. Logic symbol	Fig 2. IEC logic symbol	Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

74AHC1G07
74AHCT1G07



001aaf094

Fig 4. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
A	Y
L	L
H	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V	[1] -	±20	mA
I _O	output current	V _O > -0.5 V	-	±25	mA
V _O	output voltage	active mode	[1] -0.5	+7.0	V
		high-impedance mode	[1] -0.5	+7.0	V
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G07			74AHCT1G07			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage	active mode	0	-	V _{CC}	0	-	V _{CC}	V
		high-impedance mode	0	-	6.0	0	-	6.0	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC1G07										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25		±2.5		±10.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	20	μA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF
For type 74AHCT1G07										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.25		±2.5		±10.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f \leq 3.0\text{ ns}$. For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
For type 74AHC1G07										
t _{PZL}	OFF-state to LOW propagation delay	A to Y; see Figure 5								
		V _{CC} = 3.0 V to 3.6 V [1]								
		C _L = 15 pF	-	3.5	5.6	1.0	6.3	1.0	7.0	ns
		C _L = 50 pF	-	5.0	8.0	1.0	9.0	1.0	10.0	ns
		V _{CC} = 4.5 V to 5.5 V [2]								
		C _L = 15 pF	-	2.5	3.9	1.0	4.6	1.0	4.9	ns
		C _L = 50 pF	-	3.6	5.5	1.0	6.5	1.0	7.0	ns
t _{PLZ}	LOW to OFF-state propagation delay	A to Y; see Figure 5								
		V _{CC} = 3.0 V to 3.6 V [1]								
		C _L = 15 pF	-	5.8	7.9	1.0	8.4	1.0	8.9	ns
		C _L = 50 pF	-	8.3	11.5	1.0	12.0	1.0	12.5	ns
		V _{CC} = 4.5 V to 5.5 V [2]								
		C _L = 15 pF	-	4.2	5.1	1.0	5.6	1.0	6.1	ns
		C _L = 50 pF	-	6.0	7.5	1.0	8.0	1.0	8.5	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	5	-	-	-	-	-	pF
For type 74AHCT1G07										
t _{PZL}	OFF-state to LOW propagation delay	A to Y; see Figure 5								
		V _{CC} = 4.5 V to 5.5 V [2]								
		C _L = 15 pF	-	2.8	4.6	1.0	5.3	1.0	5.6	ns
		C _L = 50 pF	-	4.0	6.5	1.0	7.5	1.0	8.0	ns
t _{PLZ}	LOW to OFF-state propagation delay	A to Y; see Figure 5								
		V _{CC} = 4.5 V to 5.5 V [2]								
		C _L = 15 pF	-	3.9	5.6	1.0	6.1	1.0	6.6	ns
		C _L = 50 pF	-	5.5	8.0	1.0	8.5	1.0	9.0	ns
C _{PD}	power dissipation capacitance	per buffer; C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	6.5	-	-	-	-	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V.

[2] Typical values are measured at V_{CC} = 5.0 V.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

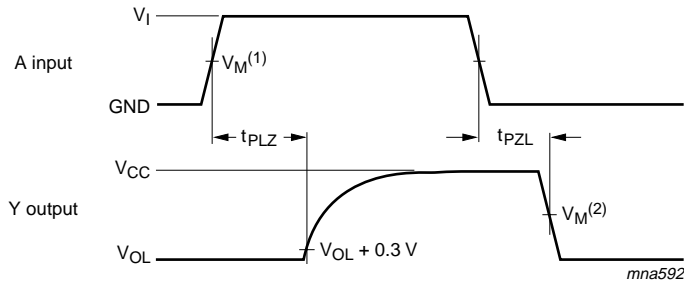
f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts

12. Waveforms

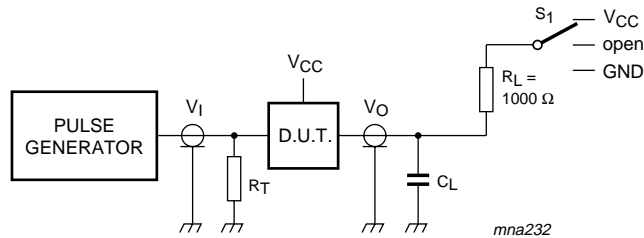


Measurement points are given in [Table 9](#).

Fig 5. Input (A) to output (Y) propagation delays

Table 9. Measurement point

Type	Input		Output
	V _I	V _M ⁽¹⁾	V _M ⁽²⁾
74AHC1G07	GND to V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}
74AHCT1G07	GND to 3.0 V	1.5 V	0.5 × V _{CC}



Test data is given in [Table 8](#). Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

For t_{PLZ}, t_{PZL}, S₁ = V_{CC}

Fig 6. Load circuitry for switching times

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

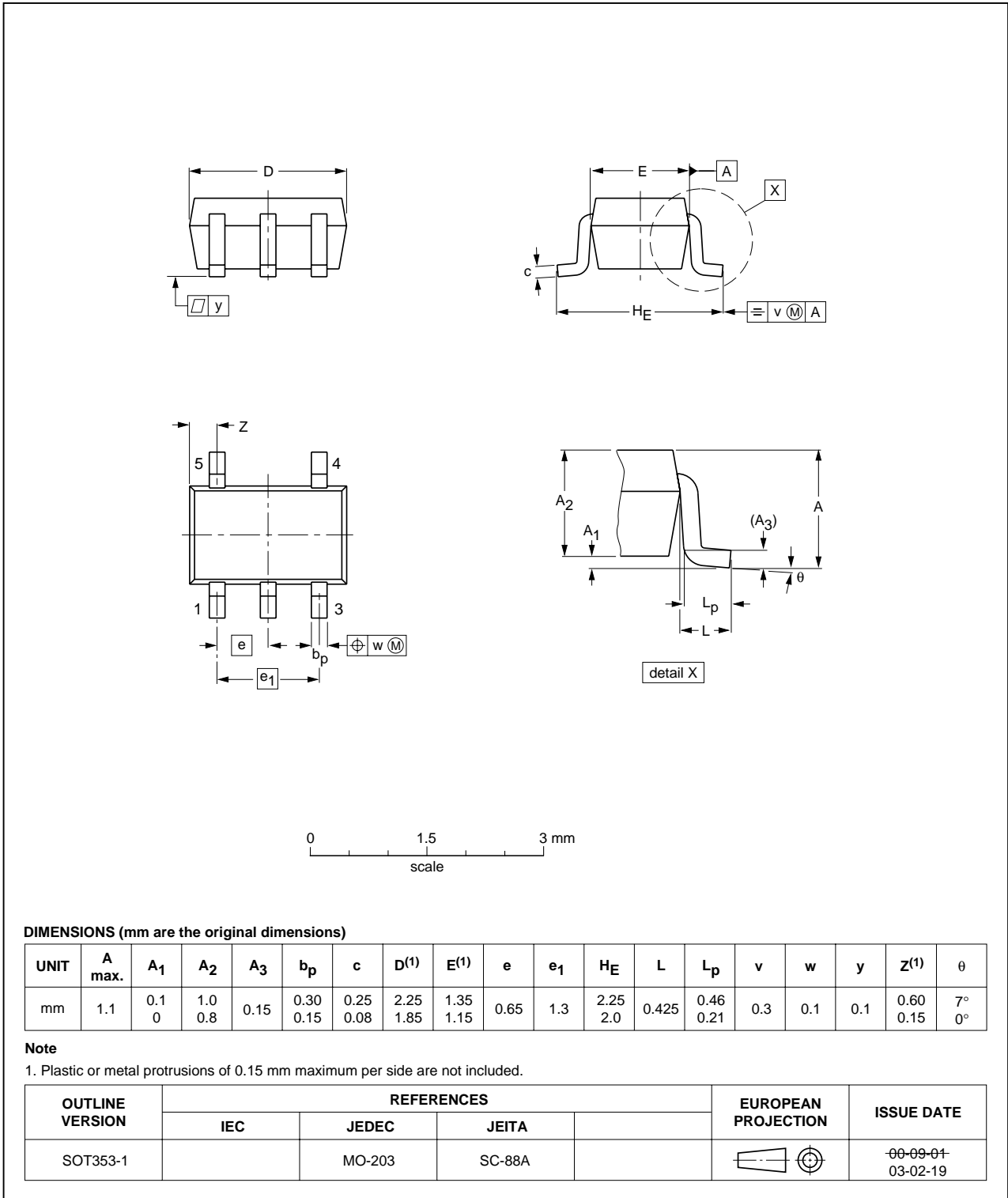


Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

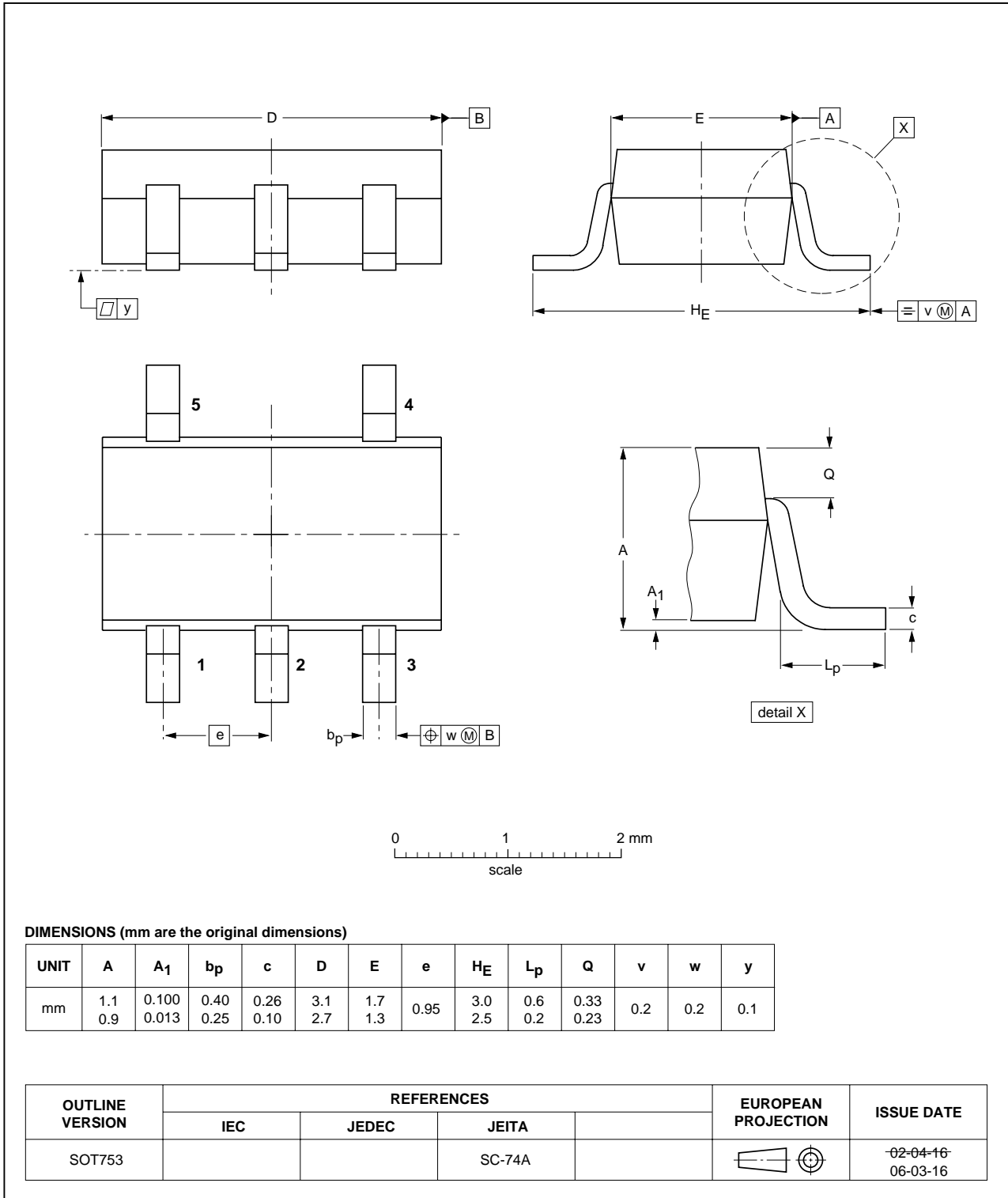


Fig 8. Package outline SOT753 (SC-74A)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G07_6	20070607	Product data sheet	-	74AHC_AHCT1G07_5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Package SOT353 changed to SOT353-1 in Section 3 and Section 13. Quick reference data and Soldering sections removed. 			
74AHC_AHCT1G07_5	20021002	Product specification	-	74AHC_AHCT1G07_4
74AHC_AHCT1G07_4	20020606	Product specification	-	74AHC_AHCT1G07_3
74AHC_AHCT1G07_3	20020221	Product specification	-	74AHC_AHCT1G07_2
74AHC_AHCT1G07_2	20010209	Product specification	-	74AHC_AHCT1G07_1
74AHC_AHCT1G07_1	20000502	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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