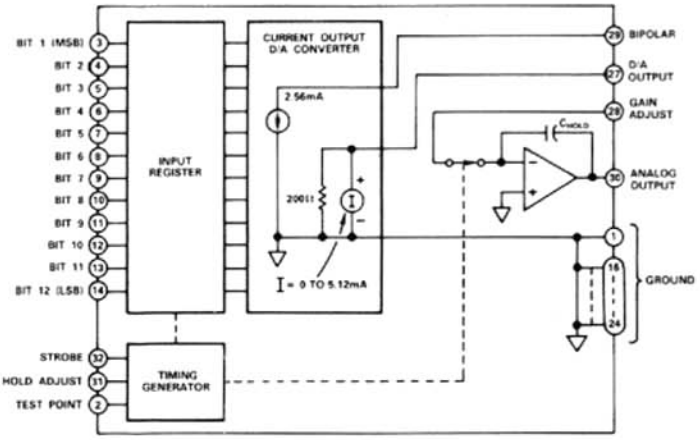
12-Bit Deglitched Voltage Out D/A Converter

HDD-1206

FEATURES
Registers, D/A, Amplifier in Single Hybrid
Deglitched Voltage Output
6MHz Update Rate

APPLICATIONS
Vector Scan Displays
Analytical Instrumentation
Digital VCOs
Military Systems

HDD-1206 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices HDD-1206 D/A converter combines innovative design techniques with remarkable hybrid construction to achieve deglitched voltage outputs at digital update rates as high as 6MHz.

Despite its small size and low power, the HDD-1206 provides the user with a complete solution to demanding applications which require the conversion of high-speed digital inputs into deglitched analog output voltages.

The unit is housed in an industry standard 32-pin hybrid and contains all the necessary circuit components to provide analog outputs at high update rates without the need for designing external circuits. Input registers, current-output D/A, deglitching circuits, and an output amplifier are all included inside the HDD-1206.

With the deglitching problem solved in a single package, the user of the HDD-1206 is able to incorporate the solution into his system with a minimum of design effort. User involvement is limited to the simple task of establishing the "hold" time for an optimum value by selecting the correct resistor value.

After that step is accomplished, the addition of a low-pass filter at the output of the D/A assures a "clean" voltage representation of the 12 bits of digital information applied to the inputs at video update rates.

The HDD-1206 is available in 32-pin dual in-line ceramic packages.

PIN DESIGNATIONS
HDD-1206

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	17	GROUND
2	TEST POINT	18	GROUND
3	BIT 1 (MSB)	19	GROUND
4	BIT 2	20	GROUND
5	BIT 3	21	GROUND
6	BIT 4	22	GROUND
7	BIT 5	23	GROUND
8	BIT 6	24	GROUND
9	BIT 7	25	+15V
10	BIT 8	26	-15V
11	BIT 9	27	D/A OUTPUT
12	BIT 10	28	GAIN ADJUST
13	BIT 11	29	BIPOLAR
14	BIT 12 (LSB)	30	OUTPUT
15	+5V	31	HOLD ADJUST
16	GROUND	32	STROBE

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 1kΩ output load unless otherwise noted)

Model	HDD-1206JW			HDD-1206SM			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION		12			*		Bits
LSB WEIGHT (FS = 10.24V)		2.5			*		mV
ACCURACY (Linearity)			±0.0125			*	% FS
Differential Nonlinearity		±1/2			*		LSB
Zero Offset[1] (Initial)		±35	±50		*	*	mV
Monotonicity		Guaranteed			*		
TEMPERATURE COEFFICIENTS							
Linearity		5			*		ppm/°C
Gain		60			*		ppm/°C
Offset		100			*		ppm/°C
DYNAMIC CHARACTERISTICS[2]							
Settling Time to ½LSB							
±5.12V FS Change		2			*		µs
1LSB Change		60			*		ns
Internal Current D/A		50			*		ns
Slew Rate		25			*		V/µs
Gain		Adjustable			*		V/V
DIGITAL DATA INPUTS							
Logic Compatibility		TTL(S)			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load (each bit)		One Standard			*		TTL(S) Load
Coding (see Table on last page)		Complementary Binary (CBN); Complementary Offset Binary (COB)			*		
STROBE INPUT							
Logic Compatiblity		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load		One Standard			*		TTL Load
Risetime/Falltime (10%–90%)			15			*	ns
Width	50		.65/word rate	*		*	ns
Frequency (see chart below)			6			*	MHz
OUTPUT (see Coding Table)							
R_{FB} = 1,000Ω							
Bipolar Voltage[3]		±2.56			*		V
Unipolar Voltage		0 to −5.12			*		V
Current	8			*			mA
R_{FB} = 2,000Ω							
Bipolar Voltage		±5.12			*		V
Current	8			*		*	mA
Residual Glitch		50	100		*	*	mV
Output Impedance		0.1	1		*	*	Ω
Capacitive Loading		1,000			*		pF
POWER REQUIREMENTS							
+15V ± 3% Current		55	60		*	*	mA
−15V ± 3% Current		30	35		*	*	mA
+5V ± 5% Current		95	130		*	*	mA
Power Supply Rejection Ratio	−2		+2		*		mV/V
Power Dissipation		1.95	2.25		*	*	W
TEMPERATURE RANGE							
Operating[4]	0		+70	−55		+125	°C
Storage	−55		+125	*		*	°C
THERMAL RESISTANCE[5]							
Junction to Air, θja (free air)		32			*		°C/W
Junction to Case, θjc		13			*		°C/W
MTBF[6]							
Mean Time Between Failures				3.015×10^5			Hours
PACKAGE OPTIONS[7]							
Ceramic (DH-32A)		HDD-1206JW					
Metal (DH-32C)					HDD-1206SM		

NOTES
[1] Adjustable to zero.
[2] All dynamic characteristics are based on FS = ±5.12V; R_{FB} = 2,000Ω.
[3] With R_{FB} = 1k, analog output voltages are half those shown in Table on last page.
[4] Case Temperature.
[5] Maximum junction temperature is 150°C.
[6] Calculated per MIL-HDBK 217, Ground; Fixed; Case Temperature = 60°C.
[7] See Section 14 for package outline information.
*Specifications same as HDD-1206JW.
Specifications subject to change without notice.

THEORY OF OPERATION

The equivalent circuit for the for the HDD-1206 D/A converter is shown in functional block diagram.

The unit consists of input registers, fast-settling current output D/A, output amplifier, timing generator, and associated circuits.

The purpose of the input register circuits is to de-skew the input bits and assure their simultaneous arrival at the input of the current D/A. This is critical because time skew on the input data bits is a major contributor to discontinuities, or "glitches," in the analog output of a D/A.

The Timing Generator includes a Track & Hold circuit and generates the required internal pulses for operation whenever it receives a Strobe input pulse. See Figure 1, the HDD-1206 timing diagram.

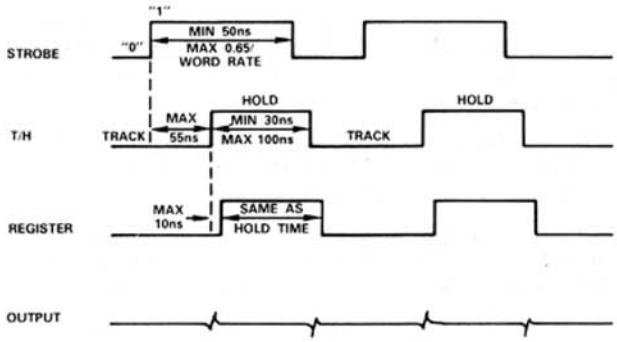


Figure 1. HDD-1206 Timing Diagram (Digital Inputs not Changing)

As shown, the Strobe pulse is a positive-going TTL pulse supplied by the user of the HDD-1206. Internal timing circuits establish the maximum 55ns delay from the leading edge of the Strobe pulse to the leading edge of the T/H (Track/Hold) pulse; and the maximum 10ns delay from the leading edge of the T/H pulse to the leading edge of the Register pulse. The data from the input registers are strobed into the current D/A at the end of this 65ns interval, so they must be valid by that time.

The user determines the width of the T/H pulse (and the Register pulse) by selecting the value of the R_{HOLD} resistor. See Figures 1 and 2. As shown, the width of the Hold pulse can vary from approximately 30ns to approximately 100ns by using resistor values from 1k to 5k, respectively.

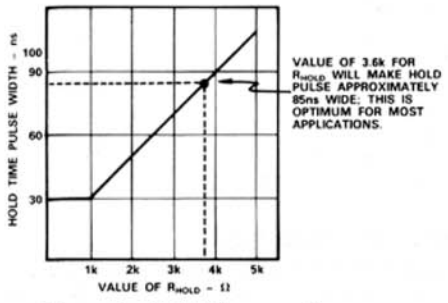


Figure 2. Hold Time vs. R_{HOLD}

For most applications, a value of 3.6kΩ and a pulse width of approximately 85ns is the optimum choice. This pulse width will "hold" the analog output of the HDD-1206 D/A until the "glitch" resulting from the most recent update has passed, without infringing on the word rate capabilities of the HDD-1206.

CURRENT-OUTPUT D/A CONVERTERS

A brief review of the salient characteristics of current D/A converters may be a useful approach to understanding the operation of the HDD-1206 unit.

Current-switching D/A converters are inherently faster than voltage-output types because of the absence of an output amplifier. This means current-switching converters have no slew rate limitation which can slow settling; nor are they subject to the overshoot and ringing problems often associated with feedback amplifiers.

Both current-switching and voltage-output converters display a discontinuity, or "glitch," in their analog outputs because of the basic characteristic of saturated logic (TTL is an example) which causes the propagation delay to be less for negative-going inputs than it is for positive-going inputs.

This difference in propagation delay manifests itself as a "worst case glitch" at the major carry point, or mid-scale, of the output range of the current converter. This is the point at which nearly equal and opposite currents are being switched within the converter.

The "glitch" at mid-scale, the switching point of the Most Significant Bit (MSB), will be halved at the ¼ and ¾ points; halved again at the ⅛ and ⅞ points, etc. The amplitude of the "glitch," therefore, is a function of signal dynamics and cannot be eliminated with filtering.

The variations in glitch amplitude caused by signal dynamics create a multitude of intermodulation (IM) products, some of which fall into the video pass-band as spurious signals, and increased noise level. These IM products are also relatively immune to elimination by filtering.

The amplitude of the glitch can be reduced by de-skewing the input bits; but no amount of de-skewing or filtering can negate the physics of saturated logic which cause the glitch to be generated initially.

The best solution, then, is to cause the glitch to remain a constant across the entire output range of the converter. The efficiencies of the circuit will be enhanced if the solution can also permit using the full drive capabilities of the current-output D/A in either unipolar or bipolar modes of operation.

The design approach used in the Analog Devices HDD-1206 D/A converter accomplishes these desired goals and provides voltage outputs at high update rates.

NOTES ON DEGLITCHING

Refer again to the equivalent circuit for the HDD-1206. The data bits are applied through the input register to the current-output D/A converter, which is capable of supplying up to 5.12mA of output current.

The output of the current D/A, in turn, is applied to the input of the output amplifier via strapping external to the HDD-1206. The Timing Generator supplies the necessary pulses and timing to apply signals to the current D/A and output amplifier after the initial glitch caused by the digital inputs has subsided.

The digital "1" (Hold) level of the T/H pulse causes the switch at the input of the amplifier to open, holding the last value of the current D/A converter. During this hold interval, the switching transients caused by updating digital inputs are masked from the amplifier, thereby avoiding HDD-1206 output discontinuities whose amplitude would be a function of signal dynamics.

Ten nanoseconds after the T/H pulse goes to the digital "1" level, the register pulse also changes state from "0" to "1".

This transition moves the output of the current D/A to the new value established by the most recent digital inputs applied to the HDD-1206.

Any change in the current D/A output has stablized by the time the T/H pulse returns to the digital "0" (Track) level. Re-establishing the track mode closes the switch at the input of the amplifier and the output of the HDD-1206 moves to the new analog value dictated by the digital input word.

As shown in Figure 1, the output of the HDD-1206 will contain switching transients associated with the T/H pulse. But these "glitches" will be constant in amplitude and duration and will occur at the update rate, since they are a function of the strobe pulse applied by the user.

These switching transients will settle out in approximately 500ns, and will have uniform amplitude over the complete analog output range of the D/A. For strobe rates of 2MHz and above, the settling interval switching from "hold" to "track", and vice versa, will produce a constant dc offset on the output. The HDD-1206 is not intended to get rid of all glitches per se; it is designed to provide a constant-amplitude glitch.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line, i.e., a single-line spectrum at the sample rate frequencies, and harmonics of the sample frequency.

The HDD–1206 effectively eliminates the IM products discussed above. When it does, the signal-to-noise (S/N) ratio approaches that of an ideally-quantized signal, where the rms noise is $q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

GLITCH VS. PEDESTAL

In addition to the "glitch" which is a characteristic of current D/As, the track & hold used in the HDD-1206 also contributes an anomaly to the output signal.

Refer to Figure 3. This diagram compares the "glitch" created by the HDD-1206 to the pedestal created by the internal T/H circuits.

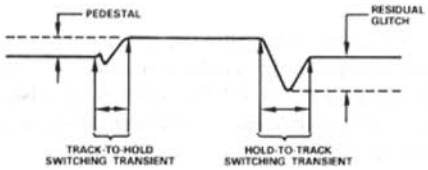


Figure 3. Pedestal/Glitch Relationship

As shown, the "glitch" is a transient signal which remains constant in width and amplitude over the entire output range, at all update rates. The pedestal, on the other hand, is an offset signal whose amplitude can vary (because of switching transient settling) as a function of hold time and word rate.

This pedestal is caused by charge transfer associated with the hold capacitor; the transfer occurs when the HDD-1206 circuits are switched from a "track" to "hold" condition. The pedestal is basically an offset error in the HDD-1206 output and can be compensated with the Offset Adjust when the unit is installed in the user's system.

Figure 3 is not drawn to scale; there is no attempt to imply the identified elements have precisely that relationship to one another. They are exaggerated for illustrative purposes.

Applications

Bipolar connections for the HDD-1206 D/A converter are shown in Figure 4. As indicated, a unipolar negative output is accomplished by connecting Bipolar Pin 29 to ground, instead of to Pins 27 and 28.

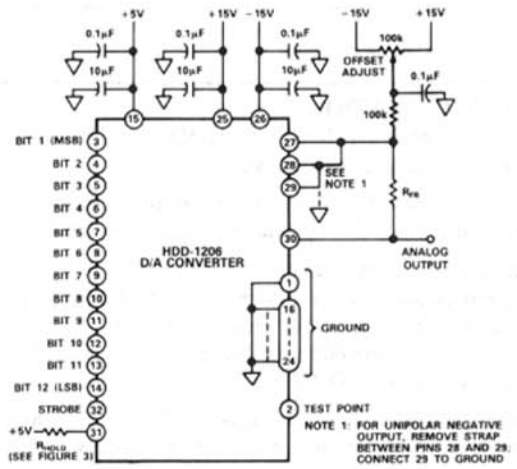


Figure 4. HDD-1206 Bipolar Connections

The output voltage swing is established by the value of feedback resistor R_{FB}. The table below indicates output levels for both unipolar and bipolar operation, with feedback resistors of either 1,000Ω or 2,000Ω.

Hold resistor R_{HOLD} connected between the +5V supply and Pin 31 sets the width of the Hold mode of the T/H pulse. Test Point Pin 2 is used for observing the pulse.

The Offset Adjust potentiometer is used to set the desired analog output of the HDD-1206 and can be used to help assure correct voltages are present when the D/A is installed in the system.

When operated in a unipolar mode with digital "0" applied to all inputs but no continuous strobe pulses applied, the Offset Adjust is set for an analog output of −5.12V or less 1LSB, with 1k for the value of R_{FB}. (NOTE: At least one strobe pulse needs to be applied to latch the input data into the registers.)

If the HDD-1206 is installed in a system and the strobe pulse is applied continuously, the Offset Adjust is calibrated for the desired output value with a digital "0" applied to all input pins.

HDD-1206 ANALOG OUTPUT WITH 1kΩ LOAD

Digital Inputs	Complementary Offset Binary (COB) Bipolar Output R_{FB} = 2k	Complementary Binary (CBN) Unipolar Negative Output R_{FB} = 1k
111...111	+5.12 (+FS)	0.0000 (0)
111...110	+5.1175	− 0.00125 (+1LSB)
110...000	+2.5625 (+1/2FS)	− 1.27875
101...111	+2.56	− 1.28 (1/4)
100...000	+0.0025 (+1LSB)	− 2.55875
011...111	0.0000	− 2.56 (1/2)
010...000	−2.5575 (−1/2FS)	− 3.83875
001...111	−2.56	− 3.84 (3/4)
000...001	−5.1150	−5.1175
000...000	−5.1175 (−FS − 1LSB)	−5.11875 (FS − 1LSB)

ORDERING INFORMATION

Model HDD-1206JW D/A converter is housed in a ceramic package, the model HDD-1206SM is a hermetically sealed version; outline dimensions are shown elsewhere.

Mating individual pin sockets are available from AMP. Part number 6-330808-0 are knockout end type; 6-330808-3 are open end type.

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