

# CLC110

## Wideband, Closed-Loop Monolithic Buffer Amplifier

### General Description

Using a unique closed-loop design, the CLC110 buffer offers a high-fidelity, high-performance alternative to conventional open-loop buffers. For example, the  $-3\text{dB}$  bandwidth is  $730\text{MHz}$  ( $0.5V_{pp}$ ) and the settling time to  $0.2\%$  is typically only  $5\text{ns}$ . Yet all this is achieved while maintaining excellent signal fidelity as demonstrated by the  $-65\text{dBc}$  harmonic distortion at  $20\text{MHz}$  – a value unmatched by any high-speed buffer.

The CLC110 is an ideal choice for a wide variety of applications. With its speed and accuracy, the CLC110 offers designers the benefit of buffering signals which might otherwise go unbuffered due to performance penalties imposed by conventional buffers. For example, the CLC110 is well suited for use within closed-loop systems such as amplifier or phase locked loop systems; with its  $400\text{ps}$  rise time, its effect on loop dynamics is usually negligible.

Ultra-fast flash A/D converter systems can also benefit from the speed of the CLC110. And, since most flash A/D's have capacitive inputs, the CLC110's dynamic performance has been characterized for various loads. In addition, the amplifier specifications are for a  $100\Omega$  load.

The CLC110 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC110AJP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	8-pin plastic DIP
CLC110AJE	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	8-pin plastic SOIC

DESC SMD number: 5962-89975

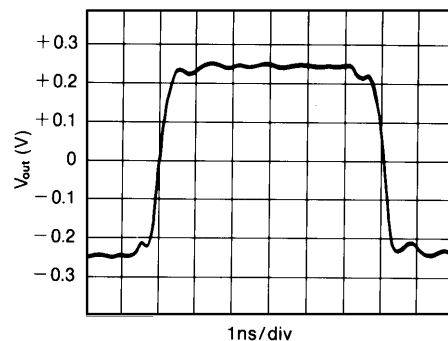
### Features

- Closed-loop, unity-gain operation
- $-3\text{dB}$  bandwidths of  $730\text{MHz}$  ( $0.5V_{pp}$ )
- $0.2\%$  settling in  $5\text{ns}$
- Low power,  $150\text{mW}$
- Low distortion,  $-65\text{dBc}$  at  $20\text{MHz}$

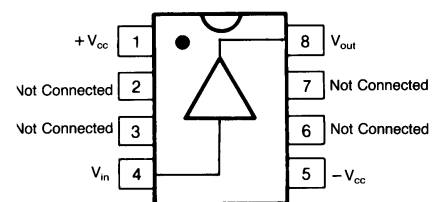
### Applications

- Ultra-fast flash A/D conversion
- Line driving
- High-speed communications
- Impedance transformation
- Power buffers
- IF processors

Small Signal Pulse Response



Pinout  
DIP & SOIC



# CLC110 Electrical Characteristics ( $V_{cc} = \pm 5V$ , $R_L = 100\Omega$ , $R_S = 50\Omega$ ; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC110AJ	+25°C	-40°C	+25°C	+85°C		
<b>FREQUENCY DOMAIN PERFORMANCE<sup>1</sup></b>							
-3dB bandwidth	$V_{out} < 0.5V_{pp}$	730	>400	>400	>300	MHz	SSBW
gain flatness	$V_{out} < 5V_{pp}$	90	>50	>55	>50	MHz	LSBW
peaking	$V_{out} < 0.5V_{pp}$	0	<0.8	<0.5	<0.6	dB	GFPH
rolloff	DC to 200MHz	0	<1.0	<0.8	<1.2	dB	GFRH
group delay	DC to 200MHz	0.75	<1.0	<1.0	<1.2	ns	GD
linear phase deviation	DC to 200MHz	0.7	<1.5	<1.5	<2.0	°	LPD
<b>TIME DOMAIN PERFORMANCE<sup>1</sup></b>							
rise and fall time (input signal rise/fall = 300ps)	0.5V step	0.4	<1.0	<1.0	<1.4	ns	TRS
overshoot (input signal rise/fall = 300ps)	0.5V step	0	<15	<10	<15	%	OS
rise and fall time (input signal rise/fall $\leq$ 1ns)	5V step	4.5	<8.5	<7.5	<8.5	ns	TRL
settling time to $\pm 0.2\%$	2V step	5	<10	<10	<10	ns	TSP
slew rate		800	>450	>500	>450	V/ $\mu$ s	SR
<b>DISTORTION AND NOISE PERFORMANCE</b>							
2nd harmonic distortion	$2V_{pp}$ , 20MHz	-65	<-48	<-55	<-55	dBc	HD2
	$2V_{pp}$ , 50MHz	-60	<-48	<-55	<-55	dBc	HHD2
3rd harmonic distortion	$2V_{pp}$ , 20MHz	-65	<-55	<-55	<-55	dBc	HD3
	$2V_{pp}$ , 50MHz	-60	<-50	<-50	<-45	dBc	HHD3
equivalent input noise							
noise floor	> 1MHz	-158	<-155	<-155	<-154	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	<57	<57	<63	$\mu$ V	INV
<b>STATIC, DC PERFORMANCE</b>							
small signal gain into 100 $\Omega$ load		0.97	>0.95	>0.96	>0.95	V/V	GA
integral endpoint linearity	$\pm 2V$ full scale	0.2	<0.8	<0.4	<0.3	%FS	ILIN
* output offset voltage		2	<16	<8.0	<13	mV	VIO
average temperature coefficient		20	<100	—	<50	$\mu$ V/ $^{\circ}$ C	DVIO
* input bias current		20	<100	<50	<50	$\mu$ A	IBN
average temperature coefficient		200	<700	—	<300	nA/ $^{\circ}$ C	DIBN
power supply rejection ratio		50	>45	>45	>45	dB	PSRR
* supply current	no load	15	<20	<20	<20	mA	ICC
<b>MISCELLANEOUS PERFORMANCE</b>							
input resistance		160	>50	>100	>200	k $\Omega$	RIN
capacitance		1.6	<2.5	<2.2	<2.5	pF	CIN
output impedance	at DC	2	<3.5	<3.0	<3.5	$\Omega$	RO
output voltage range	100 $\Omega$ load	$\pm 4$	> $\pm 3.0$	> $\pm 3.2$	> $\pm 3.2$	V	VO
output current		$\pm 70$	> $\pm 45$	> $\pm 50$	> $\pm 50$	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Absolute Maximum Ratings

## Miscellaneous Ratings

$V_{cc}$	$\pm 7V$
$I_{out}$	output is short circuit protected to ground, but, maximum reliability will be obtained if $I_{out}$ does not exceed...
input voltage	70mA
junction temperature	$\pm V_{cc}$
operating temperature range	+150°C
AI:	-40°C to +85°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

### Notes:

- \* AJ 100% tested at +25°C.
- note 1: AC performance is very dependent on layout. Specifications apply only in a 50 $\Omega$  microstrip environment.

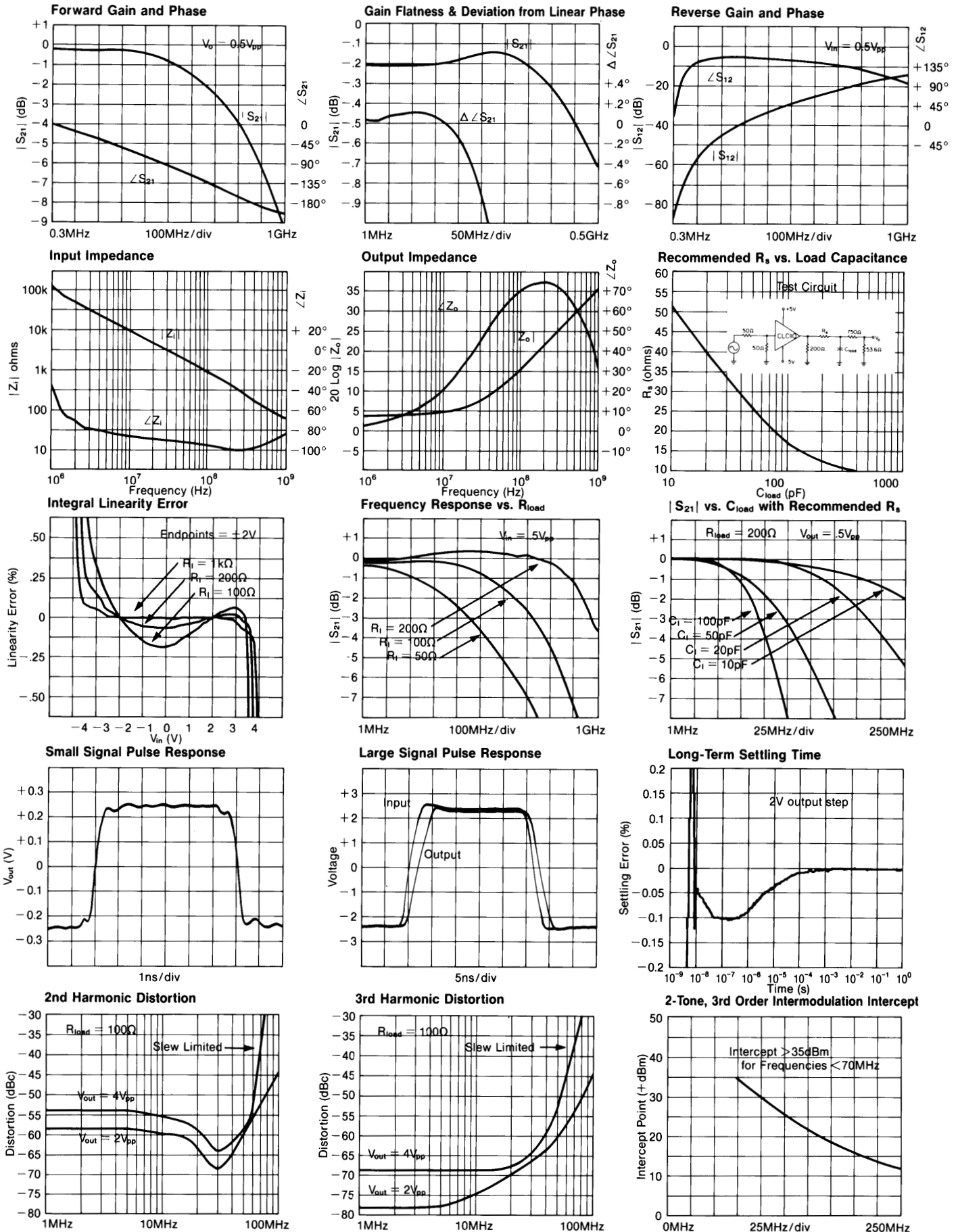
## Package Thermal Resistance

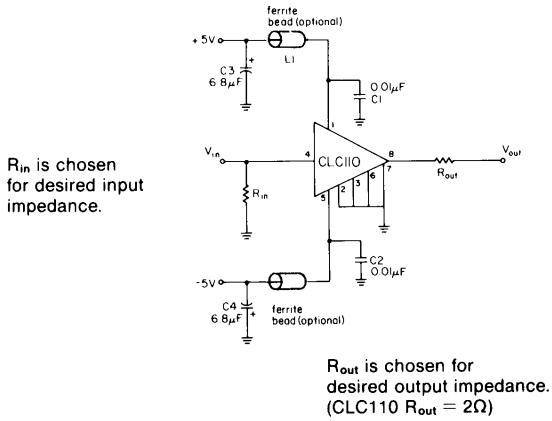
Package	$\theta_{JC}$	$\theta_{JA}$
Plastic (AJP)	65°C/W	115°C/W
Surface Mount (AJE)	55°C/W	125°C/W

## Reliability Information

Transistor Count	21
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# CLC110 Typical Performance Characteristics ( $V_{CC} = \pm 5V$ , $R_L = 100\Omega$ , $R_S = 50\Omega$ ; unless specified)





**Figure 1:** recommended circuit and evaluation board schematic

### Operation

The CLC110 is based upon a unique, patented closed-loop design, which provides the accuracy characteristics of a closed-loop amplifier, yet also has unmatched dynamic performance.

### Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC110, which has a typical bandwidth of 730MHz.

To minimize capacitive feedthrough, the pins not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC110. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation is needed from high-frequency (>400MHz) resonances of the power supply.

Parasitic or load capacitance directly on the output of the CLC110 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and the resulting performance vs. capacitance.

Precision buffered resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they will cause a degradation of AC performance due to their reactive nature at high frequencies.

### Evaluation Board

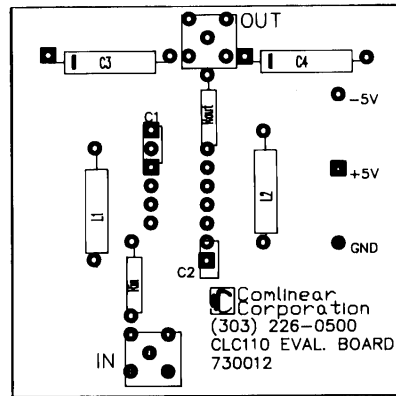
An evaluation board (part CLC730012) is available for the CLC110 to assist in the evaluation of the CLC110. It may also be used as a guide in developing a printed circuit layout. Figure 1 shows the board's schematic; Figures 2 through 4 show the board layout.

### Evaluation Board Parts List:

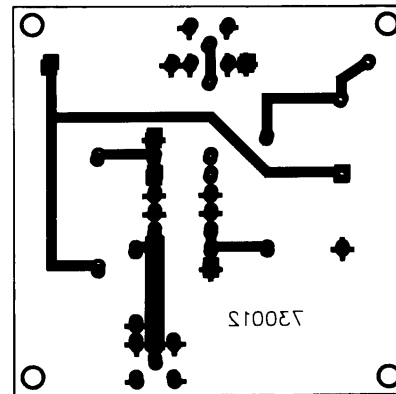
- $R_{in}$  select for desired input impedance
- $R_{out}$  select for desired output impedance
- $C_1, C_2$  0.1µF ceramic radial lead
- $C_3, C_4$  6.8µF (Sprague 150D series)
- $L_1, L_2$  ferrite beads (optional) (Ferroxcube #VK 200 19/4B)

### Hardware (optional)

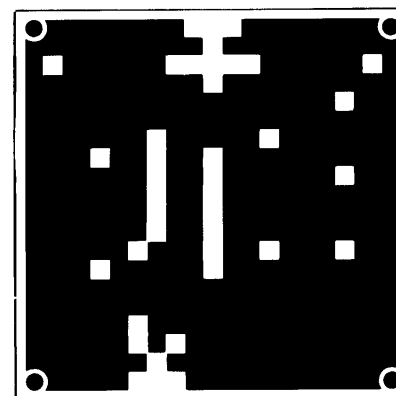
- Sockets Cambion flush-mount connector jacks (#450-2598-01-06-00)
- SMA Connectors (female)
  - Amphenol 901-144 (straight)
  - Amphenol 901-143 (angled)



**Figure 2:** component placement guide



**Figure 3:** solder side (bottom) as viewed from component side (top)



**Figure 4:** component side (top) showing extensive ground plane

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