August 1996

National Semiconductor

Comlinear CLC404
Wideband, High-Slew Rate, Monolithic Op Amp

General Description

The CLC404 is a high-speed, monolithic op amp that combines low power consumption (110mW typical, 120mW maximum) with superior large signal performance. Operating off of ±5V supplies, the CLC404 demonstrates a large-signal bandwidth ($5V_{pp}$ output) of 165MHz. The bandwidth performance, along with other speed characteristics such as rise and fall time (2.1ns for a 5V step), is nearly identical to the small signal performance since slew rate is not a limiting factor in the CLC404 design.

With its 175MHz bandwidth and 10ns settling (to 0.2%), the CLC404 is ideal for driving ultra-fast flash A/D converters. The 0.5° deviation from linear phase, coupled with -53dBc 2nd harmonic distortion and -60dBc 3rd harmonic distortion (both at 20MHz), is well suited for many digital and analog communication applications. These same characteristics, along with 70mA output current, differential gain of 0.07%, and differential phase at 0.03°, make the CLC404 an appropriate high-performance solution for video distribution and line driving applications.

Constructed using an advanced, complementary bipolar process and Comlinear's proven current feedback topologies, the CLC404 provides performance far beyond that of other monolithic op amps. The CLC404 is available in several versions to meet a variety of requirements. A three-letter suffix determines the version:

CLC404AJP	-40°C to +85°C	8-pin plastic DIP
CLC404AJE	-40°C to +85°C	8-pin plastic SOIC
CLC404ALC	-40°C to +85°C	dice
CLC404AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B
CLC404AID	-40°C to +85°C	8-pin sidebrazed CERDIP
CLC404A8D	-55°C to +125°C	8-pin sidebrazed CERDIP, MIL-STD-883, Level B
CLC404AJM5	-40°C to +85°C	5-pin SOT

DESC SMD number: 5962-90994

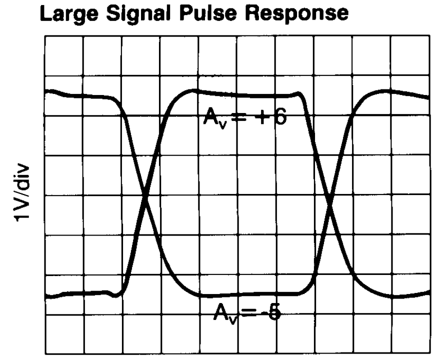
Features

- 165MHz large signal bandwidth ($5V_{pp}$)
- 2600V/µs slew rate
- Low power: 110mW
- Low distortion: -53dBc at 20MHz
- 10ns settling to 0.2%
- 0.07% diff. gain, 0.03% diff. phase

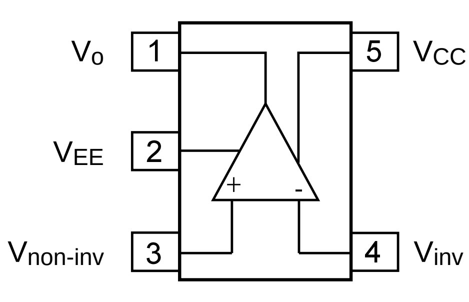
Applications

- Fast A/D conversion
- Line drivers
- Video distribution
- High-speed communications
- Radar, IF processors

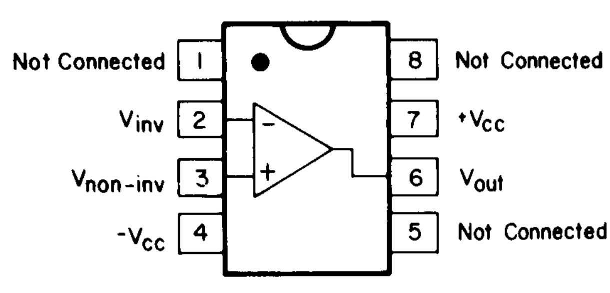
Large Signal Pulse Response



Pinout
SOT23-5



Pinout
DIP & SOIC



CLC404 Electrical Characteristics (A_V = +6, V_{CC} = ±5V, R_g & R_L = 100Ω, R_f = 500Ω; unless specified)

PARAMETER	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC404A8/AL/AM	+25°C	−55°C	+25°C	+125°C		
Ambient Temperature	CLC404AJ/AI	+25°C	−40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† -3dB bandwidth	Vout<$2V_{pp}$	175	>150	>150	>120	MHz	SSBW
-3dB large signal	Vout<$5V_{pp}$	165	>140	>140	>110	MHz	LSBW
gain flatness[3]	Vout<$2V_{pp}$						
† peaking	<40MHz	0	<0.4	<0.3	<0.4	dB	GFPL
† peaking	>40MHz	0	<0.7	<0.5	<0.7	dB	GFPH
† rolloff	<75MHz	0.2	<1.0	<1.0	<1.3	dB	GFR
linear phase deviation	DC to 75MHz	0.5	<1.0	<1.0	<1.2	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.0	<2.4	<2.4	<2.9	ns	TRS
	5V step	2.1	<2.6	<2.6	<3.2	ns	TRL
settling time to ±0.2%	2V step	10	<15	<15	<15	ns	TS
overshoot	2V step	5	<15	<12	<15	%	OS
slew rate (measured at A_v +2)[1]		2600	>2000	>2000	>2000	V/µs	SR
DISTORTION AND NOISE RESPONSE							
† 2nd harmonic distortion	$2V_{pp}$, 20MHz	−53	<−40	<−45	<−45	dBc	HD2
† 3rd harmonic distortion	$2V_{pp}$, 20MHz	−60	<−50	<−50	<−50	dBc	HD3
equivalent input noise							
noise floor	>1MHz	−159	<−157	<−157	<−156	dBm(1Hz)	SNF
integrated noise	1MHz to 200MHz	40	<45	<45	<50	µV	INV
differential gain[2]		0.07	—	—	—	%	DG
differential phase[2]		0.03	—	—	—	°	DP
STATIC, DC PERFORMANCE							
* input offset voltage		2	<±9.0	<±5.0	<±10.0	mV	VIO
average temperature coefficient		30	<±50	—	<±50	µV/°C	DVIO
* input bias current	non-inverting	15	<±44	<±22	<±22	µA	IBN
average temperature coefficient		150	<±275	—	<±200	nA/°C	DIBN
* input bias current	inverting	15	<±40	<±18	<±22	µA	IBI
average temperature coefficient		150	<±275	—	<±200	nA/°C	DIBI
† power supply rejection ratio		52	>45	>48	>45	dB	PSRR
common mode rejection ratio		50	>44	>46	>44	dB	CMRR
* supply current	no load, quiescent	11	<12	<12	<12	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input	resistance	1000	>250	>500	>1000	kΩ	RIN
	capacitance	1	<2	<2	<2	pF	CIN
output impedance	at DC	0.1	<0.3	<0.2	<0.2	Ω	RO
output voltage range	no load	±3.3	>±2.8	>±3.0	>±3.0	V	VO
common mode input range for rated performance		±2.2	>±1.4	>±1.8	>±2.0	V	CMIR
output current	−40°C to +85°C	±70	>±35	>±50	>±50	mA	IO
	−55°C to +125°C	±70	>±30	>±50	>±50	mA	IO

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

V_{cc}	±7V
output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	70mA
common mode input voltage	$\pm V_{cc}$
differential input voltage	10V
junction temperature	+ 175°C
operating temperature range	
AI/AJ:	– 40°C to + 85°C
A8/AM/AL:	– 55°C to + 125°C
storage temperature range	– 65°C to + 150°C
lead solder duration (+ 300°C)	10 sec

Miscellaneous Ratings

recommended gain range: + 2 to + 21, – 1 to – 20

NOTES:

*	AI, AJ	100% tested at + 25°C, sample at + 85°C.
†	AJ	Sample tested at + 25°C.
†	AI	100% tested at + 25°C.
*	A8	100% tested at + 25°C, – 55°C, + 125°C.
†	A8	100% tested at + 25°C, sample – 55°C, + 125°C.
*	AL, AM	100% wafer probe tested at + 25°C to + 25°C. min/max specifications.

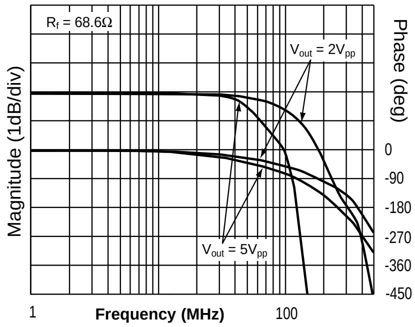
note 1: See the text on the back page of the datasheet.

note 2: Differential gain and phase measured at A_v + 2, R_f 500Ω, R_L 150Ω $1V_{pp}$ equivalent video signal, 0-100 IRE, 40 IRE_{pp}, 0IRE = 0 volts, at 75Ω load and 3.58MHz. See text.

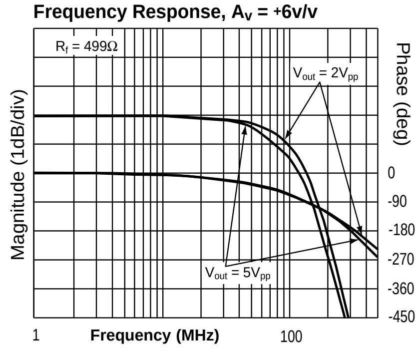
note 3: Gain flatness tests are performed from 0.1MHz.

CLC404 Typical Performance Characteristics (T_A = 25°, A_V = +6, V_{CC} = ±5V, R_L = 100Ω, R_f = 500Ω; unless specified)

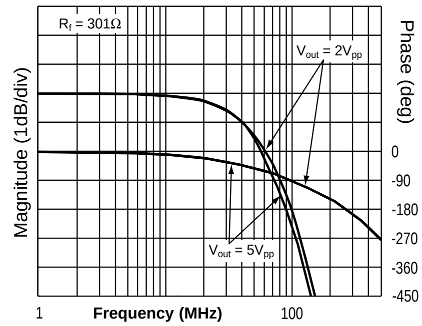
Frequency Response, A_v = +2v/v



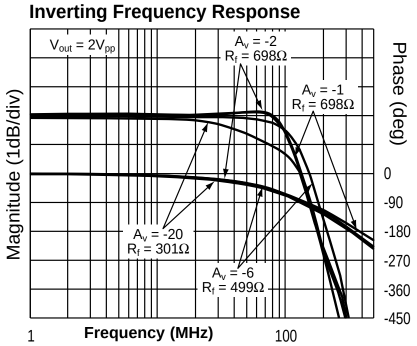
Frequency Response, A_v = +6v/v



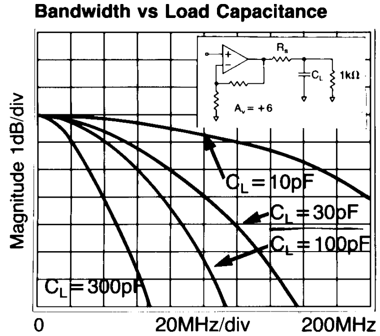
Frequency Response, A_v = +20v/v



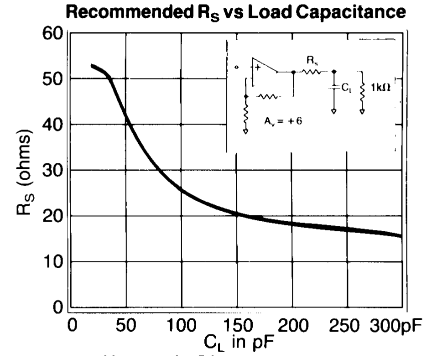
Inverting Frequency Response



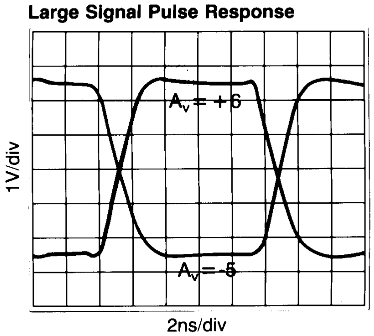
Bandwidth vs Load Capacitance



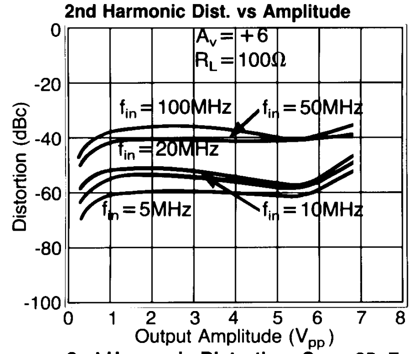
Recommended R_S vs Load Capacitance



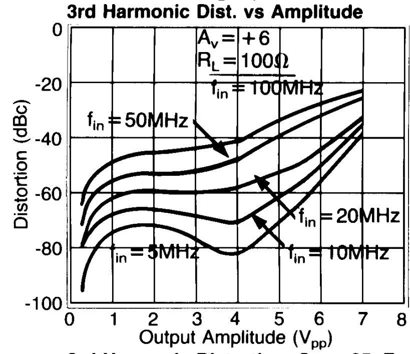
Large Signal Pulse Response



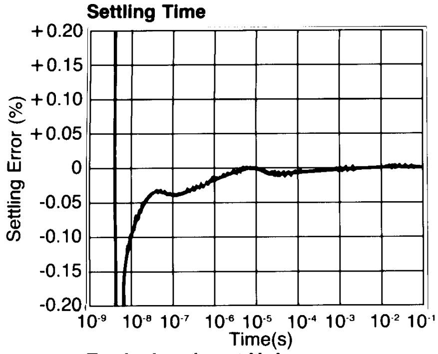
2nd Harmonic Dist. vs Amplitude



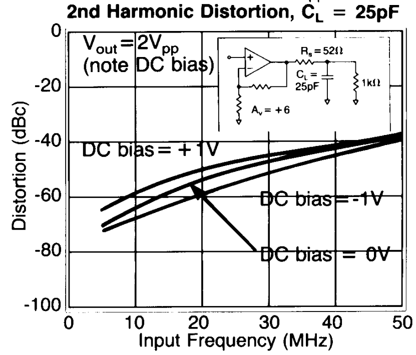
3rd Harmonic Dist. vs Amplitude



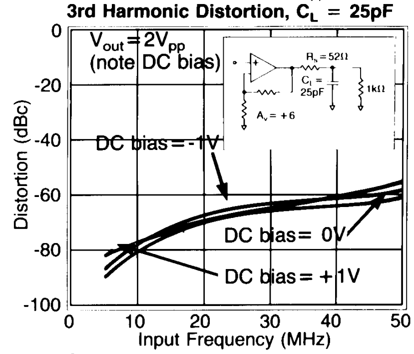
Settling Time



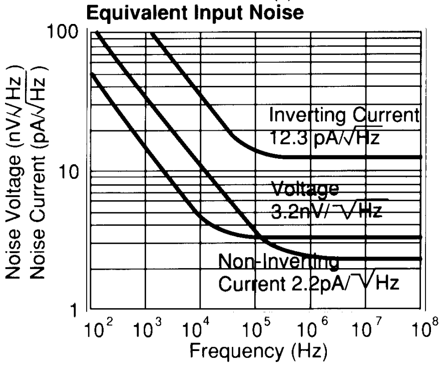
2nd Harmonic Distortion, C_L = 25pF



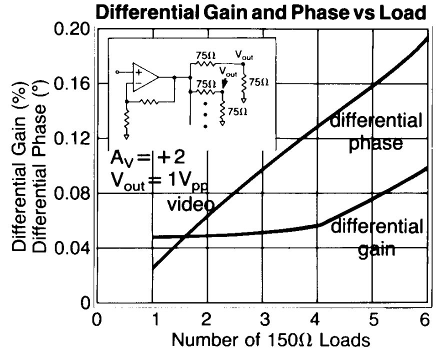
3rd Harmonic Distortion, C_L = 25pF



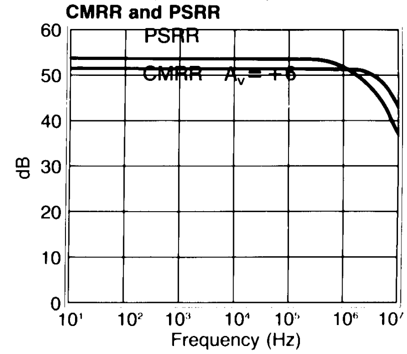
Equivalent Input Noise

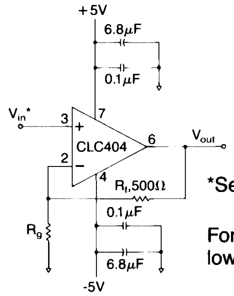


Differential Gain and Phase vs Load



CMRR and PSRR





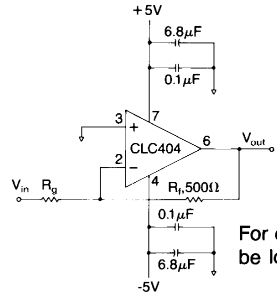
$$A_V = 1 + \frac{R_f}{R_g}$$

*See source impedance discussion.

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 1: recommended non-inverting gain circuit



$$A_V = \frac{-R_f}{R_g}$$

For optimum performance, R_f and R_g should be low-inductance, low-capacitance resistors.

(Pin designations are for DIP versions.)

Figure 2: recommended inverting gain circuit

Slew Rate

Slew rate limiting is a nonlinear response which occurs in amplifiers when the output voltage swing approaches hard, abrupt limits in the speed at which it can change. In most applications, this results in an easily identifiable "slew rate" as well as a dramatic increase in distortion for large signal levels. The CLC404 has been designed to provide enough slew rate to avoid slew rate limiting in almost all circuit configurations. The large signal bandwidth of 165MHz, therefore, is nearly the same as the 175MHz small signal bandwidth. The result is a low-distortion, linear system for both small signals *and* large signals.

Slew rate and large signal performance in the CLC404 can best be understood by first comparing the small and large signal performance plots at a gain of +6. In the CLC404, there is almost no difference between large and small signal performance at this gain. Large signal performance in the CLC404 at a gain of +6 is not slew rate limited. (In an amplifier which is slew limiting, the large signal response rolloff has an abrupt break indicating the onset of slew rate limitation.)

The CLC404 reaches slew rate limits only for low non-inverting gains. In other words, slew rate limiting is constrained by common mode voltage swings at the input. (This is different from traditional slew rate constraints.) The large-signal frequency response plot at a gain of +2 shows a break in the response, which shows that slew rate limit has been reached. Note also that the frequency response plots at gain of +21 show that the large signal and small signal responses are nearly identical.

Differential Gain and Phase

Differential gain and phase are measurements useful primarily in composite video channels. Differential gain and phase are measured by monitoring the gain and phase of a high frequency carrier (3.58MHz for NTSC composite video) as the output of the amplifier is swept over a range of DC voltages. Any changes in gain and phase at the carrier frequency are the desired measurement, differential gain and phase.

Specifications for the CLC404 include differential gain and phase. The test signals used are based on a $1V_{pp}$ video level. Test conditions used are the following:

DC sweep range:	0 to 100 IRE units (black to white)
Carrier:	3.58MHz at 40 IRE units peak to peak

The amplifier is specified for a gain of +2, and 150Ω load (for a backmatched 75Ω system). IRE amplitudes are referred to 75Ω, at the load of a video system. This is a different condition from the rest of the specifications ($A_v = +6, R_l = 100\Omega$).

Source Impedance

For best results, source impedance in the non-inverting circuit configuration (see Figure 1) should be kept below 3kΩ. Above 3kΩ it is possible for oscillation to occur, depending on other circuit parasitics. Depending on the signal source, a resistor with a value of less than 3kΩ may be used to terminate the non-inverting input to ground.

Feedback Resistor

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value resistor. The CLC404 provides optimum performance with a 500Ω feedback resistor. Furthermore, the specifications shown on the previous pages are valid only when a 500Ω feedback resistor is used. Selection of an incorrect value can lead to severe rolloff in frequency-response (if the resistor value is too large) or peaking or oscillation (if the value is too low). See Comlinear application notes AN and AN 300-1 for a complete discussion of current feedback.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC404 are available.

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