

2-channel REC/PB Amplifier for 8mm VCR

Description

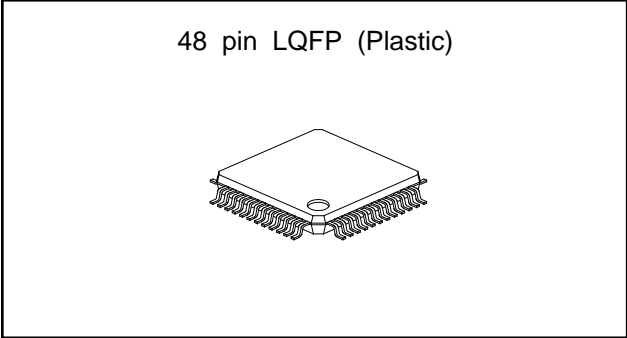
The CXA1704R is a bipolar IC designed as a recording/playback amplifier for Hi8-compatible VCRs.

Features

- O Recording system
 - Feedback damping provided in the recording amplifier and its EVR control function facilitate circuit board design.
 - Y, chroma, and low-band level adjustment functions
 - Ramp circuit
- O Playback system
 - Feedback damping provided in the playback amplifier facilitates circuit board design.
 - Middle-frequency tuner on chip; EVR permits independent adjustment of f_0 , Q and boost
 - RF AGC and dropout detection circuit

Structure

Bipolar silicon monolithic IC



Absolute Maximum Ratings (Ta=25°C)

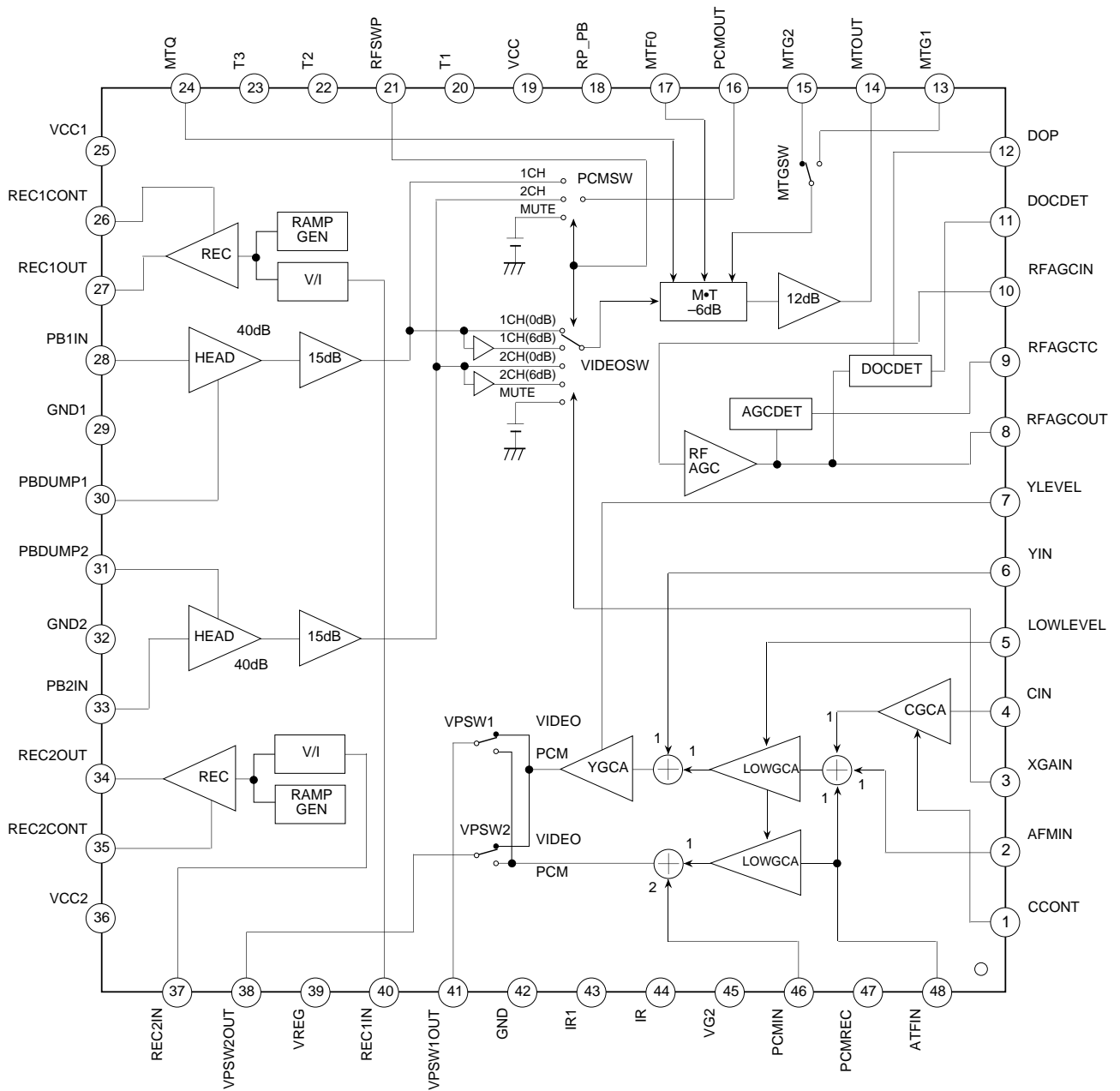
• Supply voltage	V _{CC}	7	V
• Operating temperature	T _{opr}	-10 to +75	°C
• Storage temperature	T _{stg}	-65 to +150	°C
• Allowable power dissipation	P _D	1100	mW
		(when board is mounted)	

Operating Conditions

Supply voltage	V _{CC}	4.75	+0.5 -0.25	V
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Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	CCONT	—		<p>EVR adjustment of recording chroma level.</p> <p>Gain is small when the applied voltage is large.</p>
2	AFMIN	—		<p>Recording AFM input.</p> <p>DC is cut off by internal capacitor.</p> <p>Input level is 125 mVp-p (typ.).</p> <p>When not used, connect this pin to Vcc.</p>
3	XGAIN	—		<p>VIDEO SW gain switch.</p> <p>Low : 6 dB</p> <p>High : 0 dB</p>
4	CIN	2.4 V		<p>Recording chroma input.</p> <p>Input the signal with capacitor coupling.</p> <p>Input level is 300 mVp-p (typ.).</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
5	LOW LEVEL	—		<p>EVR adjustment of recording RF signal level.</p> <p>Gain is small when the applied voltage is large.</p> <p>Adjusts both the VIDEO path and the PCM path simultaneously.</p> <p>VIDEO path: Adjustment of C + AFM + ATF</p> <p>PCM path: Adjustment of ATF</p>
6	YIN	24V		<p>Recording Y signal input.</p> <p>Input the signal with capacitor coupling.</p> <p>Input level is 500 mVp-p (typ.).</p>
7	YLEVEL	—		<p>EVR adjustment of recording Y signal level.</p> <p>The Y LEVEL is small when the applied voltage is large.</p>
8	RFAGCOUT	2.8 V		<p>Playback Y signal output.</p> <p>Output level is 380 mVp-p (typ.).</p>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
9	RFAGCTC	—		RF AGC time constant.
10	RFAGCIN	—		RF AGC input of playback Y level. The playback video signal output from Pin 14 (MTOUT) passes through an external ATF TRAP, AFM TRAP, and C TRAP, and is then input to Pin 10 (RFAGCIN) again. DC is cut off by internal capacitor. When not used, connect this pin to Vcc.
11	DOCDT	25V		Determines the dropout detection level.
12	DOP	H: 3.1 V L: 0 V		Dropout detection signal output. Goes high when a dropout is detected.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13	MTG1	—		REVR adjustment of channel 1 middle-frequency tuner boost. Boost is small when the applied voltage is large.
14	MTOUT	24V		Playback VIDEO output. Y + C + AFM + ATF is output.
15	MTG2	—		EVR adjustment of channel 2 middle-frequency tuner boost. Boost is small when the applied voltage is large.
16	PCMOUT	2 V		Playback PCM output.
17	MTF0	—		EVR adjustment that determines f_0 of the middle-frequency tuner. f_0 is large when the applied voltage is large.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18	RP_PB	—		REC/PB switch. High : PB Low : REC
19	VCC	4.75V		Power supply for sections other than the REC amplifier and the PB amplifier.
20	T1	—		Connect to GND.
21	RFSWP	—		RFSWP input.
22	T2	—		Connect to GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
23	T3	—		Connect to GND.
24	MTQ	—		EVR adjustment that determines Q of the middle-frequency tuner. Q is large when the applied voltage is large.
25	VCC1CH	4.75V	—————	Channel 1 power supply.
26	REC1CONT	—		EVR adjustment of recording channel 1 damping Damping is applied strongly when the applied voltage is small.
27	REC1CONT	—		Recording channel 1 output. Open collector.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	PB1IN	0.7V		Playback channel 1 input.
29	GND1CH	0 V	—————	Channel 1 GND.
30	PBDUMP1	2.5 V		The playback channel 1 damping is determined by the external resistance. Damping is applied strongly when the resistance is large.
31	PBDUMP2	2.5 V		The playback channel 2 damping is determined by the external resistance. Damping is applied strongly when the resistance is large.
32	GND2CH	0 V	—————	Channel 2 GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
33	PB2IN	0.7V		Playback channel 2 input.
34	REC2OUT	—		Recording channel 2 output. Open collector.
35	REC2CONT	—		EVR adjustment of recording channel 2 damping. Damping is applied strongly when the applied voltage is small.
36	VCC2CH	4.75 V	—————	Channel 2 power supply.
37	REC2IN	2.4 V		Channel 2 recording amplifier input. DC cut-off is applied to the Pin 38 signal by external capacitor, and then the resulting signal is input.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	VPSW2OUT	2.4 V		Recording channel 2 VPSW output. Output level is 200 mVp-p (typ.).
39	VREG	4.15 V		4.15 V regulator output.
40	REC1IN	2.4 V		Channel 1 recording amplifier input. DC cut-off is applied to the Pin 41 signal by external capacitor, and then the resulting signal is input.
41	VPSW1OUT	2.4 V		Recording channel 1 VPSW output. Output level is 200 mVp-p (typ.).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	GND	0 V		GND for sections other than the REC amplifier and the PB amplifier.
43	IR1	1.9 V		Determines the REC amplifier gain. Generates the reference current when 15 k Ω resistance is inserted to GND. Insert 18 k Ω resistance to GND.
44	IR	1.9 V		Generates the reference current for the middle-frequency tuner, dropout detection circuit, and the ramp.
45	VG2	2.45 V		2.45 V internal reference voltage source.
46	PCMIN	2.4 V		Recording PCM input. Input the signal with capacitor coupling. Input level is 300 mVp-p (typ.).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	PCMREC	—		PCM recording switch. PCM recording is selected when high.
48	ATFIN	2.4 V		Recording ATF input. Input the signal with capacitor coupling. Input level is 125 mVp-p (typ.).

(V_{CC} = 4.75 V, T_a = 25°C ; Refer to the Electrical Characteristics Measurement Circuit.)

Electrical Characteristics

No.	Item	Symbol	Measurement conditions			Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input conditions		Control logic						
			Input pin	Level							
1	Current consumption for recording	I _{rec}	—	—	A	Measure the current consumption for two-channel recording (includes bias current).	44	63	82		
2	Recording amplifier bias current	I _{b1} , I _{b2}	—	—	A	Measure the DC current.	14.55	18.8	23.05	mA	
3	Current consumption for playback	I _{pb}	—	—	D	Measure the current consumption for two-channel playback.	24	35	46		
4	V _{reg} pin voltage	—	—	—	A	Measure the pin voltage.	3.95	4.15	4.35	V	
5	V _{g2} pin voltage	—	—	—	A	Measure the pin voltage.	2.30	2.45	2.60		
6	YGCA minimum gain	G _{ym} min	6	500mVp-p	A	Pin 7 YLEVEL = V _{CC}	—	- 15.8	- 14.1		
7	YGCA center gain	G _{yc} en	6	500mVp-p	A	Adjust Pin 7 YLEVEL so that the output is 200 mVp-p (V _{ylev}).	—	- 8	—		
8	YGCA maximum gain	G _{ym} ax	6	200mVp-p	A	Pin 7 YLEVEL = 1.8 V	- 2.2	- 1.1	—		
9	YGCA frequency response (center gain)	ΔY	6	500mVp-p	A	Level at 14 MHz/level at 300 kHz YLEVEL = V _{ylev}	- 1.5	- 0.8	0		
10	YGCA secondary distortion center gain	DY	6	500mVp-p	A	YLEVEL = V _{ylev}	—	- 53	—		
11	Low-frequency GCA (VIDEO path) minimum gain	G _{lv} min	2	125mVp-p	A	Pin 5 LOWLEVEL = V _{CC} YLEVEL = V _{ylev}	—	- 32.0	- 26.0		
12	Low-frequency GCA (VIDEO path) center gain	G _{lv} cen	2	125mVp-p	A	Adjust Pin 5 LOWLEVEL so that the output is 12.5 mVp-p (V _{ylev}). YLEVEL = V _{ylev}	—	- 20	—	dB	
13	Low-frequency GCA (VIDEO path) maximum gain	G _{lv} max 2	2	125mVp-p	A	Pin 5 LOWLEVEL = 1.8 V YLEVEL = V _{ylev}	- 14.0	- 12.4	—		
14	Low-frequency GCA (VIDEO path) maximum gain	G _{lv} max	48	125mVp-p	A	Pin 5 LOWLEVEL = 1.8 V YLEVEL = V _{ylev}	- 14.0	- 12.4	—		
15	Low-frequency GCA (PCM path) minimum gain	G _{lp} min	48	125mVp-p	A	Pin 5 LOWLEVEL = V _{CC} YLEVEL = V _{ylev}	—	- 32.0	- 26.0		

* For details on the control logic, refer to the Control Logic Truth Table.

No.	Item	Symbol	Measurement conditions				Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input conditions		Control logic							
			Input pin	Level		Frequency						
16	Low-frequency GCA (PCM path) maximum gain	G _{lp}	48	125mVp-p	100kHz	A	Pin 5 LOWLEVEL = 1.8 V YLEVEL = V _{ylev}	-14.0	-12.4	—		
17	Chroma GCA minimum gain	G _{cmin}	4	300mVp-p	300kHz	A	Pin 1 CCONT = V _{cc} YLEVEL = V _{ylev} , LOWLEV = V _{llev}	—	-24.0	-21.6		
18	Chroma GCA center gain	G _{ccen}	4	300mVp-p	300kHz	A	Adjust Pin 1 CCONT so that the output is 50 mVp-p (V _{clev}) YLEVEL = V _{ylev} , LOWLEV = V _{llev}	—	-15.6	—		
19	Chroma GCA maximum gain	G _{cmax}	4	300mVp-p	300kHz	A	Pin 1 CCONT = 1.8 V YLEVEL = V _{ylev} , LOWLEV = V _{llev}	-13.3	-11.0	—		
20	Chroma GCA frequency response (center gain)	ΔC	4	300mVp-p	2MHz 300kHz	A	Level at 2 MHz/level at 300 kHz YLEVEL = V _{ylev} , LOWLEV = V _{llev}	-0.5	0	+0.5	dB	
21	Chroma GCA center gain secondary distortion	DC	4	300mVp-p	2MHz	A	YLEVEL = V _{ylev} , LOWLEV = V _{llev}	—	-50	—		
22	PCM main path gain	G _p	46	300mVp-p	300kHz	B, C		-4.5	-3.5	-2.5		
23	PCM main path frequency response	ΔP	46	300mVp-p	300kHz	B, C	Level at 14 MHz/level at 300 kHz	-1.5	-0.8	0		
24	PCM main path secondary distortion	DP	46	300mVp-p	7MHz	B, C		—	-55	—		
25	Recording amplifier output current	I _{r1} , I _{r2}	40, 37	200mVp-p	1MHz	A	REC1CONT, REC2CONT = 3.3 V Output level (V)/51 (Ω)	17.7	20.0	22.3	mAp-p	
26	Recording amplifier frequency response	Δr1, Δr2	40, 37	200mVp-p	10MHz 1MHz	A	Level at 10 MHz/level at 1 MHz	—	-0.2	—		
27	PBMTOUT gain (XGAIN = high)	G _{mt1}	28, 33	200μVp-p	300kHz	D, E	MTG1, MTG2 = V _{cc}	57.5	61.0	64.5	dB	
28	PBMTOUT gain (XGAIN = low)	G _{mt2}	28, 33	200μVp-p	300kHz	F, G	↓	63.5	67.0	70.5	dB	
29	PBPCMOUT gain	G _{pcm}	28, 33	200μVp-p	300kHz	D, E		57.5	61.0	64.5	dB	
30	RFAGC standard output	V _{agc1}	10	224mVp-p	7MHz	D	Measure the output level.	335	380	420	mVp-p	
31	Cover range high	V _{agc2}	10	50mVp-p	7MHz	D		305	345	—		
32	Cover range low	V _{agc3}	10	1.2Vp-p	7MHz	D		—	420	530		

No.	Item	Symbol	Measurement conditions			Measurement pin or ammeter name	Measurement method	Min.	Typ.	Max.	Unit
			Input pin	Level	Frequency						
33	Dropout detection ON level	Kdop-on	Refer to the measurement method (diagram at right).		D	12		-15.0	-12.0	-9.0	dB
34	Dropout detection OFF level	Kdop-off			D	12					
35	Dropout pulse low level	Vdop-l			D	12		0	0.01	0.2	V
36	Dropout pulse high level	Vdop-h			D	12		2.9	3.1	3.3	
37	Dropout ON detection time	Tdop-on	Refer to the measurement method (diagram at right).		D	12		—	1	—	µs
38	Dropout OFF detection time	Tdop-off			D	12			2	—	

Control Logic Truth Table

Input conditions and operation	Control logic input conditions				Operation of each section for the input conditions shown at left								Operation	Mode		
					Recording system				Playback system							
	RP_PB Pin 18	RFSWP Pin 21	PCMREC Pin 47	XGAIN Pin 3	VPSW1OUT Pin 41	VPSW2OUT Pin 38	REC1OUT Pin 27	REC2OUT Pin 34	PB 1chAmp	PB2chAmp	PCMOUT Pin 16	MTOUT Pin 14			RFAGCOUT Pin 8	Dropout detection circuit
A	L	—	L	—	V	V	V	V	X	X	X	X	X	X	VIDEO REC	REC
B	L	L	H	—	P	V	P	V	X	X	X	X	X	X	PCM REC	
C	L	H	H	—	V	P	V	P	X	X	X	X	X	X	↓	
D	H	L	L	H	X	X	X	X	O	O	CH1	CH2	O	O	PB	PB
E	H	H	L	H	X	X	X	X	O	O	CH2	CH1	O	O	↓	
F	H	L	L	L	X	X	X	X	O	O	CH1	CH2	O	O	↓	
G	H	H	L	L	X	X	X	X	O	O	CH2	CH1	O	O	↓	

Explanation of input conditions:

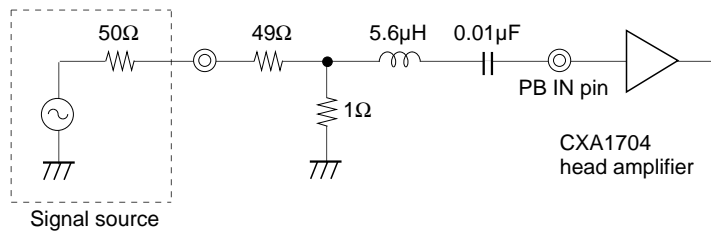
- H : Control logic input voltage is 2.3 V or more.
- L : Control logic input voltage is 0.6 V or less.
- : Don't care.

Explanation of operation symbols:

- O : Operates.
- V : VIDEO signal is selected.
- X : Does not operate.
- P : PCM signal is selected.
- CH1 : CH1 signal is output.
- CH2 : CH2 signal is output.

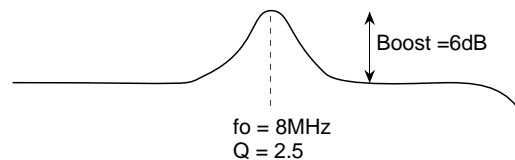
Explanation of Measurement Methods

Playback system signal input method

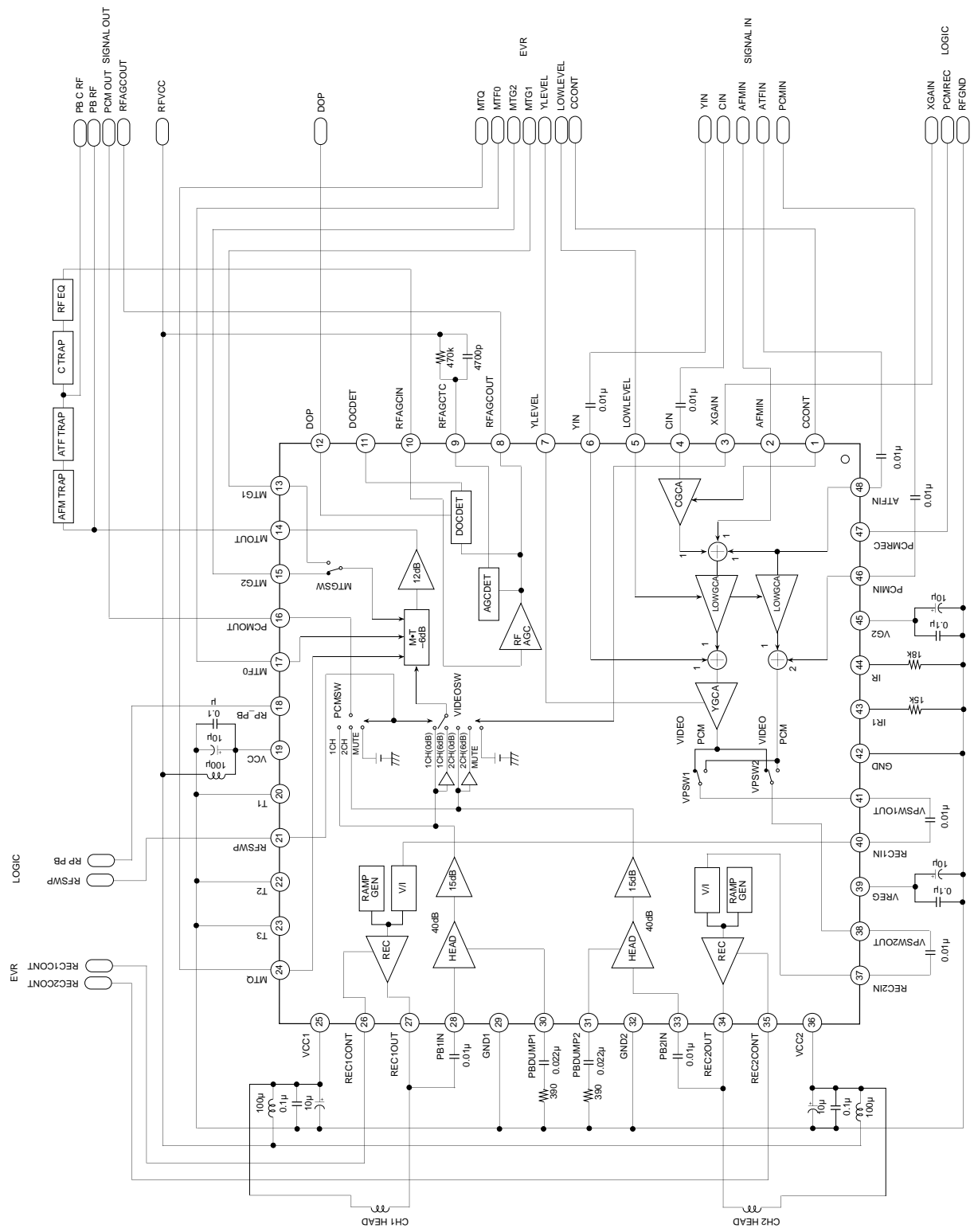


Middle-frequency tuner measurement method

As shown in the diagram at right, assume $f_0 = 8$ MHz, $Q = 2.5$, and the boost = 6 dB as the center conditions. Fix two of them at their respective center condition, and apply the EVR control of the adjustment item to measure the adjustment range.



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Description of Operation

<Recording level adjustment + SW>

After the recording level is adjusted so that the current level of the Y, chroma, AFM, ATF, and PCM signals are suitable at the head, the VIDEO + ATF and PCM + ATF signals are created and output to the CH1 and CH2 output pins with the proper timing.

The Y level adjustment is made by Pin 7 (YLEVEL), the low frequency level adjustment is made by Pin 5 (LOWLEVEL), and the chroma level adjustment is made by Pin 1 (CCONT). LOWGCA for the VIDEO path and the PCM path is also adjusted accordingly.

The gain values shown in the specifications are all I/O gain values.

<Recording amplifier>

This performs V/I conversion on the signal for which the recording level was adjusted and drives the head. Feedback damping, which is used to suppress head resonance, is performed using EVR adjustment with Pin 26 (REC1CONT) and Pin 35 (REC2CONT).

Be careful to avoid capacitance coupling between the inputs and the outputs.

<Head amplifier>

This amplifies the playback signal from the head with low noise and high gain. Feedback damping circuit to suppress head resonance is built in; the damping can be adjusted through external resistance connected to Pin 30 (PBDUMP1) and Pin 31 (PBDUMP2).

Be careful to avoid capacitance coupling between the playback system outputs and the head amplifier inputs.

<Middle-frequency tuner + SW>

This compensates for the frequency response of the playback signal. EVR adjustment of the center frequency is performed with Pin 17 (MTF0); of Q with Pin 24 (MTQ), and of the CH1 and CH2 boost with Pin 13 (MTG1) and Pin 15 (MTG2), respectively.

The CH1 and CH2 signals are switched according to the RFSWP timing and are output to MTOUT and PCMOUT. The gain of the MTOUT signal is switched between 0 dB and 6 dB by Pin 3 (XGAIN).

<RFAGC>

This outputs the playback VIDEO signal at a fixed 380 mVp-p. The input has a built-in capacitor for DC cut-off and external capacitor is not required.

The detector input includes an HPF with a cut-off frequency of approximately 1 MHz, so that the gain in the bandwidth corresponding roughly to the Y signal is detected.

<Dropout detection>

A dropout is detected in the playback video signal, and a dropout pulse is output. The detection level is set to the optimum level based on a 224 mVp-p input as a reference.

<Control logic block>

In order to save power consumption, this IC is designed to reduce power supplied to those circuit blocks that are not operating. Therefore, power saving operation is executed automatically when all of the power supplies are turned on. In addition, this IC is equipped with many I/O switching circuits that must be switched with very complex timing, so that internal logic is provided to control them.

The combinations of input and output in basic operations are as shown in the Control Logic Truth Table.

<Reference voltage in the IC>

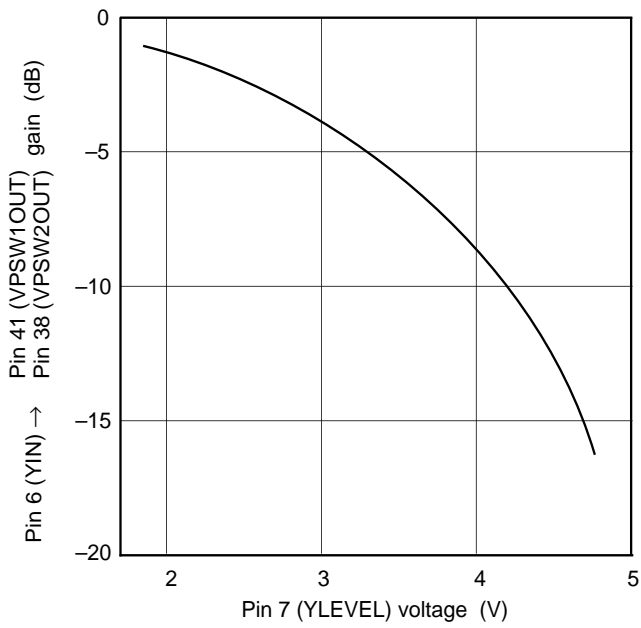
Vreg (4.15 V) and Vg2 (2.45 V) are generated as the reference voltages used in the IC. Do not use these as external power supplies because they could cause cross talk in the IC.

<EVR adjustment>

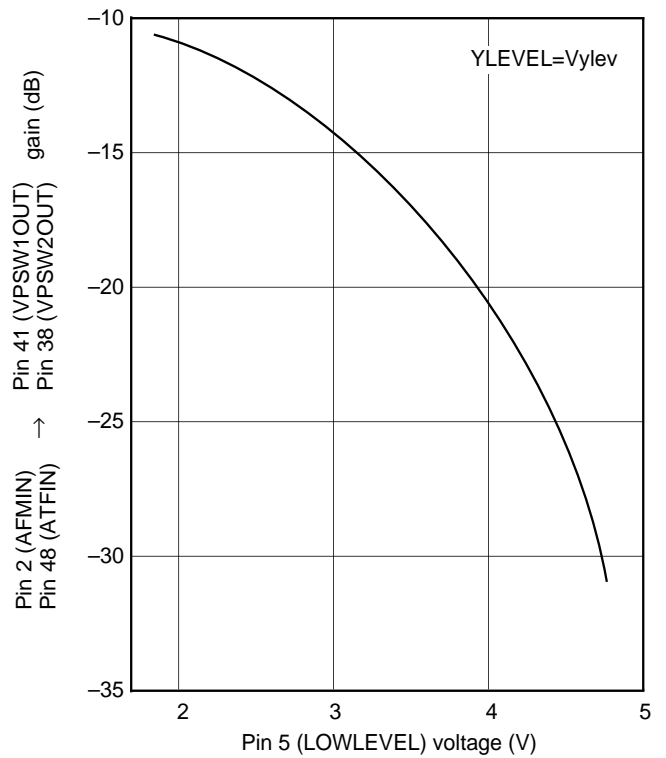
The voltage applied to the EVR adjustment pin is Vcc- variable, ranging from 1.8 V to Vcc.

Recording Level Adjustment

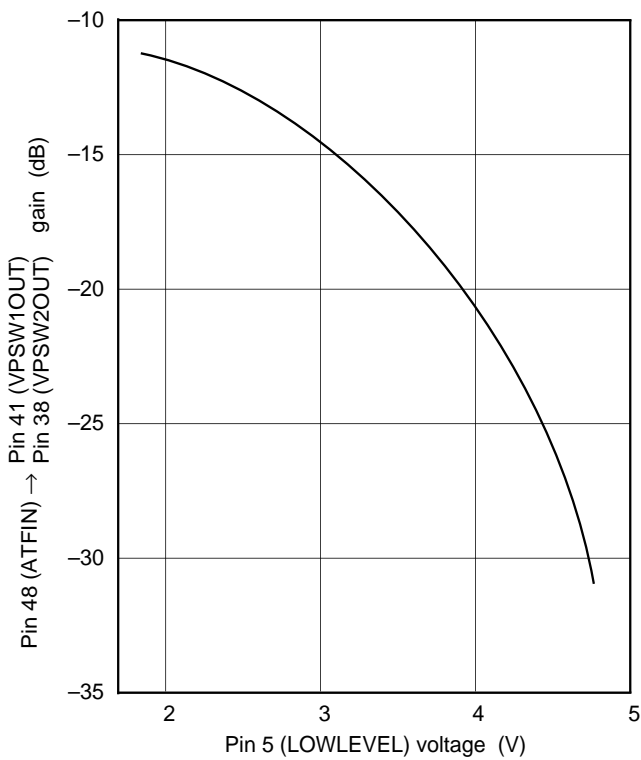
YGCA gain control



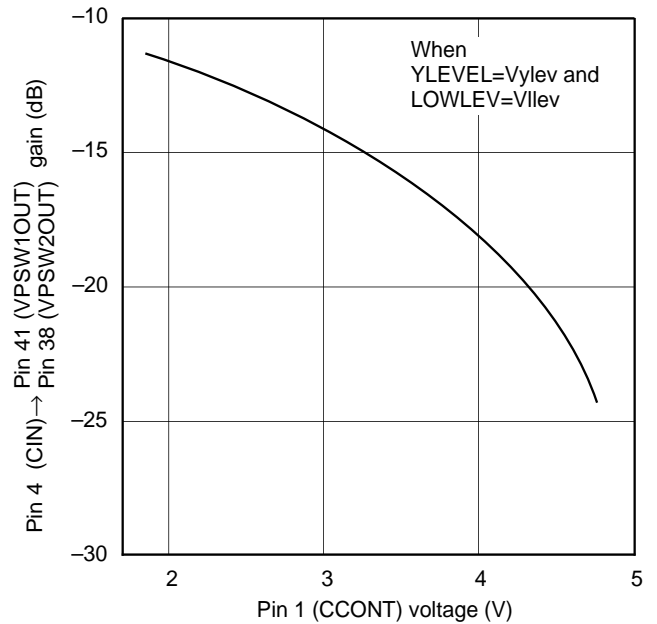
LOWGCA (Video path) gain control



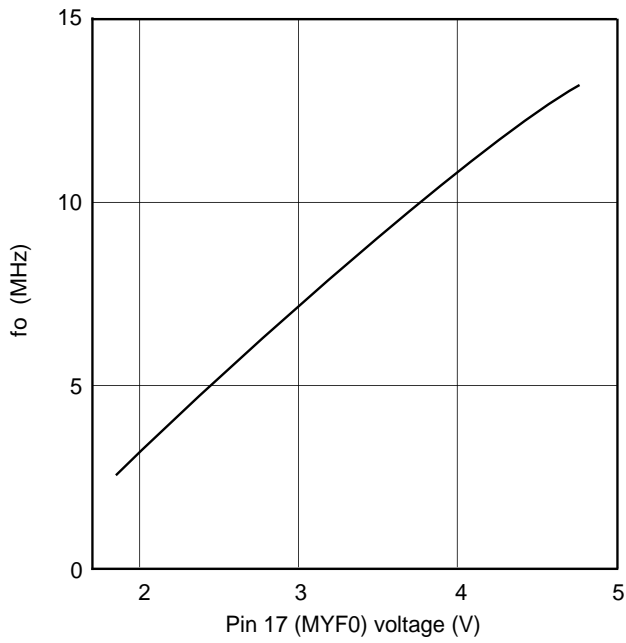
LOWGCA (PCM path) gain control



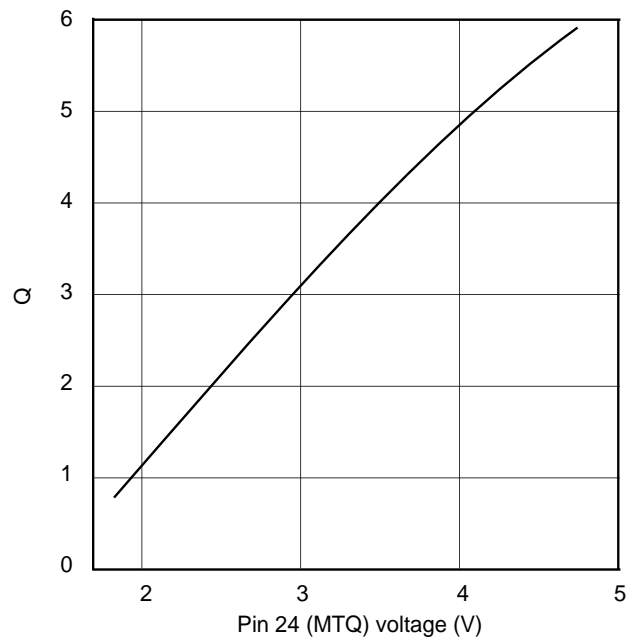
CGCA gain control



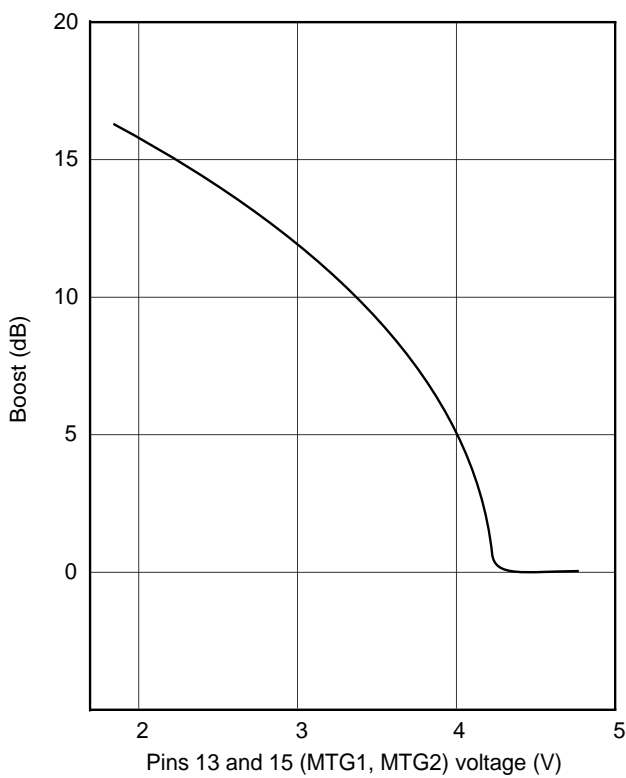
Middle-frequency tuner fo control



Middle-frequency tuner Q control

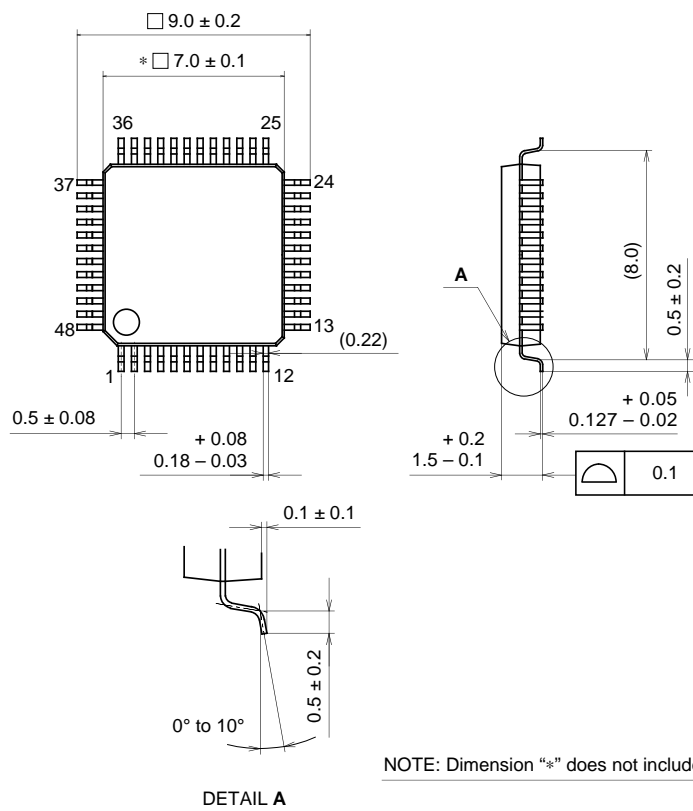


Middle-frequency tuner boost control



Package Outline Unit : mm

48PIN LQFP (PLASTIC)



SONY CODE	LQFP-48P-L01
EIAJ CODE	*QFP048-P-0707-A
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g



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