SONY

CXA1779P

Predriver for High Resolution Computer Displays

Description

The CXA1779P is a bipolar IC developed for high resolution computer displays.

Features

- Wide bandwidth (150MHz/–3dB typ.)
- RGB single package
- Permits RGB common and independent contrast control
- Permits RGB independent pedestal level control
- Input D-range: 0.7Vp-p (min.)

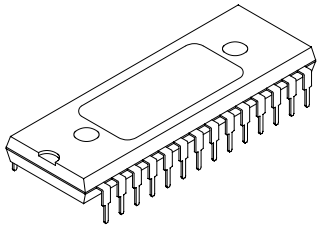
Applications

High resolution computer displays

Structure

Bipolar silicon monolithic IC

28 pin DIP (Plastic)



Absolute Maximum Ratings

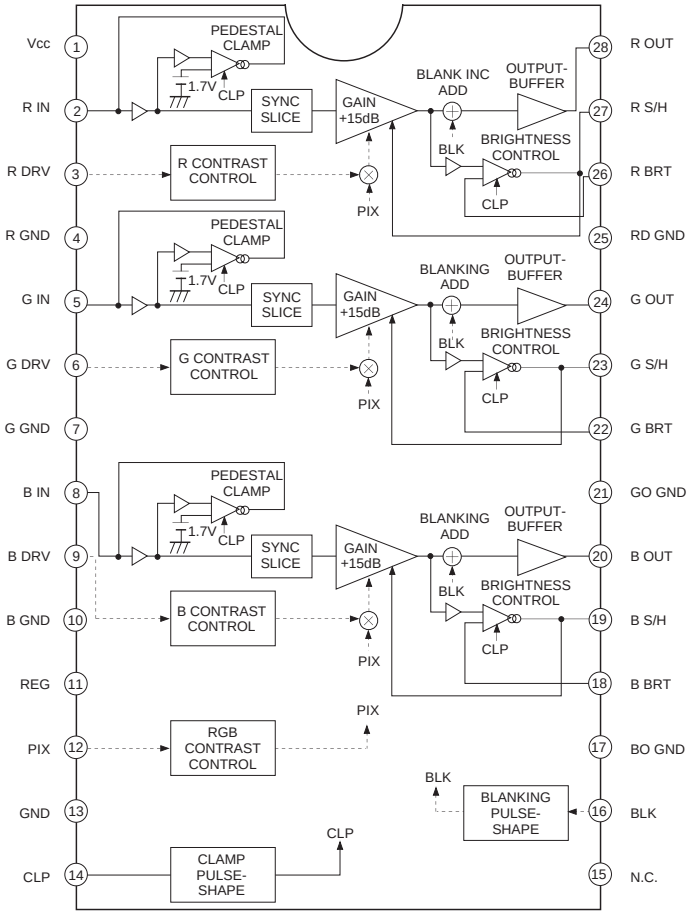
• Supply voltage	Vcc	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2.8	W

Recommended Operating Conditions

Supply voltage	Vcc	12 ± 0.6	V

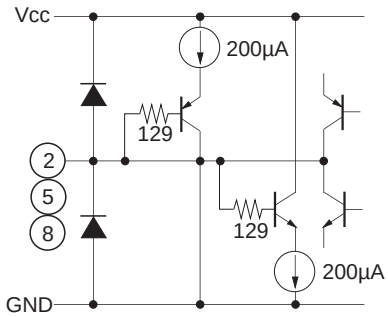
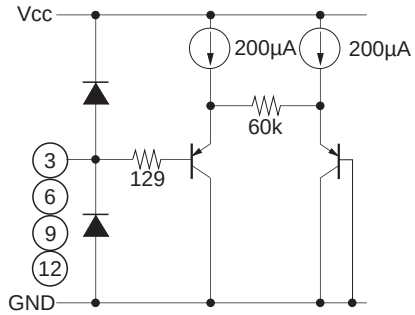
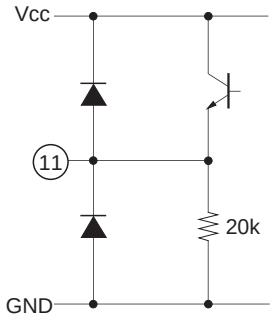
Block Diagram and Pin Configuration

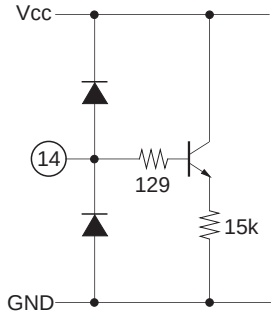
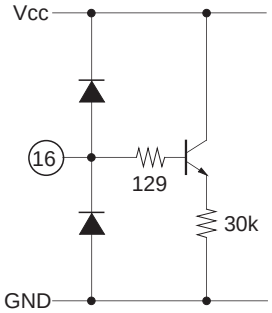
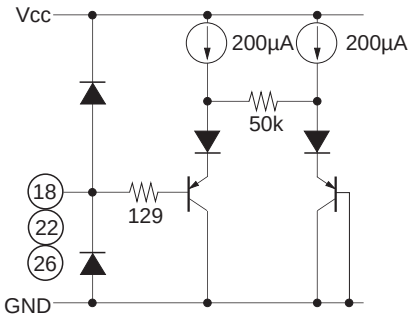
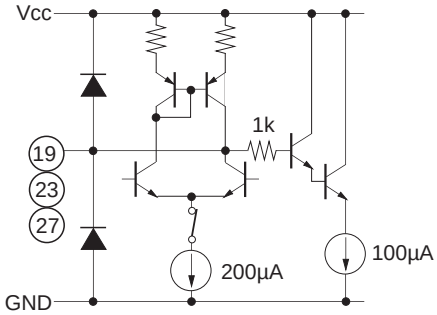
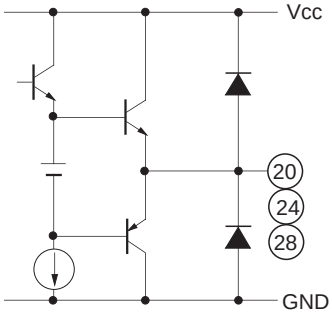
(Top View)



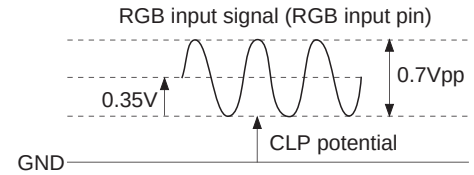
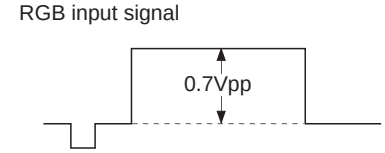
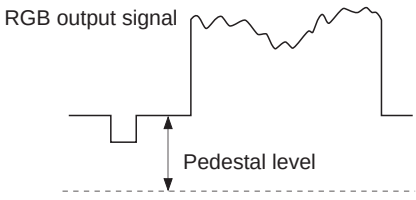
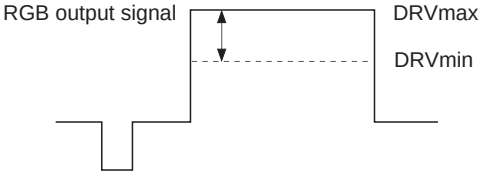
E94510-ST

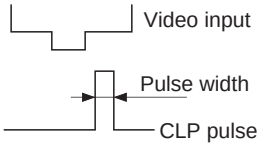
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	Vcc	12V		Power supply pin.
2	R IN	3.0V		RGB input pins. The pedestal level of the input signal is 3.0V during clamping. Connect 0.01µF in series as the clamping capacitor.
5	G IN			
8	B IN			
3	R DRV	—		RGB contrast adjustment pins. The variable range of the pin voltages is from 0 to 5V.
6	G DRV			
9	B DRV			
12	PIX			RGB simultaneous contrast adjustment pin. The variable range of the pin voltage is from 0 to 5V.
4	R GND	0V		GND pins for the input amplifier block.
7	G GND			
10	B GND			
11	REG	5V		• Internal regulator stabilizing pin. • 5V regulator output pin. • Attaches the decoupling capacitance (0.01µF).
13	GND	0V		GND pin.
17	BO GND	0V		GND pins for the output stage buffer amplifier block.
21	GO GND			
25	RO GND			

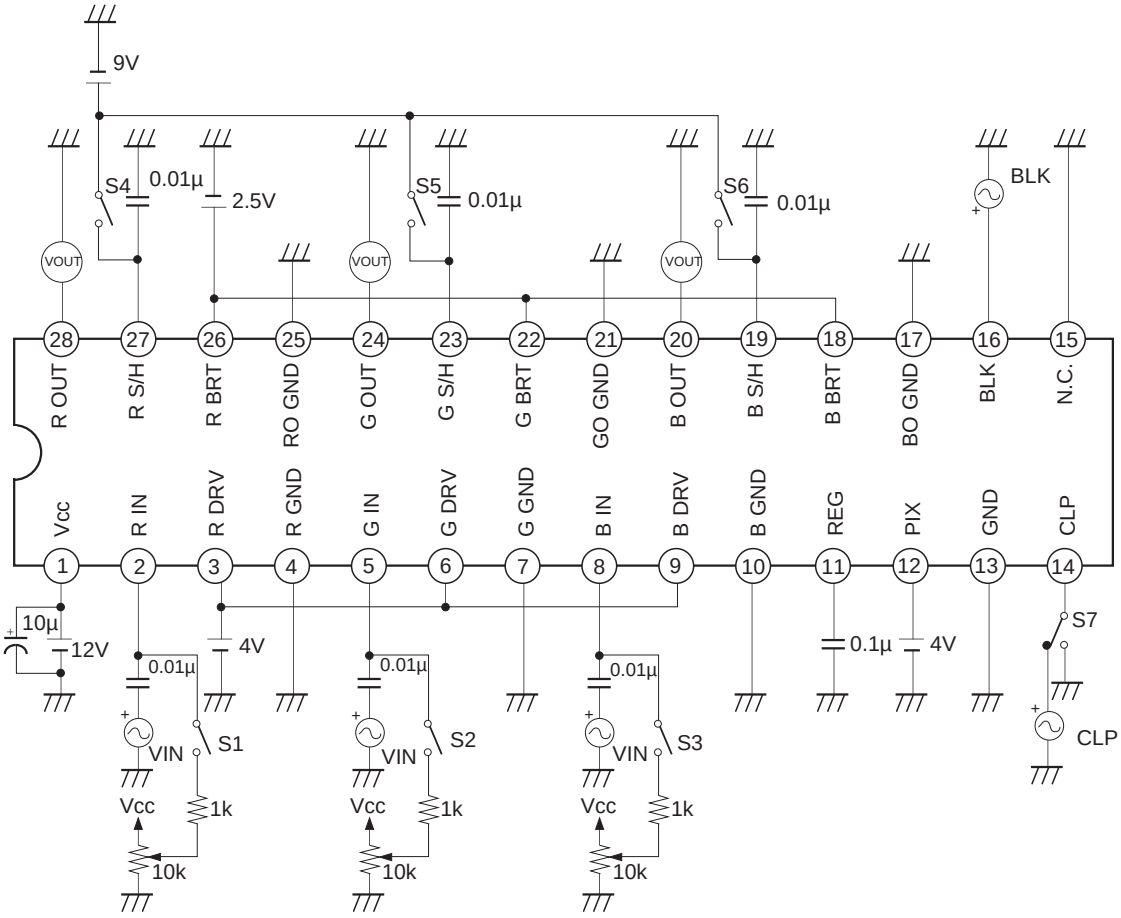
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	CLP	—		• Clamp pulse input pin. • Turns the input clamp and the bright level adjustment circuit on and off when high. V_H = 3V V_L = 1.5V
15	N.C.	—		Leave this pin open. Connect to GND.
16	BLK	—		• Blanking pulse input pin. • Threshold level at approximately 2.25V. V_H = 3V V_L = 1.5V
18	B BRT	—		RGB bright level adjustment pins. The variable range of the pin voltages is from 0 to 5V.
22	G BRT			
26	R BRT			
19	B S/H			Pins to externally attach the sample-and-hold capacitor (0.01µF).
23	G S/H			
27	R S/H			
20	B OUT			RGB output pins.
24	G OUT			
28	R OUT			

Electrical Characteristics (Ta = 25°C, Vcc = 12V, See Electrical Characteristics Measurement Circuit.)

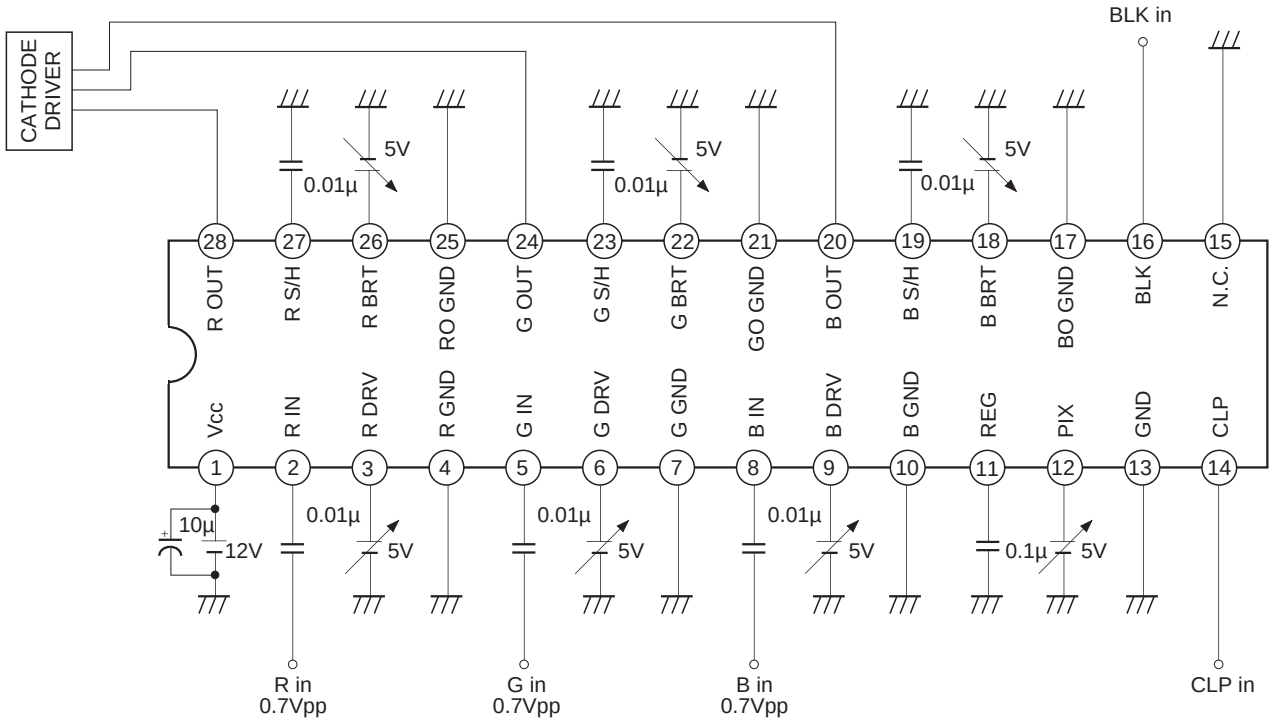
No.	Item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
1	Current consumption	Icc	S1 to S7: OFF Input signal: None	50	88	120	mA
2	Frequency response	f_{100MHz}	S1 to S7: ON Input continuous 1MHz and 100MHz sine waves at 0.7Vp-p, and measure the gain difference of the output amplitudes. Gain difference [dB] = $20\log\left(\frac{V_{OUT}\ 100M}{V_{OUT}\ 1M}\right)$ 	–3	–1.5	—	dB
3	Contrast control	$CONT_{MAX}$	S1 to S7: OFF Input video signal 0.7Vp-p and measure output signal amplitude V_{OUT}. Calculate the contrast gain from this V_{OUT}. $CONT_{MAX}$ [dB] = $20\log\left(\frac{V_{OUT}}{0.7}\right)$  Measuring is possible with or without a sync signal.	13	14	—	dB
4	Brightness control	BRTmax	S1 to S7: OFF CLP pulse width: 300ns Measure the pedestal level of the RGB output signal.  Measuring is possible with or without a sync signal.	—	3.5	—	V
		BRTmin		—	1.9	—	
5	Sub contrast gain	DRVgain	S1 to S7: OFF Input video signal 0.7Vp-p and measure the variable width of output signal V_{OUT}. Gain difference [dB] = $20\log\left(\frac{V_{OUT}\ DRVmin}{V_{OUT}\ DRVmax}\right)$  Measuring is possible with or without a sync signal.	—	–6	—	dB

No.	Item	Symbol	Measurement contents	Min.	Typ.	Max.	Unit
6	Input D-range	D rang	S1 to S7: OFF Measure the level which maintains the output gain when the input video signal level is varied.	—	0.8	—	Vp-p
7	Minimum clamp pulse width	CLPmin	S1 to S7: OFF Measure the clamp pulse width where the pedestal level of output signal V_{OUT} does not fluctuate.  	—	300	—	ns

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Contrast control

   The contrast for RGB IN (Pins 2, 5 and 8) input signals is adjusted using a DC externally input to the PIX pin (Pin 12). In addition, the contrast for each RGB channel can be adjusted independently using a DC externally input to the DRV pins (Pins 3, 6 and 9). (See Graphs 1 and 2.)

2. Pedestal clamp and brightness control

   The pedestal clamp clamps the pedestal level when the CLP pin (Pin 14) is high. The RGB IN pin voltage at the pedestal is approximately 3.2V when the pedestal is clamped. The CLP pin threshold level is 3V for V_H and 1.5V for V_L. (See Fig. 2.)

   Using a DC externally input to the R, G and B BRT pins (Pins 26, 22 and 18), the brightness control samples and holds the pedestal with the capacitance connected to the RGB SH pins (Pins 27, 23 and 19) when the CLP pin (Pin 14) is high, thereby adjusting the pedestal level of the R, G and B channels. (See Graph 3.)

3. Blanking additional function

   Output is blanked when the BLK pin (Pin 16) is high. The BLK pin threshold level is 3V for V_H and 1.5V for V_L. See the Example of Input/Output Signals for output signal levels. The output signal is 0.3V during the blanking interval. (See Figs. 4 and 5.)

Example of Input/Output Signals

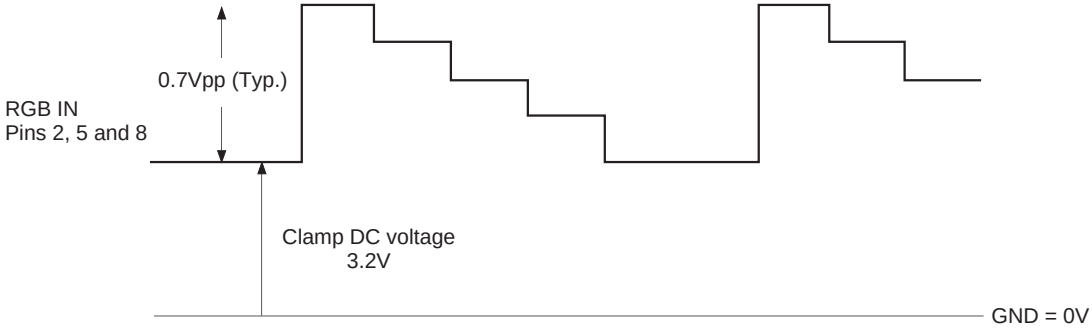
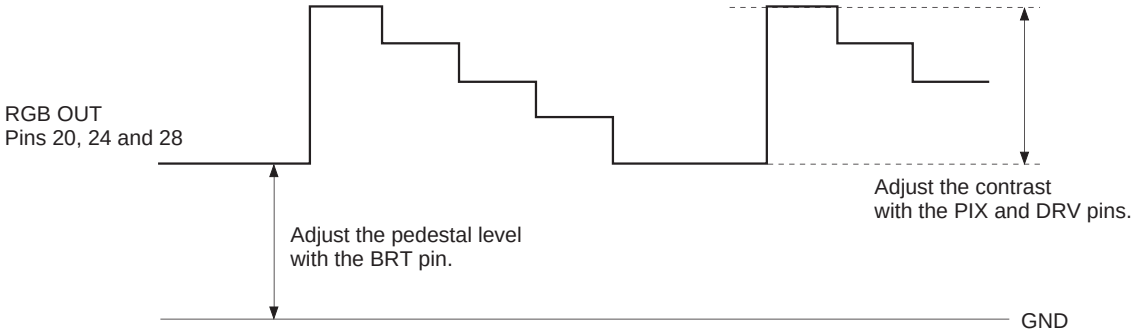


Fig. 1

Fig. 2



When a sync signal is added to the RGB input signal, after the signal is sliced into approximately 60mVp-p inside the IC, it is amplified by the gain from the PIX and DRV pins and output.

Fig. 3

Fig. 4

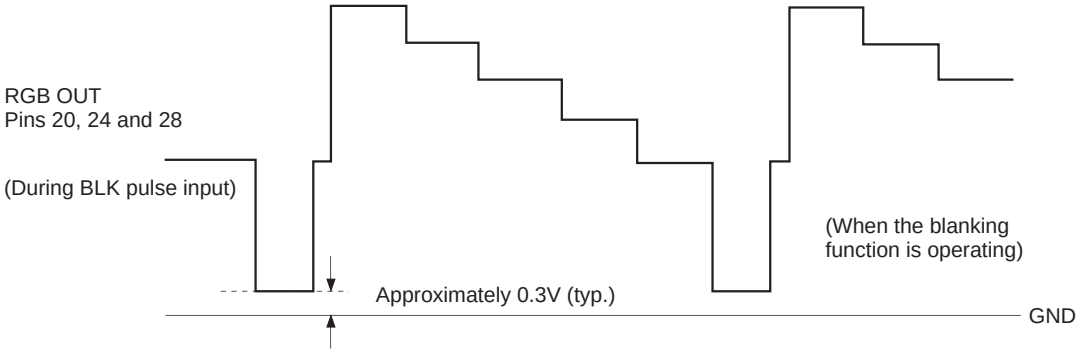
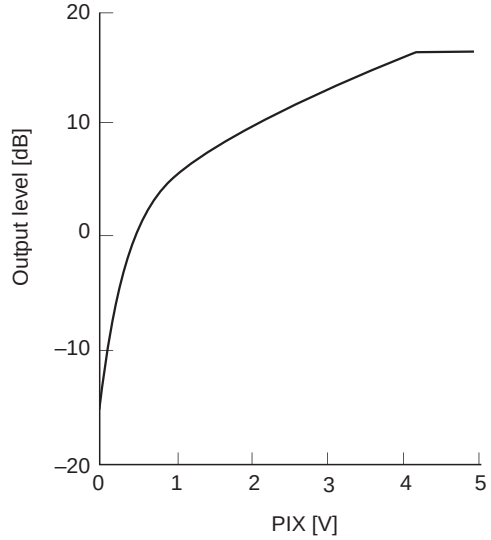


Fig. 5

Example of Representative Characteristics

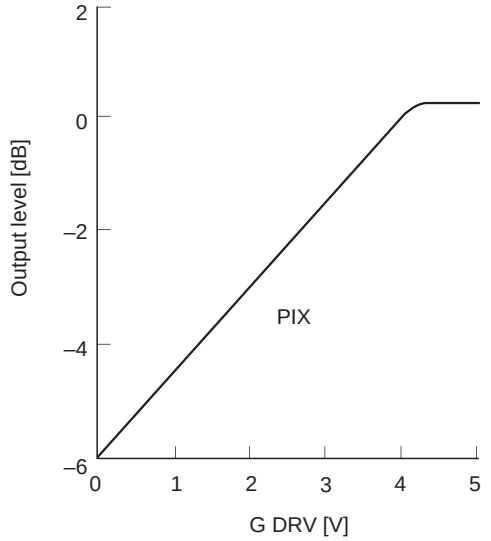
Graph 1. Contrast control (RGB common) characteristics



Input conditions for each control pin

Pin name		Pin voltage	
12	PIX	0 to 5	[V]
3	R DRV	4	[V]
6	G DRV	4	[V]
9	B DRV	4	[V]
26	R BRT	2.5	[V]
22	G BRT	2.5	[V]
18	B BRT	2.5	[V]
5	G IN	0.65	[Vpp]

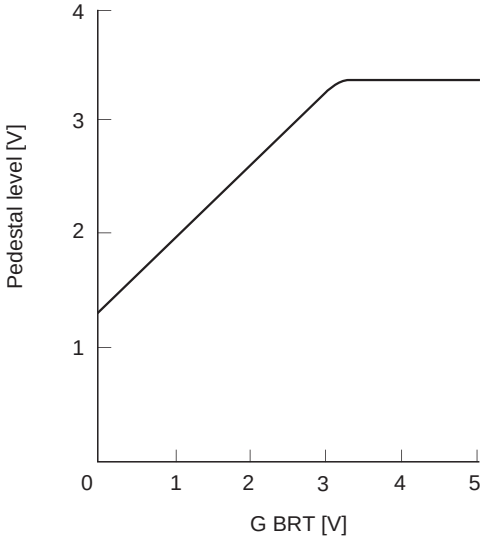
Graph 2. DRV control (RGB independent) characteristics (Gch)



Input conditions for each control pin

Pin name		Pin voltage	
12	PIX	4	[V]
3	R DRV	4	[V]
6	G DRV	0 to 5	[V]
9	B DRV	4	[V]
26	R BRT	2.5	[V]
22	G BRT	2.5	[V]
18	B BRT	2.5	[V]
5	G IN	0.65	[Vpp]

Graph 3. BRT control characteristics

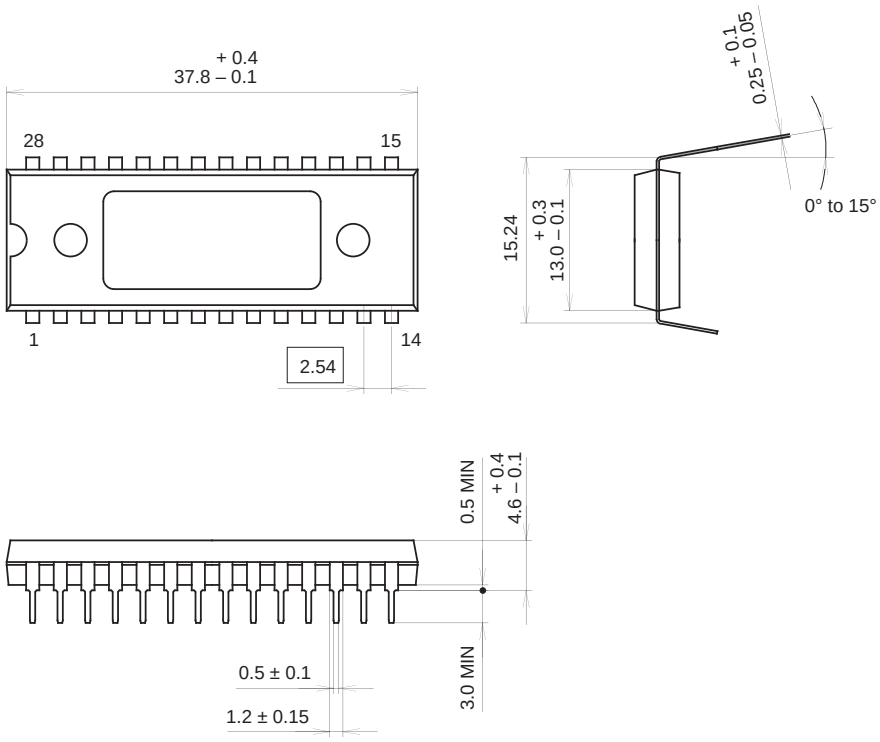


Input conditions for each control pin

Pin name		Pin voltage	
12	PIX	2.5	[V]
3	R DRV	2.5	[V]
6	G DRV	2.5	[V]
9	B DRV	2.5	[V]
26	R BRT	2.5	[V]
22	G BRT	0 to 5	[V]
18	B BRT	2.5	[V]
5	G IN	0.65	[Vpp]

Package Outline Unit: mm

28PIN DIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.Center part is mirror surface.

SONY CODE	DIP-28P-03
EIAJ CODE	DIP028-P-0600
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	4.2g

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