

10-bit 85MSPS 3-Channel D/A Converter

Description

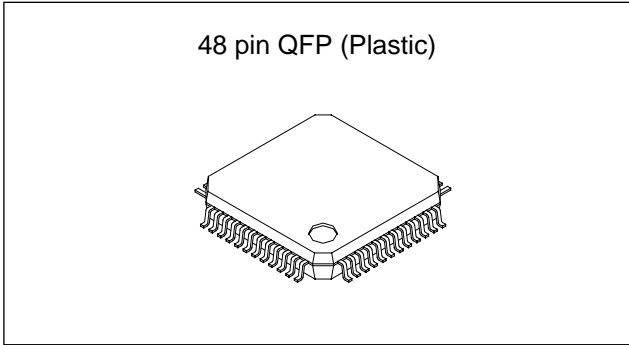
The CXD2309AQ is a 10-bit high-speed D/A converter for video band, featuring RGB 3-channel input/output. This is ideal for use in high-definition TVs and high-resolution displays.

Features

- Resolution 10-bit
- Maximum conversion speed 85MSPS
- RGB 3-channel input/output
- Differential linearity error $\pm 0.5\text{LSB}$
- Low power consumption 275mW (200 Ω load for 2Vp-p output)
- Single +5V power supply
- Low glitch
- 48-pin QFP package

Structure

Silicon gate CMOS IC



Absolute Maximum Ratings (Ta = 25°C)

- Supply voltage AVDD, DVDD 7 V
- Input voltage (All pins)

V_{IN}	$V_{DD} + 0.5$ to $V_{SS} - 0.5$	V
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- Output current IOUT 0 to 15 mA
- Storage temperature

T_{stg}	-55 to +150	°C
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Recommended Operating Conditions

- Supply voltage AVDD, AVSS 4.75 to 5.25 V
- DVDD, DVSS 4.75 to 5.25 V
- Reference input voltage

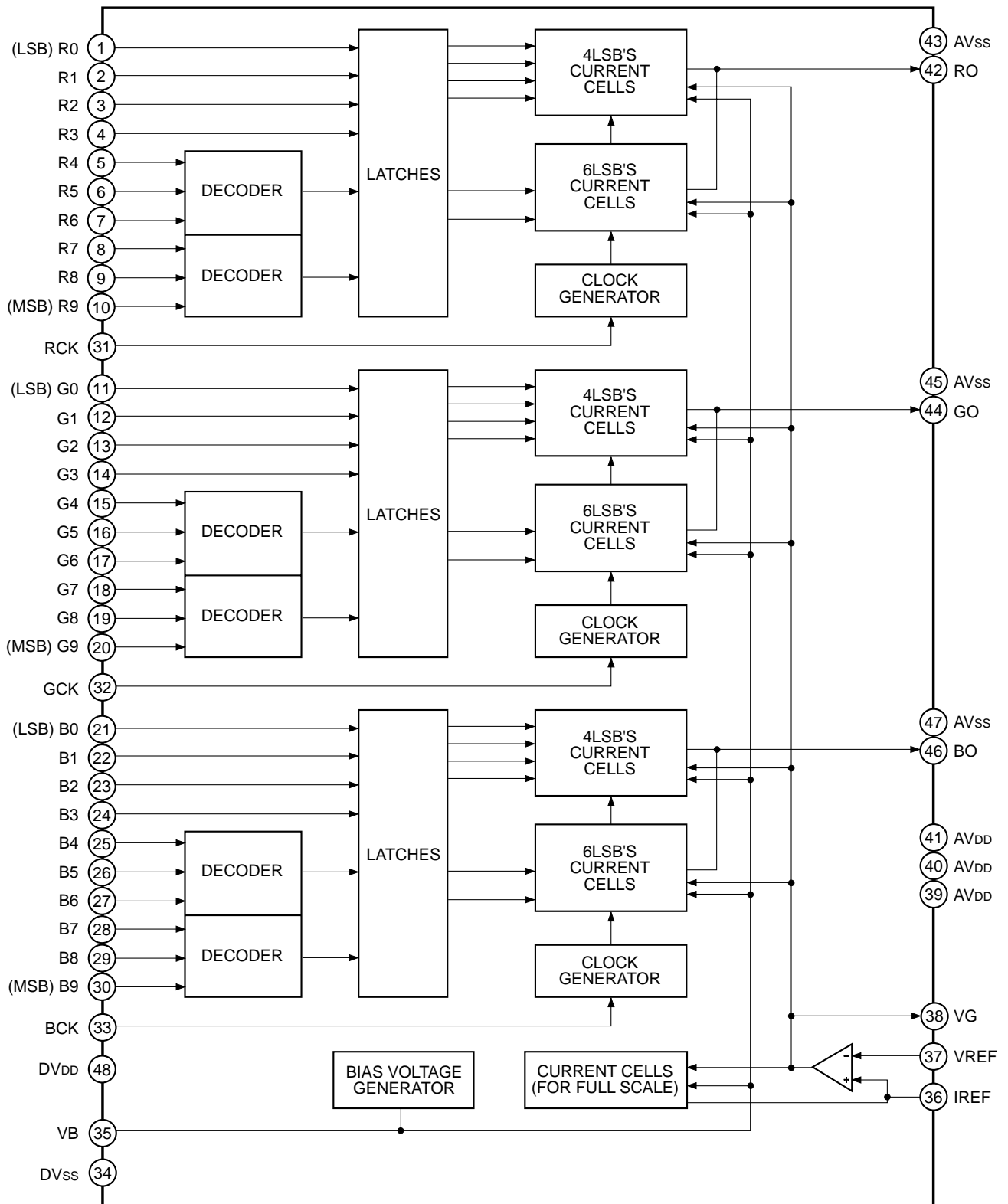
V_{REF}	1.8 to 2.0	V
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- Clock pulse width

T_{PW1}, T_{PW0}	5.2 (min.)	ns
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- Operating temperature

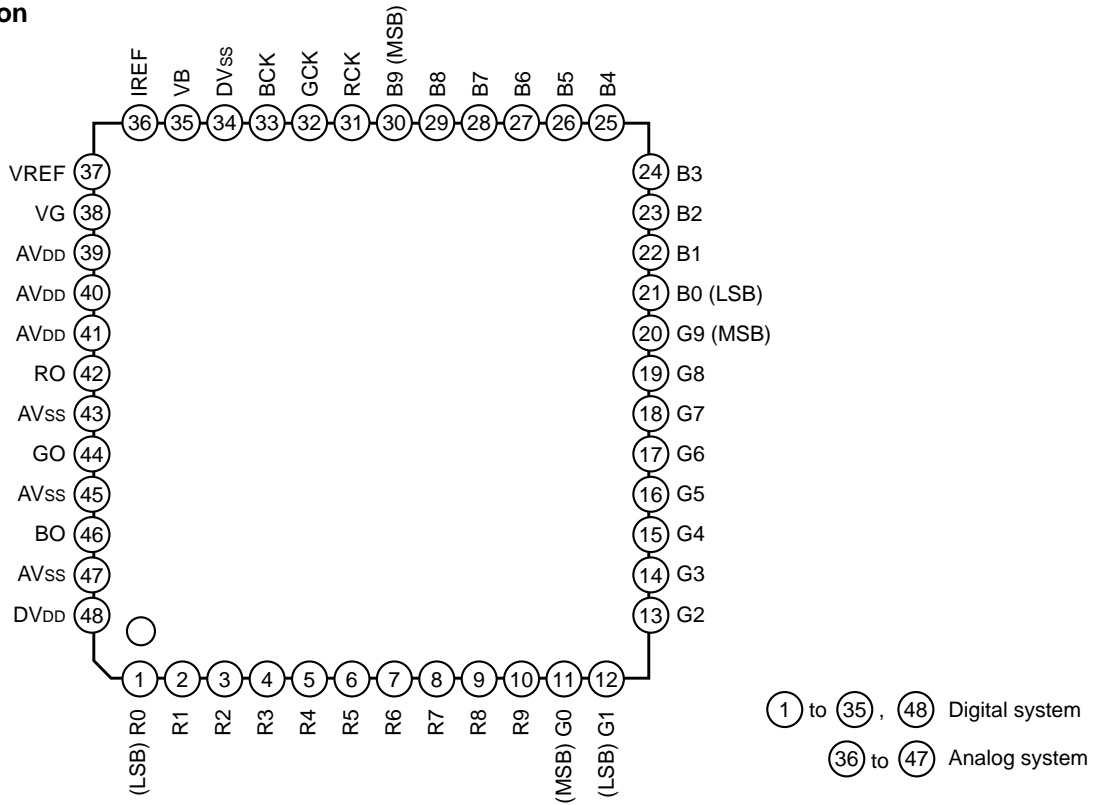
T_{opr}	-20 to +85	°C
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Block Diagram



Pin Configuration



Pin Description and Equivalent Circuit

Pin No.	Symbol	I/O	Equivalent circuit	Description
1 to 10	R0 to R9	I		Digital input. Pin 1 R0 (LSB) to Pin 10 R9 (MSB) Pin 11 G0 (LSB) to Pin 20 G9 (MSB) Pin 21 B0 (LSB) to Pin 30 B9 (MSB)
11 to 20	G0 to G9			
21 to 30	B0 to B9			
31	RCLK			
32	GCLK			
33	BCLK			
34	DVSS	—		Digital ground.
35	VB	O		Connect an approximately 0.1μF capacitor.

Pin No.	Symbol	I/O	Equivalent circuit	Description
36	IREF	O		Reference current output. Connect an "R _{IREF} " resistor which are 16 times the output resistance "R _{OUT} ".
37	VREF	I		Reference voltage input. Sets an output full-scale value.
38	VG	O		Connect an approximately 0.1μF capacitor.
39 to 41	AV _{DD}	—		Analog power supply.
42	RO	O		Current output. Output can be obtained by connecting a resistor (200Ω typ.).
44	GO			
46	BO			
43, 45, 47	AV _{SS}	—		Analog ground.
48	DV _{DD}	—		Digital power supply.

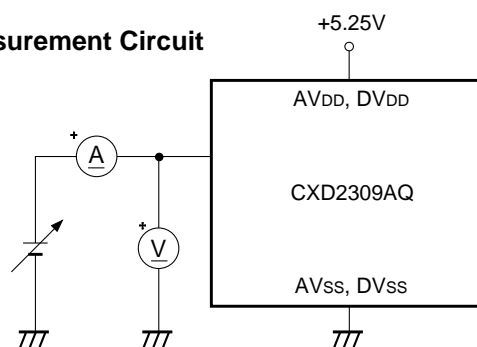
Electrical Characteristics (f_{CLK} = 85MHz, AV_{DD} = DV_{DD} = 5V, R_{OUT} = 200Ω, V_{REF} = 2.0V, R_{IR} = 3.3kΩ, Ta = 25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Resolution	n			10		bit
Conversion speed	f _{CLK}	AV _{DD} = DV _{DD} = 4.75 to 5.25V Ta = -20 to +85°C	0		85	MSPS
Integral non-linearity error	E _L	Endpoint	-2.0		2.0	LSB
Differential non-linearity error	E _D		-0.5		0.5	LSB
Precision guaranteed output voltage range	V _{OC}		1.8	1.92	2.0	V
Output full-scale voltage	V _{FS}		1.8	1.92	2.0	V
Output full-scale ratio *1	F _{SR}		0		3	%
Output full-scale current	I _{FS}		9.0	9.6	10	mA
Output offset voltage	V _{OS}	When "0000000000" data input			1	mV
Glitch energy	GE	R _{OUT} = 100Ω, 1V _{p-p} output		36		pV·s
Crosstalk	CT	When 10MHz sin wave input	F _{CLK} = 50MHz	40	49	dB
			F _{CLK} = 85MHz		49	
S/N ratio	SNR	When 1MHz sin wave input	F _{CLK} = 50MHz	50	63	dB
			F _{CLK} = 85MHz		61	
Supply current	I _{DD}	When 10MHz sin wave output	F _{CLK} = 50MHz		48	mA
			F _{CLK} = 85MHz		55	
Analog input resistance	R _{IN}	V _{REF}	1			MΩ
Input capacitance	C _I				9	pF
Output capacitance	C _O			15		pF
Digital input voltage	V _{IH}	AV _{DD} = DV _{DD} = 4.75 to 5.25V Ta = -20 to +75°C	2.15			V
	V _{IL}				0.85	
Digital input current	I _{IH}	AV _{DD} = DV _{DD} = 4.75 to 5.25V Ta = -20 to +75°C	-5		5	μA
	I _{IL}					
Setup time	t _s		4			ns
Hold time	t _h		1			ns
Propagation delay time	t _{PD}			6		ns
Rise time	t _r			7		ns
Fall time	t _f			12		ns

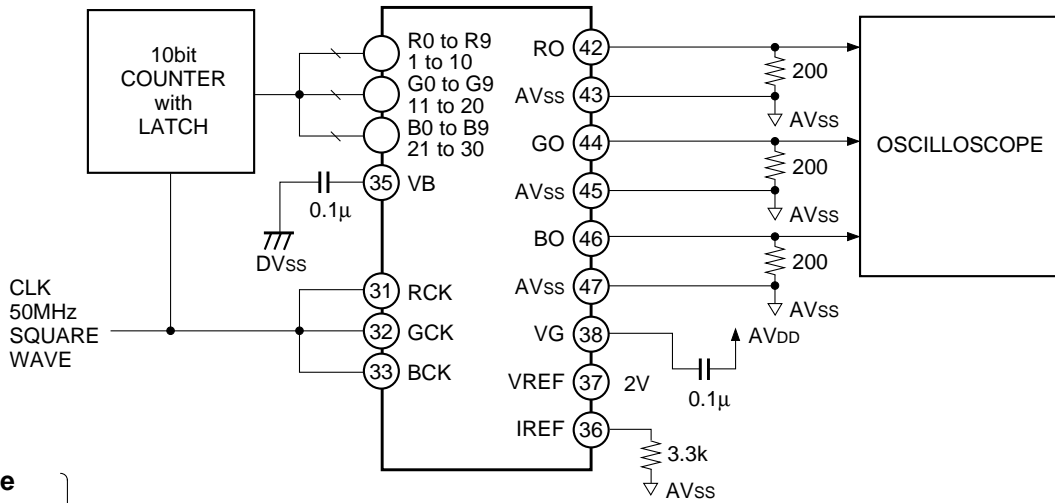
*1 Full-scale ratio = $\left| \frac{\text{Full-scale voltage of channel}}{\text{Average of the full-scale voltage of the channels}} - 1 \right| \times 100 [\%]$

Electrical Characteristics Measurement Circuit

Analog Input Resistance } Measurement Circuit
 Digital Input Current }

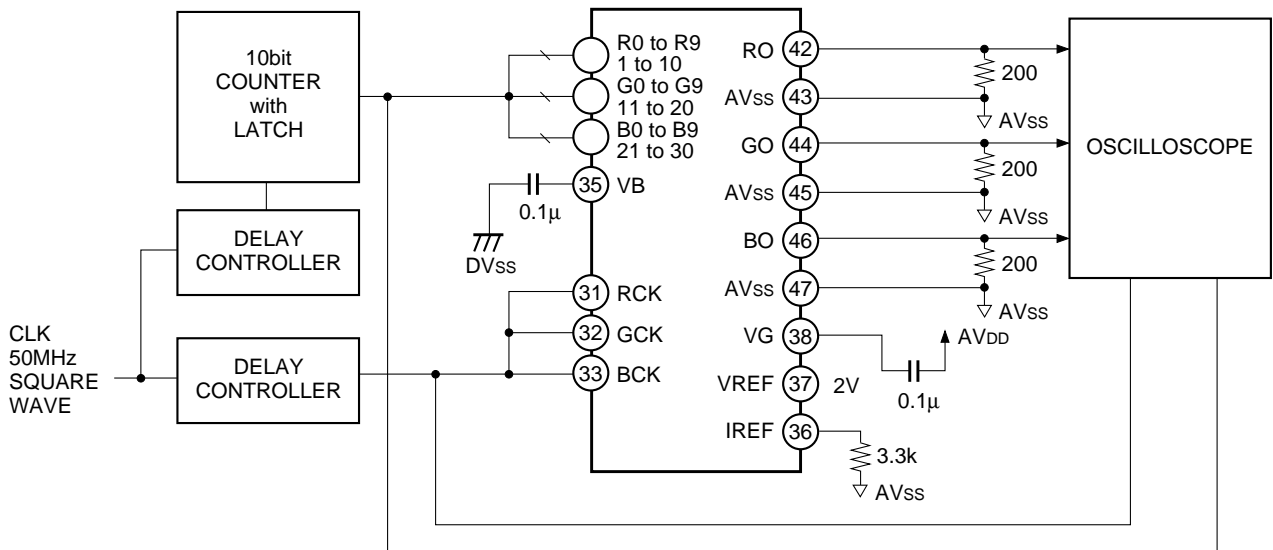


Conversion Rate Measurement Circuit

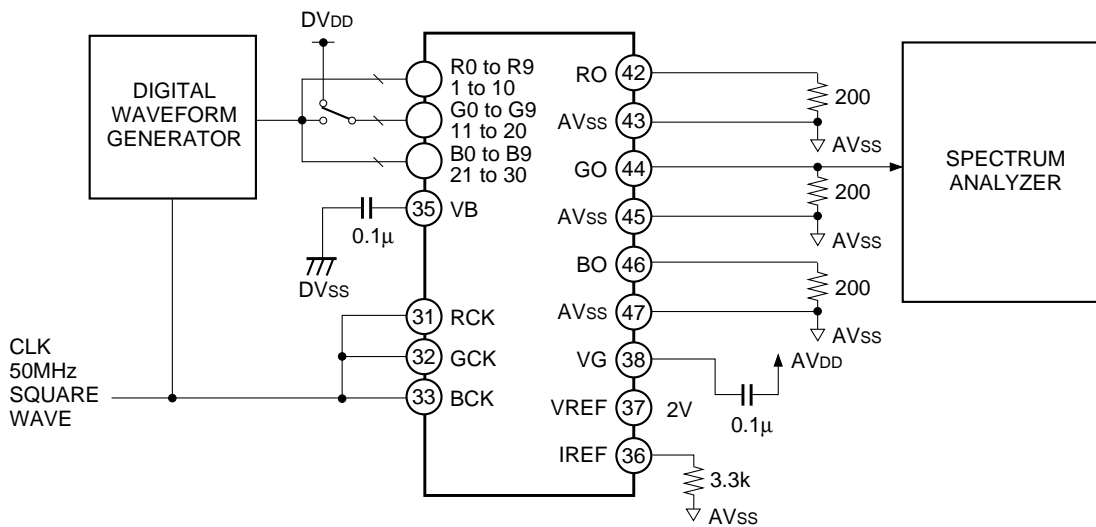


Setup Time
Hold Time
Glitch Energy

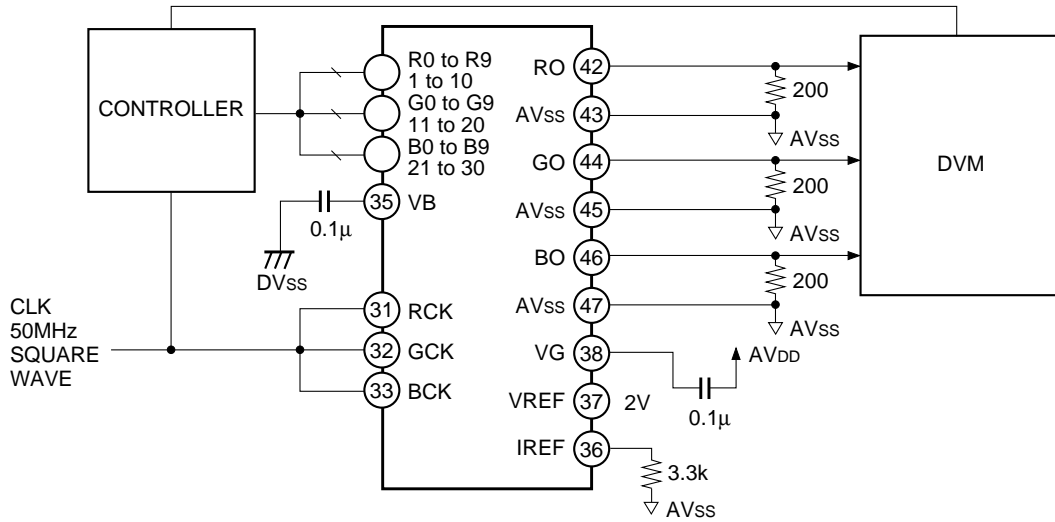
Measurement Circuit



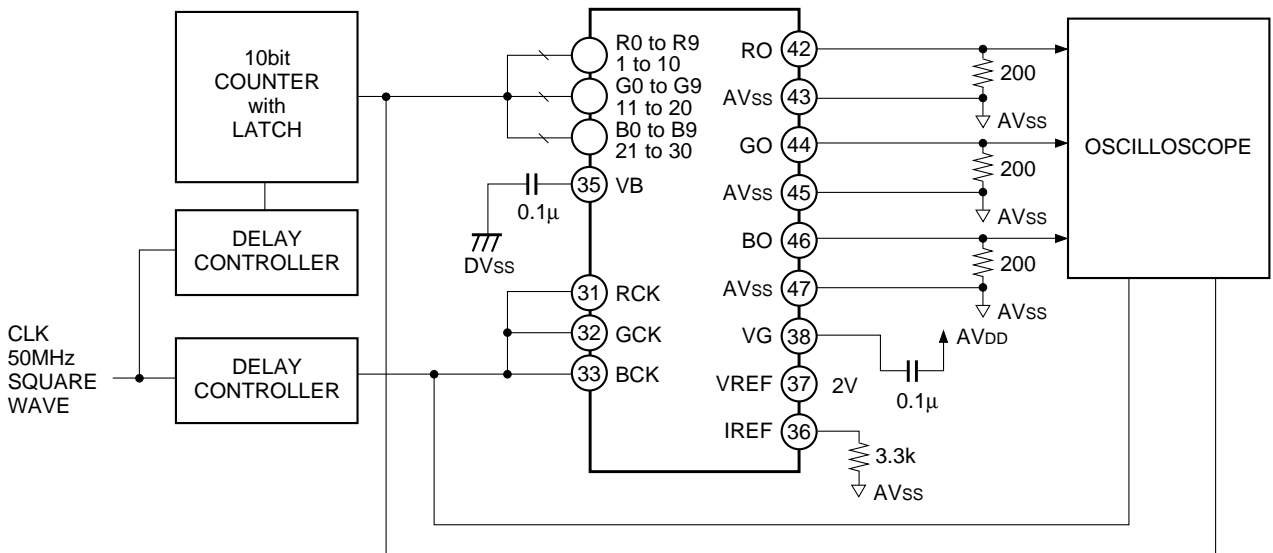
Crosstalk Measurement Circuit



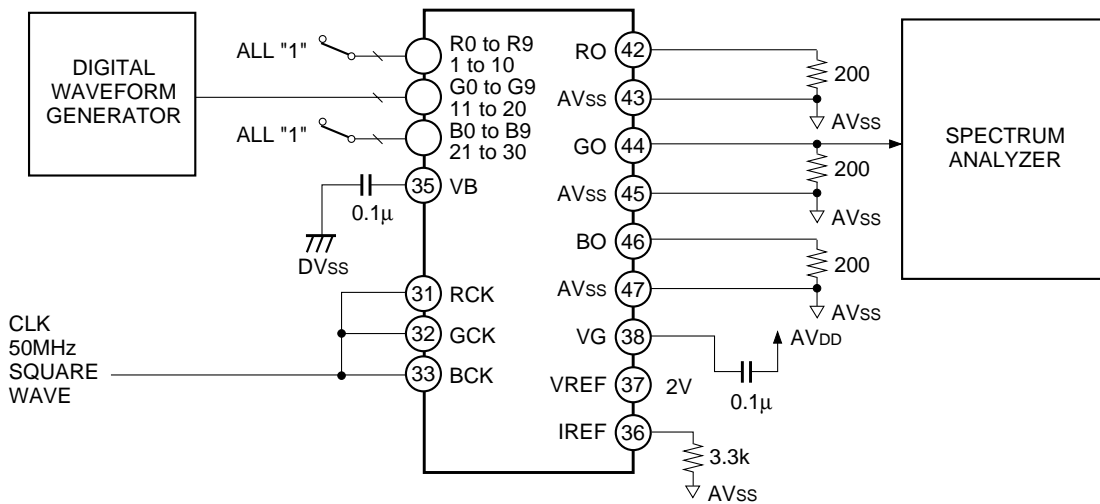
DC Characteristics Measurement Circuit



Propagation Delay Time Measurement Circuit

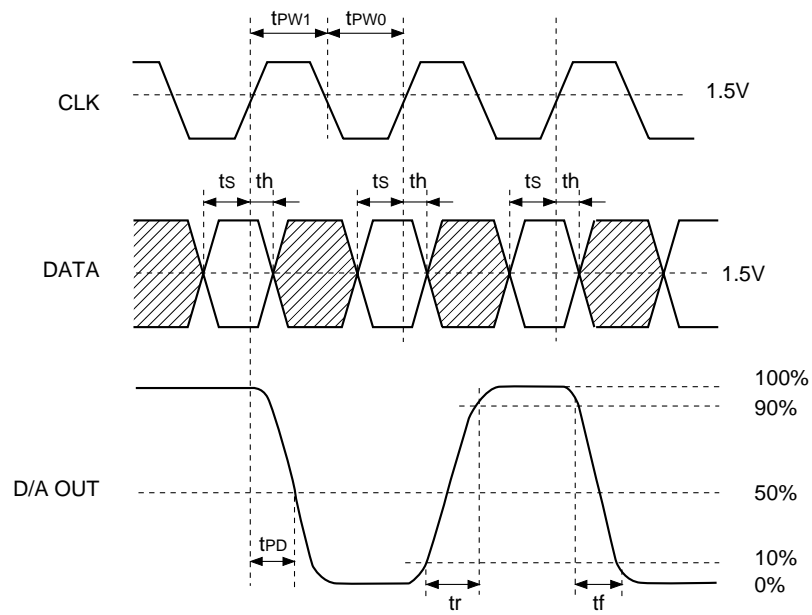


SNR Measurement Circuit



Description of Operation

Timing Chart



I/O Correspondence Table (output full-scale voltage: 2.00V)

Input code		Output voltage
MSB	LSB	
1	1	2.0V
1	1	
1	1	
1	1	
1	1	
1	1	
1	1	
1	1	
1	1	
:	:	
1	0	1.0V
0	0	
0	0	
0	0	
0	0	
0	0	
0	0	
0	0	
0	0	0V

Notes on Operation

- Selecting the Output Resistance

CXD2309AQ is a current output type D/A converter. The output voltage can be obtained by connecting the resistor R_{OUT} to the current output pins RO, GO and BO.

Specifications: Output full-scale voltage $V_{FS} = 18$ to 2.0 [V]
 Output full-scale current $I_{FS} = 9.0$ to 10.0 [mA]

Calculate the output resistance from $V_{FS} = I_{FS} \times R_{OUT}$. Connect a resistance sixteen times the output resistance to the reference current output pin IREF. In some cases, as this value may not exist, a similar value can be used instead.

Note that the V_{FS} Will be the following.

$$V_{FS} = V_{REF} \times 16R_{OUT}/R_{IR}$$

V_{REF} is the voltage set at the reference voltage input pin V_{REF} , R_{OUT} is the resistor to be connected to the current output pins RO, GO, BO and R_{IR} is the resistor to be connected to the IREF. Power consumption can be reduced by increasing the resistance, but this will on the contrary increase the glitch energy and data setting time. Set the best values according to the purpose of use.

- Power supply, ground

Separate the power supply and ground of the analog and digital signals around the device to reduce noise effects. Bypass the power supply pin to each ground with a $0.1\mu\text{F}$ ceramics capacitor as near as possible to the pin for both the digital and analog signals.

- Latch up

Analog and digital power supplies must be able to share the same power supply of the board. This is to prevent latch up caused by potential difference between the two pins when the power is turned on. See "Latch Up Prevention" on Page 11.

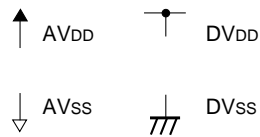
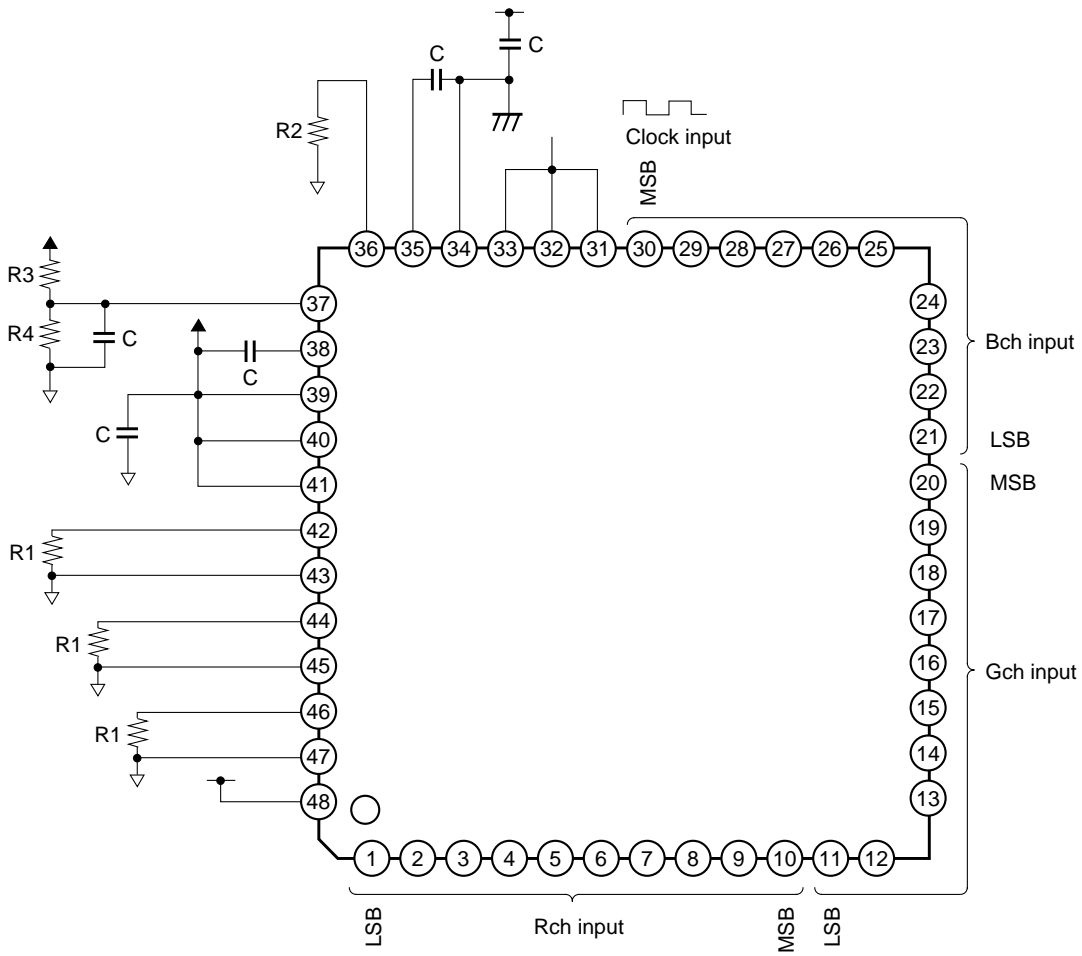
- IREF

The IREF pin is very sensitive to improve the AC characteristics. Pay attention for capacitance component not to attach to this pin because its output may become unstable.

- Output full-scale voltage

For the applications using the RGB signal, the color balance may be broken up when the RO, GO and BO output full-scale voltages are used with not adjustment.

Application Circuit



- When the power supply (AVDD and DVDD) is 5.0V.
- R1 = 200Ω
- R2 = 3.3kΩ
- R3 = 3.0kΩ
- R4 = 2.0kΩ
- C = 1μF

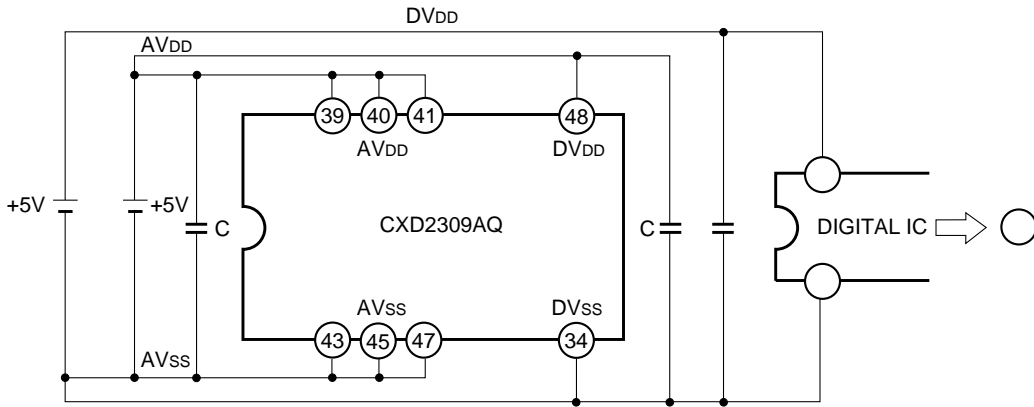
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Latch Up Prevention

The CXD2309AQ is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pin 39, 40 and 41) and DV_{DD} (Pin 48), when power supply is ON.

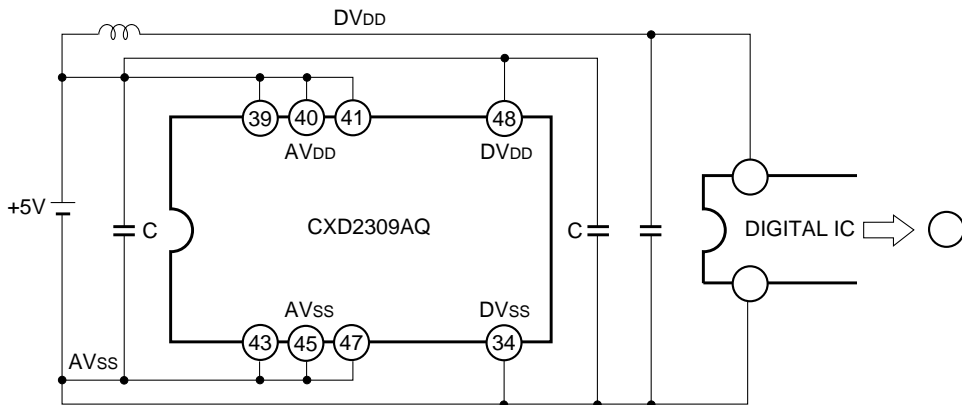
1. Correct usage

a. When analog and digital supplies are from different sources

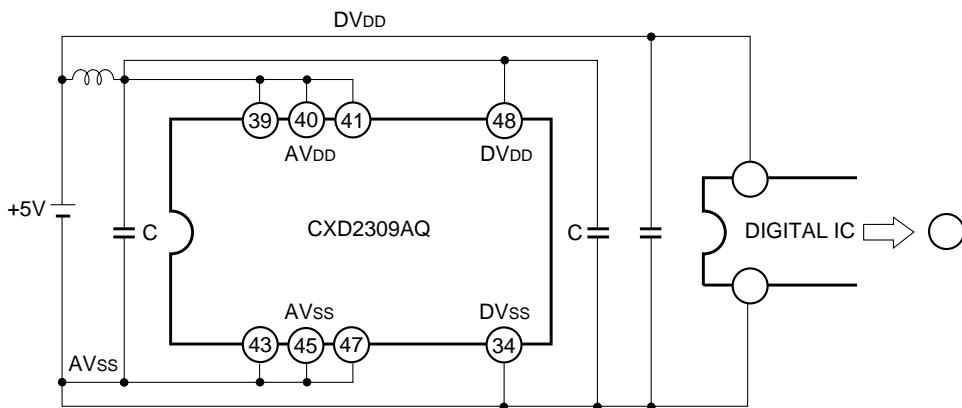


b. When analog and digital supplies are from a common source

(i)

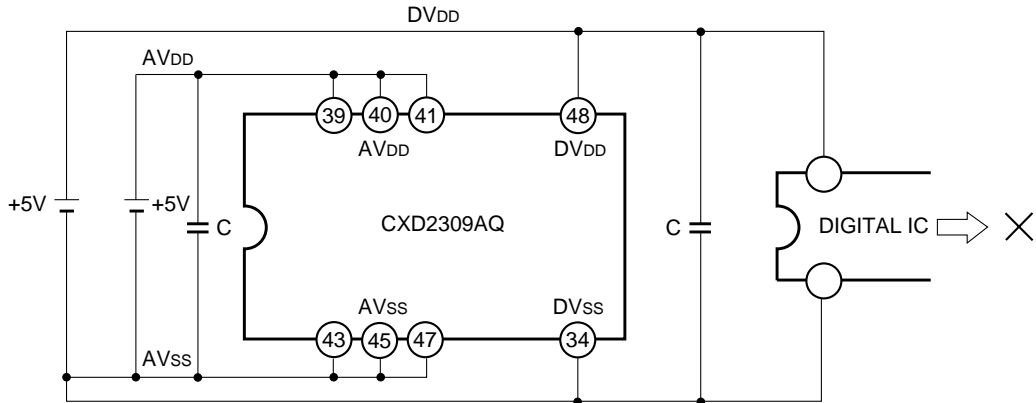


(ii)



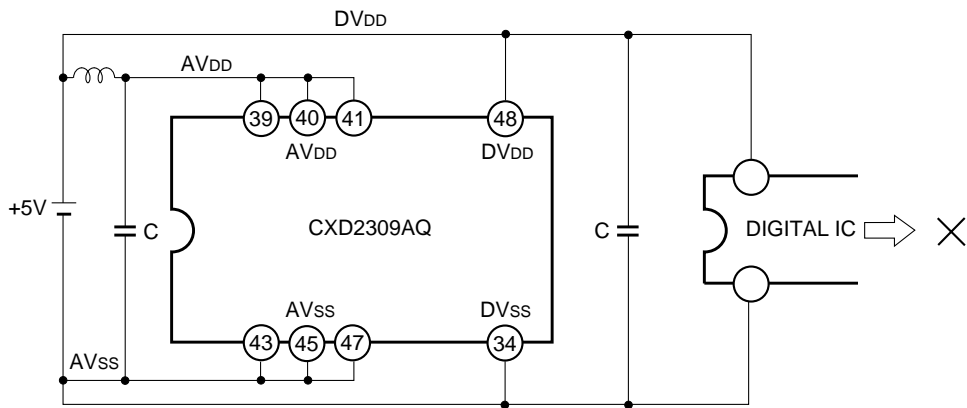
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

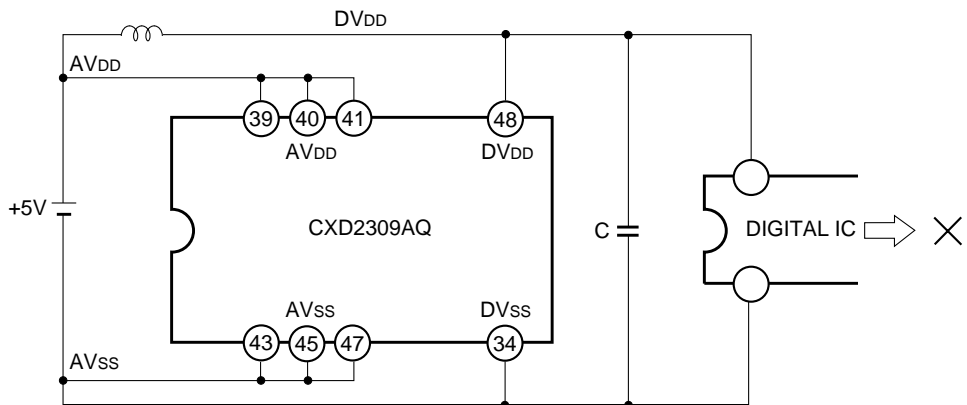


b. When analog and digital supplies are from common source

(i)



(ii)



Example of Representative Characteristics

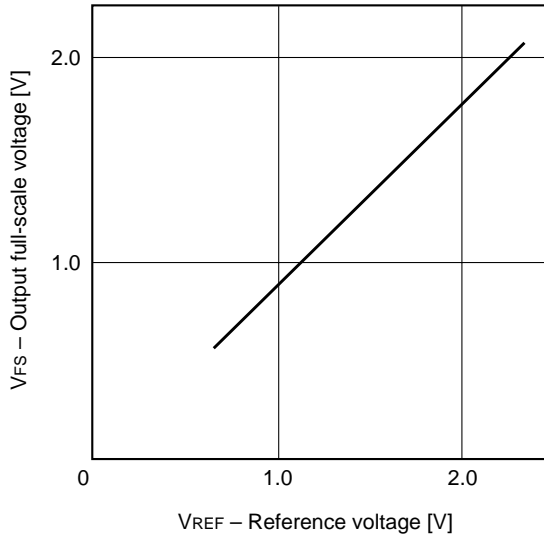


Fig. 1. Reference voltage vs. Output full-scale voltage

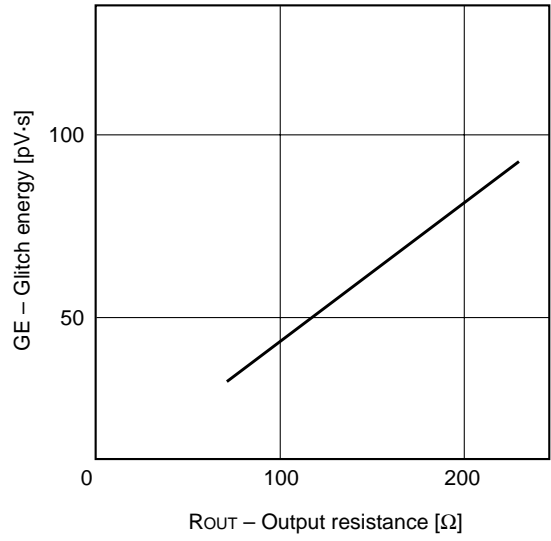


Fig. 2. Output resistance vs. Glitch energy

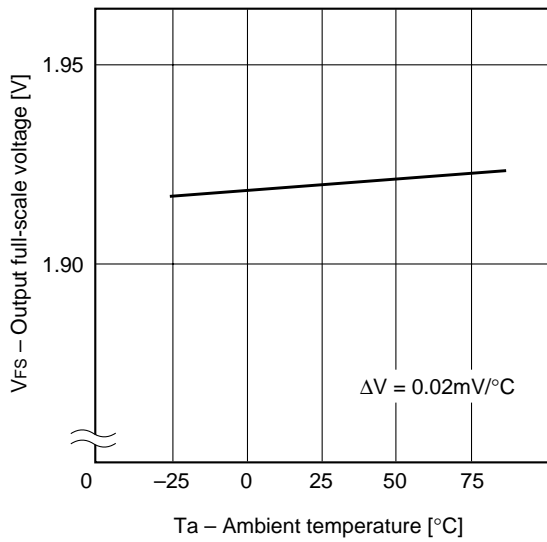


Fig. 3. Ambient temperature vs. Output full-scale voltage

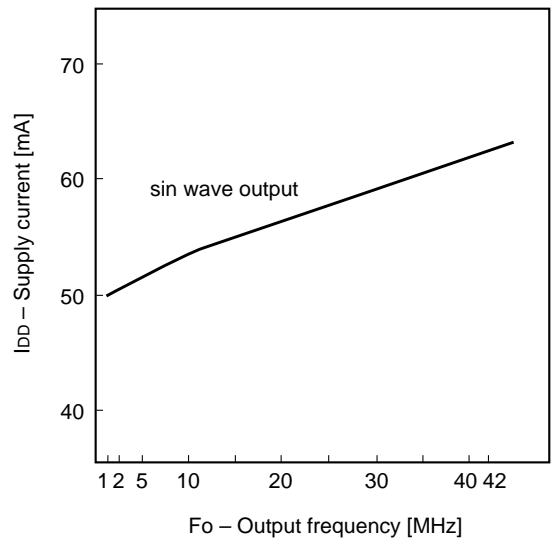


Fig. 4. Output frequency vs. Supply current

Standard Measurement Conditions

- AVDD = DVDD = 5.0V
- VREF = 2.0V
- FCLK = 85MHz
- ROUT = 200Ω
- RIR = 3.3kΩ
- Ta = 25°C

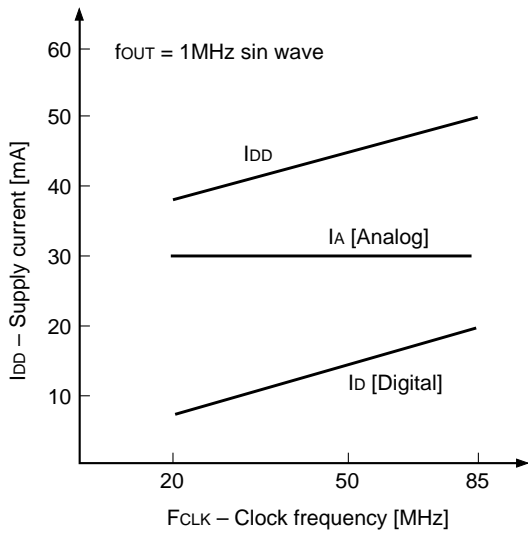


Fig. 5. Clock frequency vs. Supply current

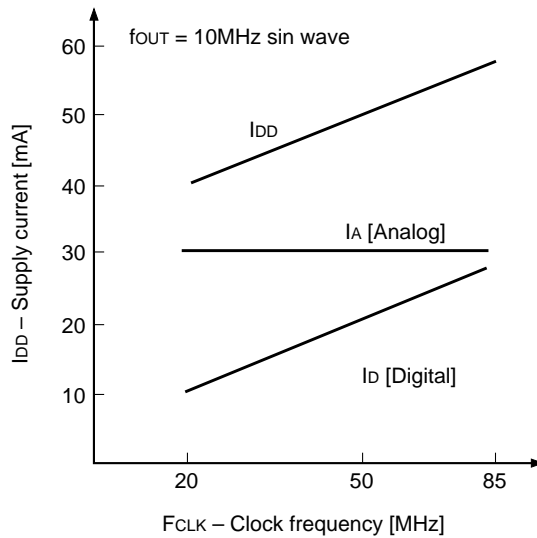


Fig. 6. Clock frequency vs. Supply current

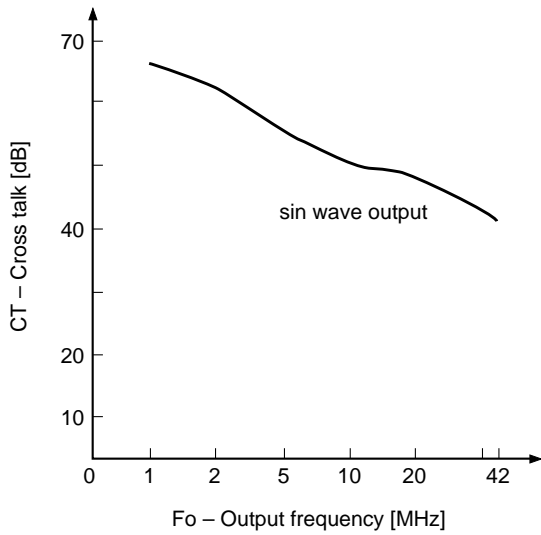


Fig. 7. Output frequency vs. Cross talk

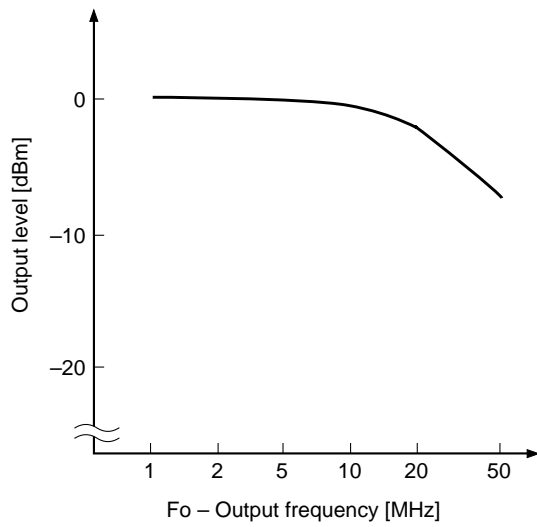


Fig. 8. Output frequency vs. Output level (Including primary hold characteristics $\sin x/x$)

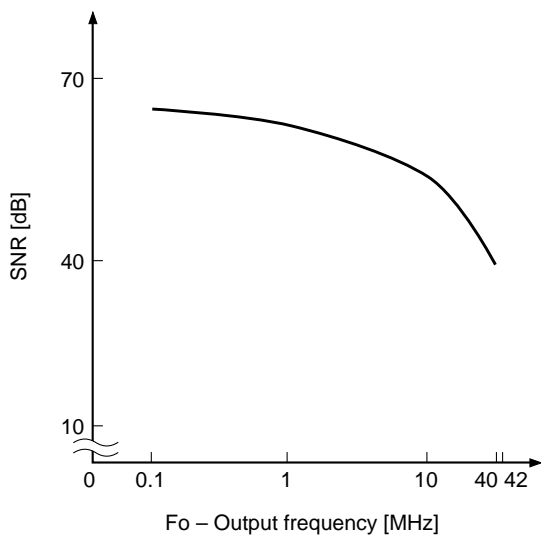


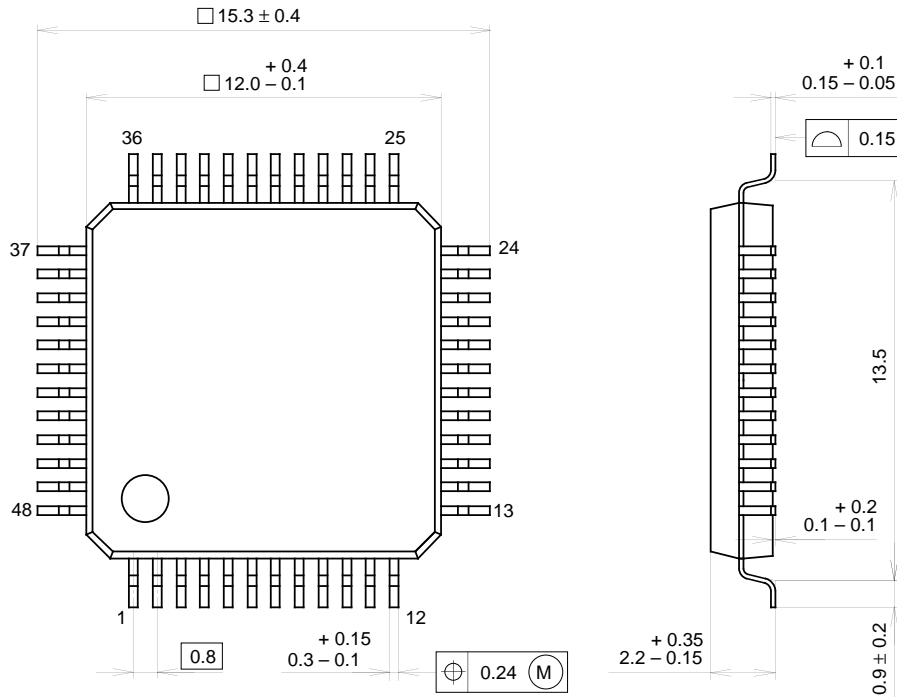
Fig. 9. Output frequency vs. SNR

Standard Measurement Conditions

- $A_{VDD} = D_{VDD} = 5.0V$
- $V_{REF} = 2.0V$
- $F_{CLK} = 85MHz$
- $R_{OUT} = 200\Omega$
- $R_{IR} = 3.3k\Omega$
- $T_a = 25^\circ C$

Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g



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