SONY

CXD3422GA

Timing Generator and Signal Processor for Frame Readout CCD Image Sensor

Description

The CXD3422GA is a timing generator and CCD signal processor IC for the ICX284, ICX432/434 CCD image sensor.

Features

- Timing generator functions
  - Horizontal drive frequency 18 to 24.3MHz (Base oscillation frequency 36 to 48.6MHz)
  - Supports frame readout/draft (sextuple speed)/ AF (Auto focus drive) (ICX432 mode)
  - Supports frame readout/draft (quadruple speed)/ AF (Auto focus drive) (ICX434 mode)
  - High-speed/low-speed shutter function
  - Horizontal and vertical drivers for CCD image sensor
- CCD signal processor functions
  - Correlated double sampling
  - Programmable gain amplifier (PGA) allows gain adjustment over a wide range (–6 to +42dB)
  - 10-bit A/D converter
- Chip Scale Package (CSP):
  CSP allows vast reduction in the CCD camera block footprint

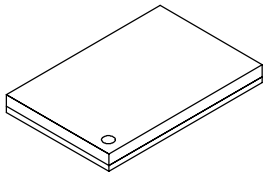
Applications

Digital still cameras

Applicable CCD Image Sensors

ICX284 (Type 1/2.7, 2020K pixels)
ICX432 (Type 1/2.7, 3240K pixels)
ICX434 (Type 1/3.2, 2020K pixels)

96 pin LFLGA (Plastic)



Absolute Maximum Ratings

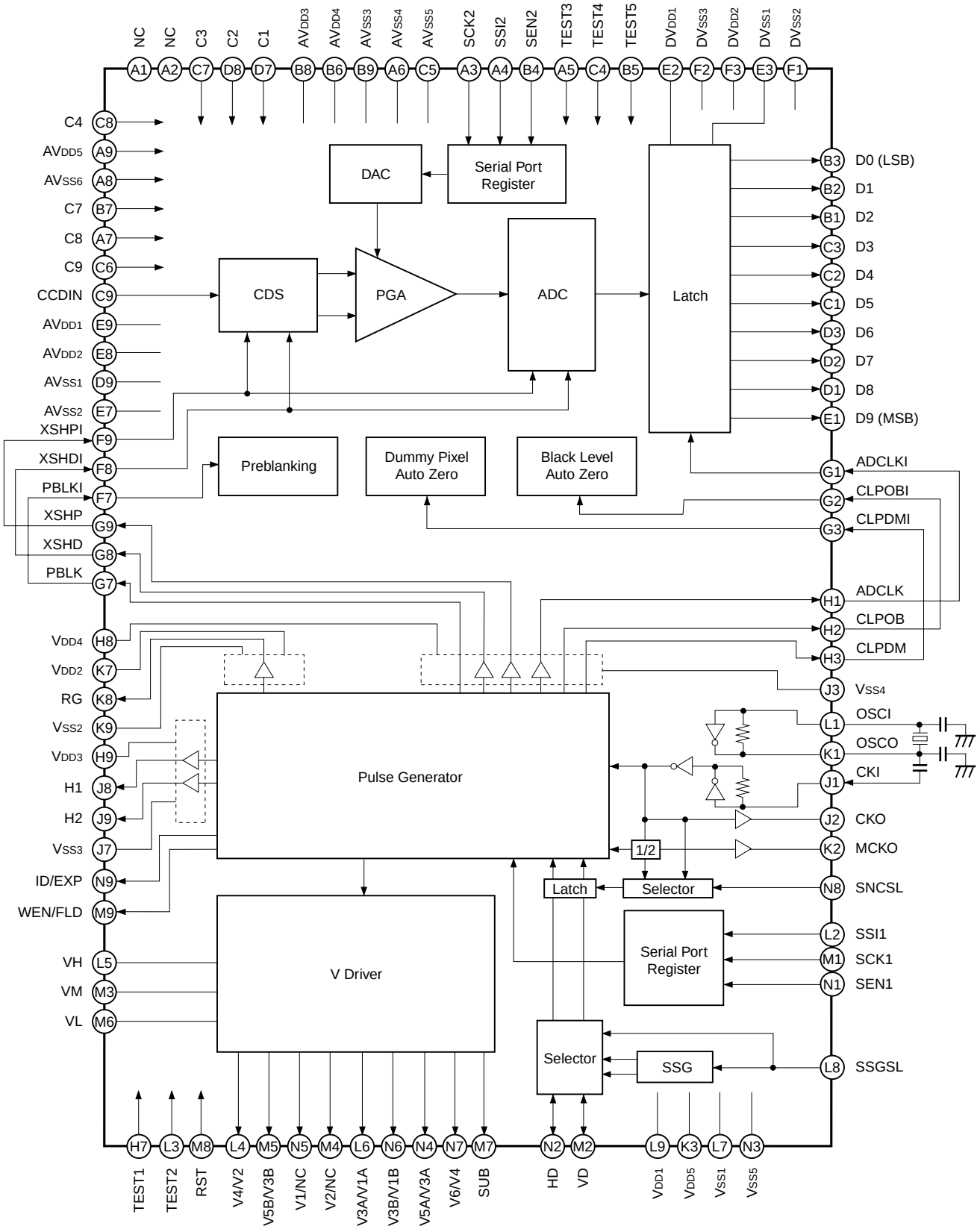
• Supply voltage			
$V_{DD}a$, $V_{DD}b$, $V_{DD}c$, $V_{DD}d$		V_{SS} – 0.3 to +7.0	V
$V_{DD}e$, $V_{DD}f$, $V_{DD}g$		V_{SS} – 0.3 to +4.0	V
	VL	–10.0 to V_{SS}	V
	VH	VL – 0.3 to +26.0	V
• Input voltage (analog)			
	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Input voltage (digital)			
	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage			
	V_{O1}	V_{SS} – 0.3 to V_{DD} + 0.3	V
	V_{O2}	VL – 0.3 to V_{SS} + 0.3	V
	V_{O3}	VL – 0.3 to VH + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +125	°C

Recommended Operating Conditions

• Supply voltage			
$V_{DD}a$, $V_{DD}b$, $V_{DD}c$, $V_{DD}d$,			
$V_{DD}e$, $V_{DD}f$, $V_{DD}g$		3.0 to 3.6	V
	VM	0.0	V
	VH	14.5 to 15.5	V
	VL	–7.0 to –8.0	V
• Operating temperature			
	Topr	–20 to +75	°C

E02125-PS

Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9
A	NC	NC	SCK2	SSI2	TEST3	AV_{SS4}	C8	AV_{SS6}	AV_{DD5}
B	D2	D1	D0	SEN2	TEST5	AV_{DD4}	C7	AV_{DD3}	AV_{SS3}
C	D5	D4	D3	TEST4	AV_{SS5}	C9	C3	C4	CCDIN
D	D8	D7	D6				C1	C2	AV_{SS1}
E	D9	DV_{DD1}	DV_{SS1}				AV_{SS2}	AV_{DD2}	AV_{DD1}
F	DV_{SS2}	DV_{SS3}	DV_{DD2}				PBLKI	XSHDI	XSHPI
G	ADCLKI	CLPOBI	CLPDMI				PBLK	XSHD	XSHP
H	ADCLK	CLPOB	CLPDM				TEST1	V_{DD4}	V_{DD3}
J	CKI	CKO	V_{SS4}				V_{SS3}	H1	H2
K	OSCO	MCKO	V_{DD5}				V_{DD2}	RG	V_{SS2}
L	OSCI	SSI1	TEST2	V4 (V2)	VH	V3A (V1A)	V_{SS1}	SSGSL	V_{DD1}
M	SCK1	VD	VM	V2 (NC)	V5B (V3B)	VL	SUB	RST	WEN/FLD
N	SEN1	HD	V_{SS5}	V5A (V3A)	V1 (NC)	V3B (V1B)	V6 (V4)	SNCSL	ID/EXP

Note) The symbol in parenthesis is for ICX434 mode.

Pin Description

Pin No.	Symbol	I/O	Description
A1	NC	—	No connected. (Open)
A2	NC	—	No connected. (Open)
A3	SCK2	I	CCD signal processor block serial interface clock input. (Schmitt trigger)
A4	SSI2	I	CCD signal processor block serial interface data input. (Schmitt trigger)
A5	TEST3	I	CCD signal processor block test input 3. Connect to DV_{SS}.
A6	AV_{SS4}	—	CCD signal processor block analog GND.
A7	C8	—	Capacitor connection.
A8	AV_{SS6}	—	CCD signal processor block analog GND.
A9	AV_{DD5}	—	CCD signal processor block analog power supply.
B1	D2	O	ADC output.
B2	D1	O	ADC output.
B3	D0	O	ADC output (LSB).
B4	SEN2	I	CCD signal processor block serial interface enable input. (Schmitt trigger)
B5	TEST5	I	CCD signal processor block test input 5. Connect to DV_{DD}.
B6	AV_{DD4}	—	CCD signal processor block analog power supply.
B7	C7	—	Capacitor connection.
B8	AV_{DD3}	—	CCD signal processor block analog power supply.
B9	AV_{SS3}	—	CCD signal processor block analog GND.
C1	D5	O	ADC output.
C2	D4	O	ADC output.
C3	D3	O	ADC output.
C4	TEST4	I	CCD signal processor block test input 4. Connect to DV_{SS}.
C5	AV_{SS5}	—	CCD signal processor block analog GND.
C6	C9	—	Capacitor connection.
C7	C3	—	Capacitor connection.
C8	C4	—	Capacitor connection.
C9	CCDIN	I	CCD output signal input.
D1	D8	O	ADC output.
D2	D7	O	ADC output.
D3	D6	O	ADC output.
D7	C1	—	Capacitor connection.
D8	C2	—	Capacitor connection.
D9	AV_{SS1}	—	CCD signal processor block analog GND.
E1	D9	O	ADC output (MSB).
E2	DV_{DD1}	—	CCD signal processor block digital power supply. (Power supply for ADC)
E3	DV_{SS1}	—	CCD signal processor block digital GND. (GND for ADC)
E7	AV_{SS2}	—	CCD signal processor block analog GND.

Pin No.	Symbol	I/O	Description
E8	AV_{DD2}	—	CCD signal processor block analog power supply.
E9	AV_{DD1}	—	CCD signal processor block analog power supply.
F1	DV_{SS2}	—	CCD signal processor block digital GND.
F2	DV_{SS3}	—	CCD signal processor block digital GND.
F3	DV_{DD2}	—	CCD signal processor block digital power supply.
F7	PBLKI	I	Pulse input for horizontal and vertical blanking period pulse cleaning. (Schmitt trigger)
F8	XSHDI	I	CCD data level sample-and-hold pulse input. (Schmitt trigger)
F9	XSHPI	I	CCD precharge level sample-and-hold pulse input. (Schmitt trigger)
G1	ADCLKI	I	Clock input for analog/digital conversion. (Schmitt trigger)
G2	CLPOBI	I	CCD optical black signal clamp pulse input. (Schmitt trigger)
G3	CLPDMI	I	CCD dummy signal clamp pulse input. (Schmitt trigger)
G7	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning.
G8	XSHD	O	CCD data level sample-and-hold pulse output.
G9	XSHP	O	CCD precharge level sample-and-hold pulse output.
H1	ADCLK	O	Clock output for analog/digital conversion. Logical phase adjustment possible using the serial interface data.
H2	CLPOB	O	CCD optical black signal clamp pulse output. Horizontal and vertical OB pattern charge possible using the serial interface data.
H3	CLPDM	O	CCD dummy signal clamp pulse output.
H7	TEST1	I	Timing generator block test input 1. Normally fix to GND. (With pull-down resistor)
H8	V_{DD4}	—	Timing generator block digital power supply. (Power supply for CDS block)
H9	V_{DD3}	—	Timing generator block digital power supply. (Power supply for H1/H2)
J1	CKI	I	Inverter input.
J2	CKO	O	Inverter output.
J3	V_{SS4}	—	Timing generator block digital GND.
J7	V_{SS3}	—	Timing generator block digital GND.
J8	H1	O	CCD horizontal register clock output.
J9	H2	O	CCD horizontal register clock output.
K1	OSCO	O	Inverter output for oscillation. When not used, leave open or connect a capacitor.
K2	MCKO	O	System clock output for signal processor IC.
K3	V_{DD5}	—	Timing generator block digital power supply. (Power supply for common logic block)
K7	V_{DD2}	—	Timing generator block digital power supply. (Power supply for RG)
K8	RG	O	CCD reset gate pulse output.
K9	V_{SS2}	—	Timing generator block digital GND.
L1	OSCI	I	Inverter input for oscillation. When not used, fix to low.
L2	SSI1	I	Timing generator block serial interface data input. Schmitt trigger input.

Pin No.	Symbol	I/O	Description
L3	TEST2	I	Timing generator block test input 2. Normally fix to GND. (With pull-down resistor)
L4	V4 (V2)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
L5	VH	—	Timing generator block 15.0V power supply. (Power supply for vertical driver)
L6	V3A (V1A)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
L7	V_{SS1}	—	Timing generator block digital GND.
L8	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External sync valid (With pull-down resistor)
L9	V_{DD1}	—	Timing generator block digital power supply. (Power supply for common logic block)
M1	SCK1	I	Timing generator block serial interface clock input. Schmitt trigger input.
M2	VD	I/O	Vertical sync signal input/output.
M3	VM	—	Timing generator block GND. (GND for vertical driver)
M4	V2 (NC)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
M5	V5B (V3B)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
M6	VL	—	Timing generator block –7.5V power supply. (Power supply for vertical driver)
M7	SUB	O	CCD electric shutter pulse.
M8	RST	I	Timing generator block reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input.
M9	WEN/FLD	O	Memory write timing pulse output/field discrimination pulse output. Switching possible using the serial interface data. (Default: WEN output)
N1	SEN1	I	Timing generator block serial interface strobe input. Schmitt trigger input.
N2	HD	I/O	Horizontal sync signal input/output.
N3	V_{SS5}	—	Timing generator block digital GND.
N4	V5A (V3A)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
N5	V1 (NC)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
N6	V3B (V1B)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
N7	V6 (V4)	O	CCD vertical register clock output. The symbol in parenthesis is for ICX434 mode.
N8	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync (With pull-down resistor)
N9	ID/EXP	O	Vertical direction line identification pulse output/Exposure time idenfication pulse output. Switching possible using the serial interface data. (Default: ID output)

Electrical Characteristics

Timing Generator Block Electrical Characteristics

DC Characteristics (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD2}	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	V_{DD3}	$V_{DD}b$		3.0	3.3	3.6	V
Supply voltage 3	V_{DD4}	$V_{DD}c$		3.0	3.3	3.6	V
Supply voltage 4	V_{DD1}, V_{DD5}	$V_{DD}d$		3.0	3.3	3.6	V
Input voltage 1*1	RST, SSI1, SCK1, SEN1	V_{I+}		0.8V_{DD}d			V
		V_{I-}				0.2V_{DD}d	V
Input voltage 2*2	TEST1, TEST2, SNCSL, SSGSL	V_{IH1}		0.7V_{DD}d			V
		V_{IL1}				0.3V_{DD}d	V
Input/output voltage	VD, HD	V_{IH2}		0.8V_{DD}d			V
		V_{IL2}				0.2V_{DD}d	V
		V_{OH1}	Feed current where I_{OH} = –1.2mA	V_{DD}d – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 1	H1, H2	V_{OH2}	Feed current where I_{OH} = –14.0mA	V_{DD}b – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 9.6mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	V_{DD}a – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, PBLK, CLPOB, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	V_{DD}c – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	CKO	V_{OH5}	Feed current where I_{OH} = –6.9mA	V_{DD}d – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 5	MCKO	V_{OH6}	Feed current where I_{OH} = –3.3mA	V_{DD}d – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 6	ID/EXP, WEN/FLD	V_{OH7}	Feed current where I_{OH} = –2.4mA	V_{DD}d – 0.8			V
		V_{OL7}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output current 1	V1, V2, V3A, V3B, V4, V5A, V5B, V6	I_{OL}	V1, V2, V3A/B, V4, V5A/B, V6 = –8.25V	10.0			mA
		I_{OM1}	V1, V2, V3A/B, V4, V5A/B, V6 = –0.25V			–5.0	mA
		I_{OM2}	V1, V3A/B, V5A/B = 0.25V	5.0			mA
		I_{OH}	V1, V3A/B, V5A/B = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 This input pin is a schmitt trigger input.

*2 These input pins are with pull-down resistor in the IC.

Note) The above table indicates the condition for 3.3V drive.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DD}d/2$		V
Input voltage	OSCI	V_{IH}		0.7$V_{DD}d$			V
		V_{IL}				0.3$V_{DD}d$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –3.6mA	$V_{DD}d$ – 0.8			V
		V_{OL}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	V_{IN} = $V_{DD}d$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DD}d/2$		V
Input voltage		V_{IH}		0.7$V_{DD}d$			V
		V_{IL}				0.3$V_{DD}d$	V
Input amplitude		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source.
Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

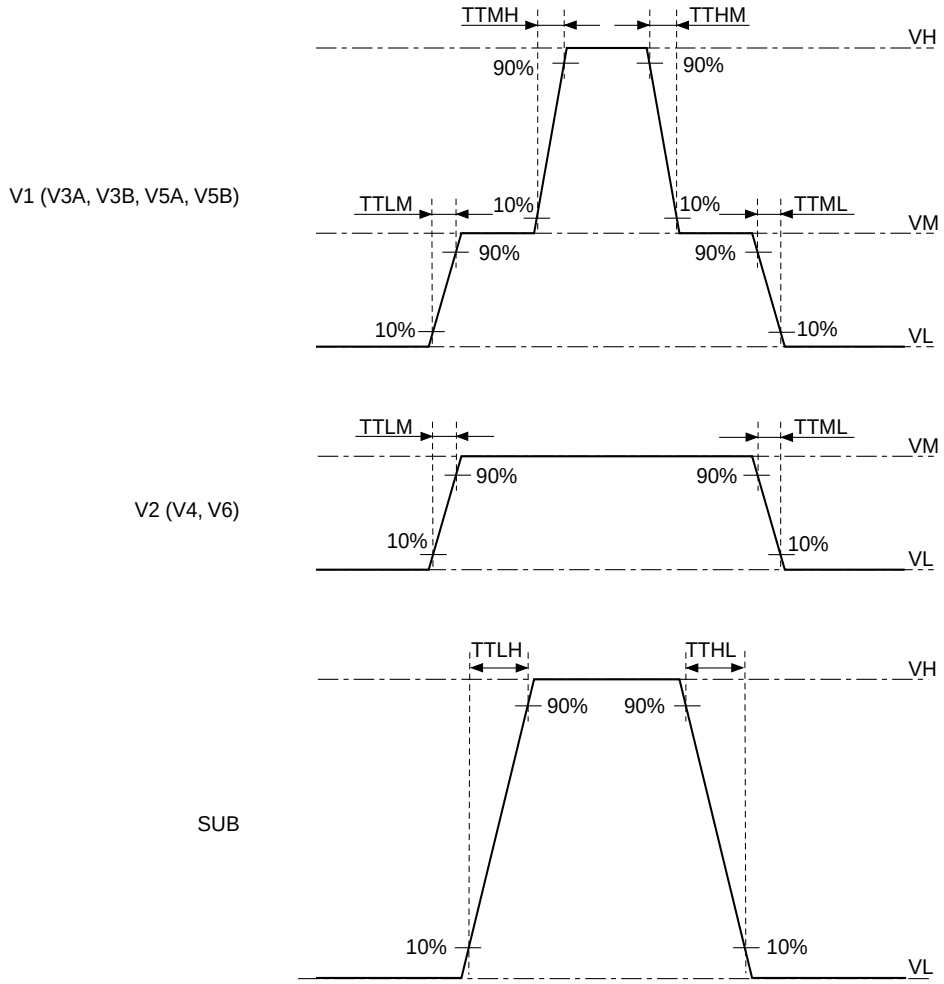
Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

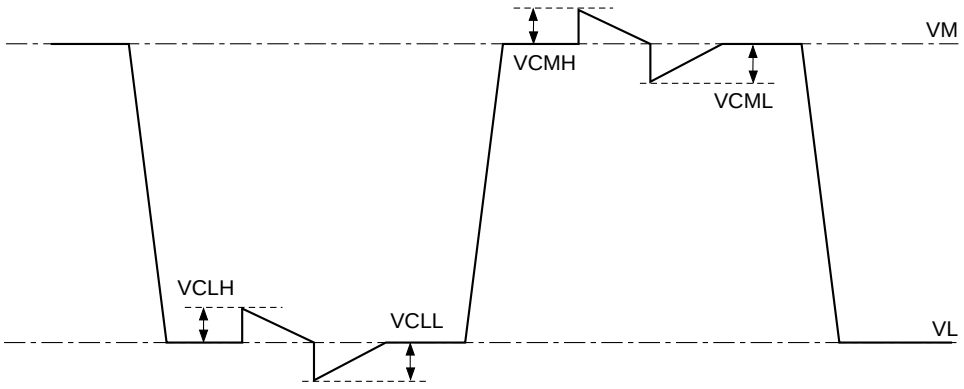
Notes)

1. The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2. For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3. To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

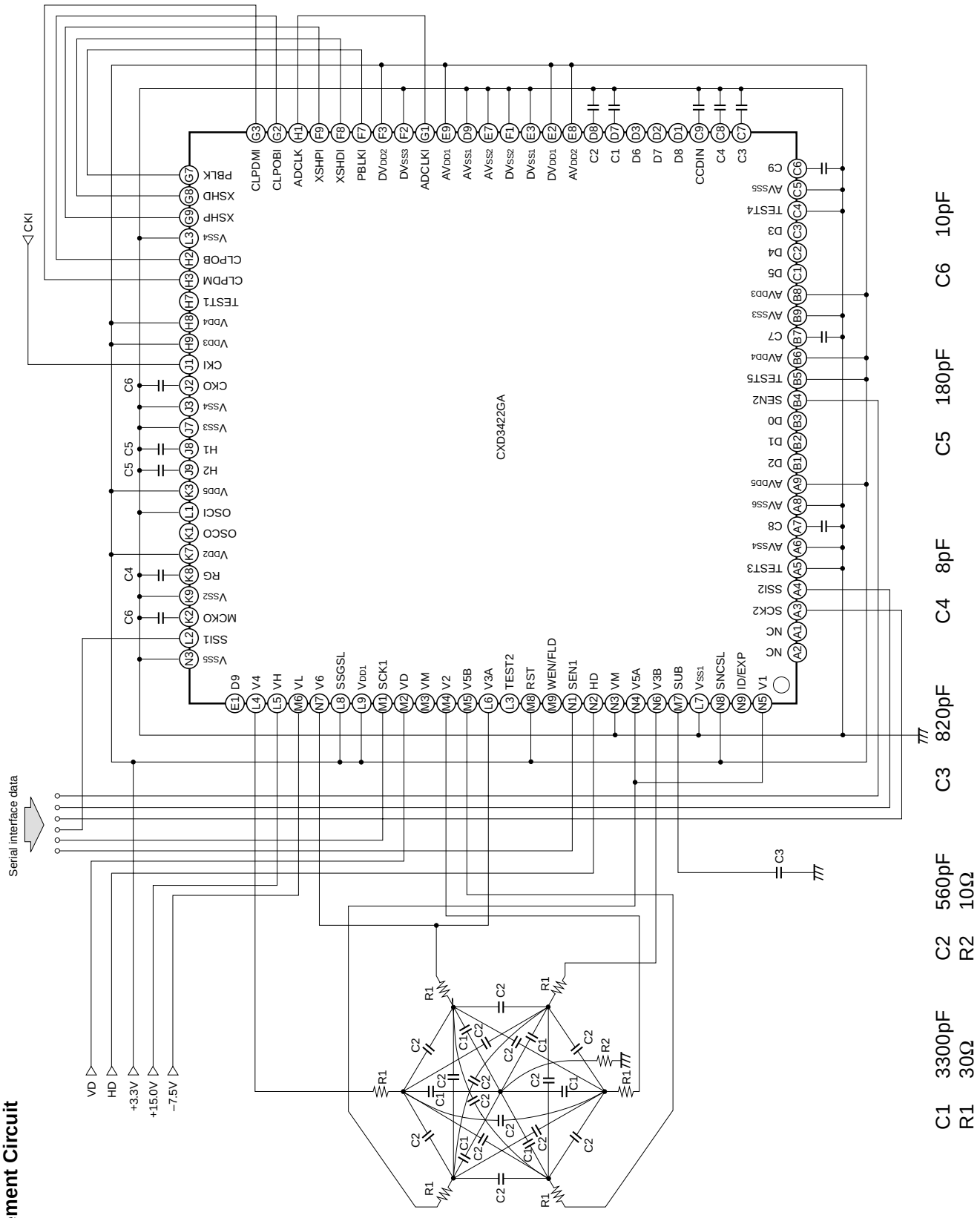
Switching Waveforms



Waveform Noise

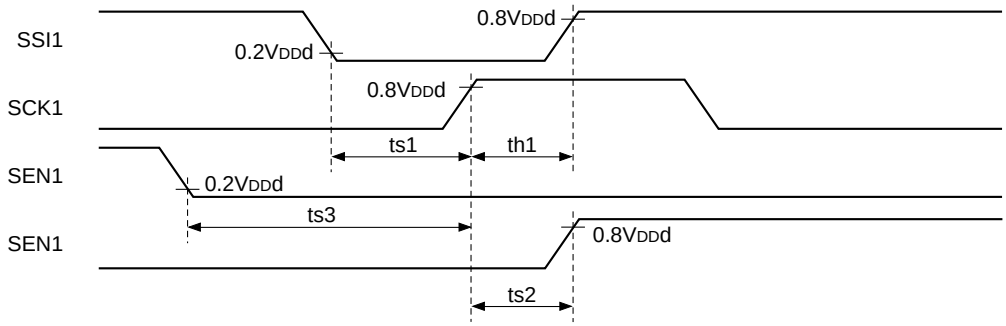


Measurement Circuit



AC Characteristics

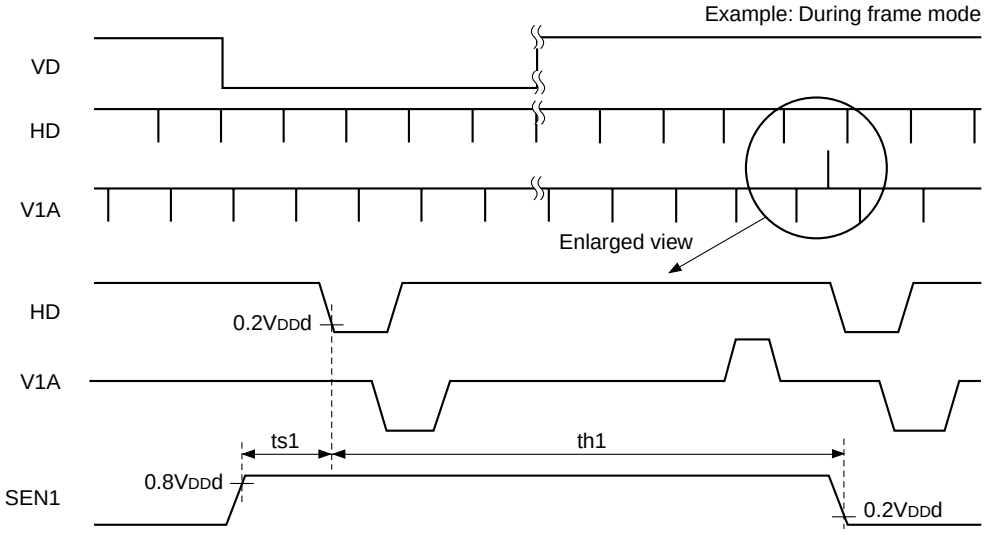
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI1 setup time, activated by the rising edge of SCK1	20			ns
th1	SSI1 hold time, activated by the rising edge of SCK1	20			ns
ts2	SCK1 setup time, activated by the rising edge of SEN1	20			ns
ts3	SEN1 setup time, activated by the rising edge of SCK1	20			ns

Serial interface clock internal loading characteristics (1)

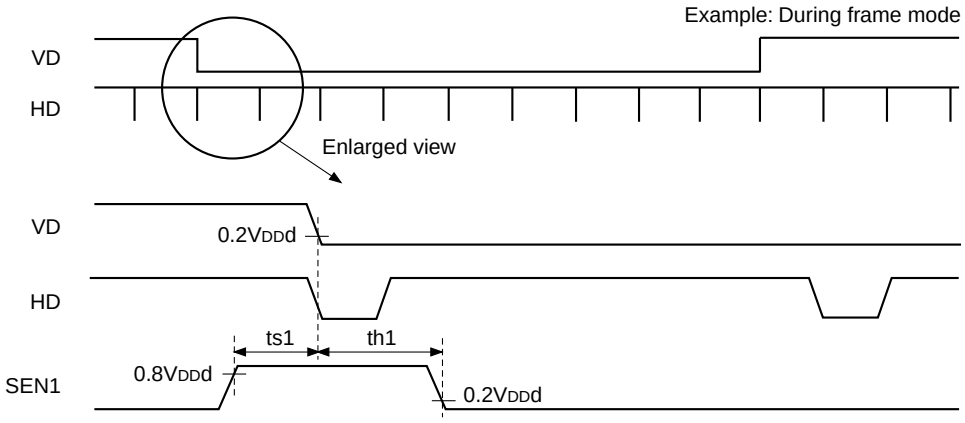


* Be sure to maintain a constantly high SEN1 logic level near the falling edge of the HD in the horizontal period during which V1A/B and V3A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of HD	0			ns
th1	SEN1 hold time, activated by the falling edge of HD	123			µs

Serial interface clock internal loading characteristics (2)



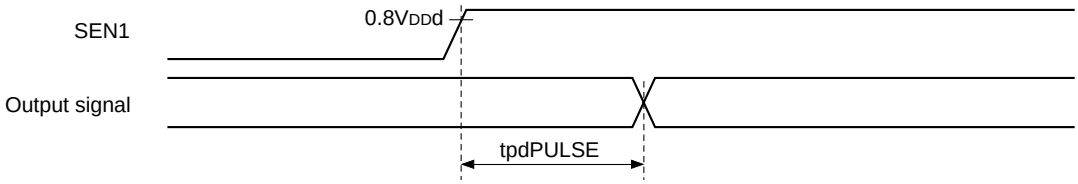
* Be sure to maintain a constantly high SEN1 logic level near the falling edge of VD.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN1 setup time, activated by the falling edge of VD	0			ns
th1	SEN1 hold time, activated by the falling edge of VD	200			ns

Serial interface clock output variation characteristics

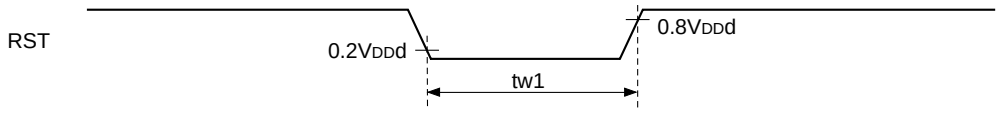
Normally, the serial interface data is loaded to the CXD3422GA at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD3422GA and controlled at the rising edge of SEN1. See "Description of Operation".



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN1	5		100	ns

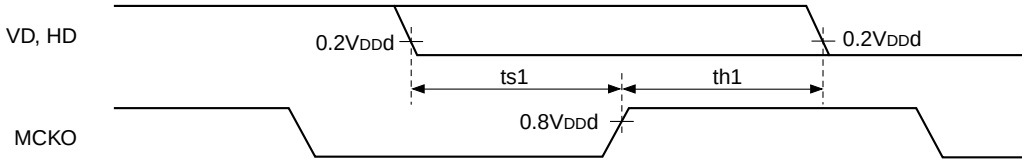
RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

VD and HD loading characteristics

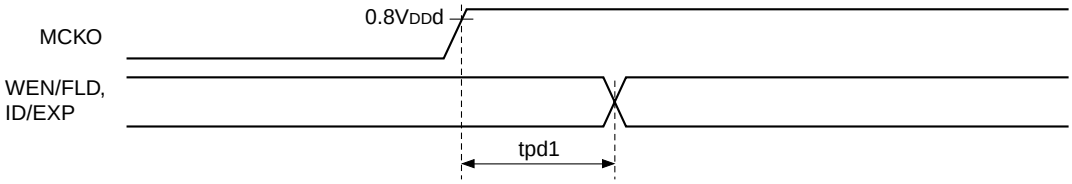


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VD and HD setup time, activated by the rising edge of MCKO	13			ns
th1	VD and HD hold time, activated by the rising edge of MCKO	0			ns

Output variation characteristics



WEN/FLD and ID/EXP load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	20		60	ns

CCD Signal Processor Block Electrical Characteristics

DC Characteristics

(Fc = 24.3MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	DV_{DD1}	V_{DD}e		3.0	3.3	3.6	V
Supply voltage 2	DV_{DD2}	V_{DD}f		3.0	3.3	3.6	V
Supply voltage 3	AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}	V_{DD}g		3.0	3.3	3.6	V
Analog input capacitance	CCDIN	C_{IN}			15		pF
Input voltage	SCK2, SSI2, SEN2, TEST3, TEST4, XSHDI, XSHPI, ADCLKI, CLPOBI, CLPDMI, PBLKI	V_{I+}			1.8		V
		V_{I-}			1.1		V
A/D clock duty	ADCLKI				50		%
Output voltage	D0 to D9	V_{OH}	Feed current where I_{OH} = –2.0mA	V_{DD}e – 0.9			V
		V_{OL}	Pull-in current where I_{OL} = 2.0mA			0.4	V

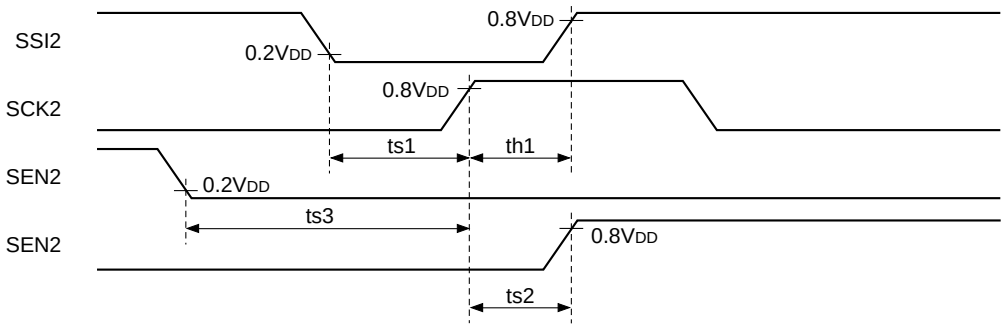
Analog Characteristics

(Fc = 24.3MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Item	Pins	Conditions	Min.	Typ.	Max.	Unit
CCDIN input voltage amplitude	V_{IN}	PGA gain = 0dB, output full scale	900		1100	mV
PGA maximum gain	Gmax	PGA gain setting data = "3FFh"		42		dB
PGA minimum gain	Gmin	PGA gain setting data = "000h"		–6		dB
ADC resolution				10		bit
ADC maximum conversion rate	Fc max		24.3			MHz
ADC integral non-linearity error	E_L	PGA gain = 0dB		±1.0	±5.0	LSB
ADC differential non-linearity error	E_D	PGA gain = 0dB		±0.5	±1.0	LSB
Signal-to-noise ratio	SNR	PGA gain = 0dB		77		dB
CCDIN input voltage clamp level	CLP			1.5		V
CCD optical black signal clamp level	OB	OBLVL = "8h" PGA gain = 0dB		32		LSB

AC Characteristics

AC characteristics between the serial interface clocks

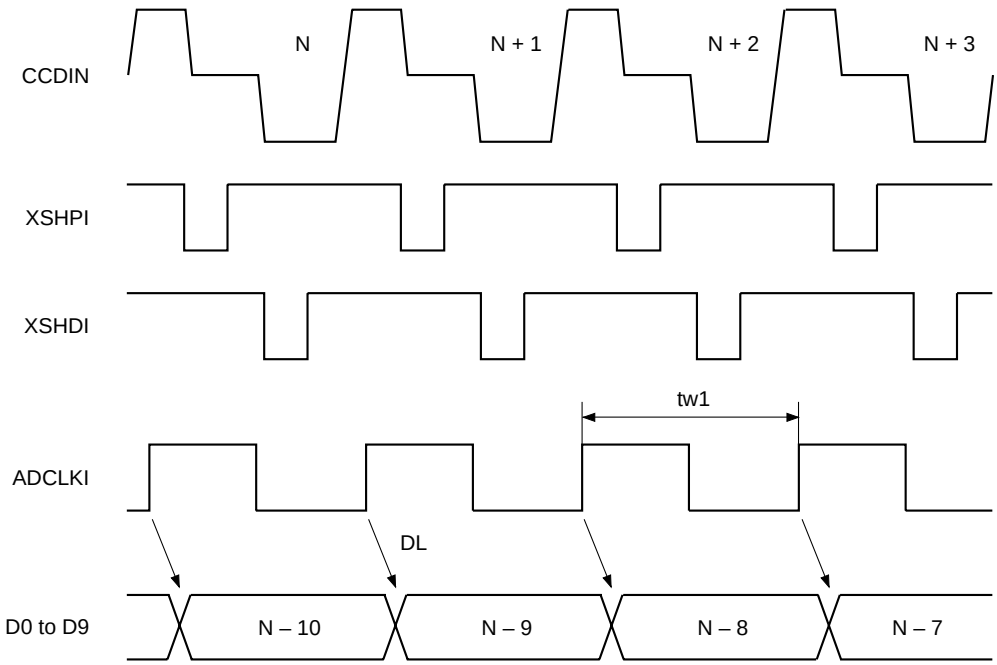


* The setting values are reflected to the operation 6 ADCLKI clocks after the serial data is loaded at the rise of SEN2.

(Fc = 24.3MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tp1	SCK2 clock period	100			ns
ts1	SSI2 setup time, activated by the rise of SCK2	30			ns
th1	SSI2 hold time, activated by the rise of SCK2	30			ns
ts2	SCK2 setup time, activated by the rise of SEN2	30			ns
ts3	SEN2 setup time, activated by the rise of SCK2	30			ns

CDS/ADC Timing Chart

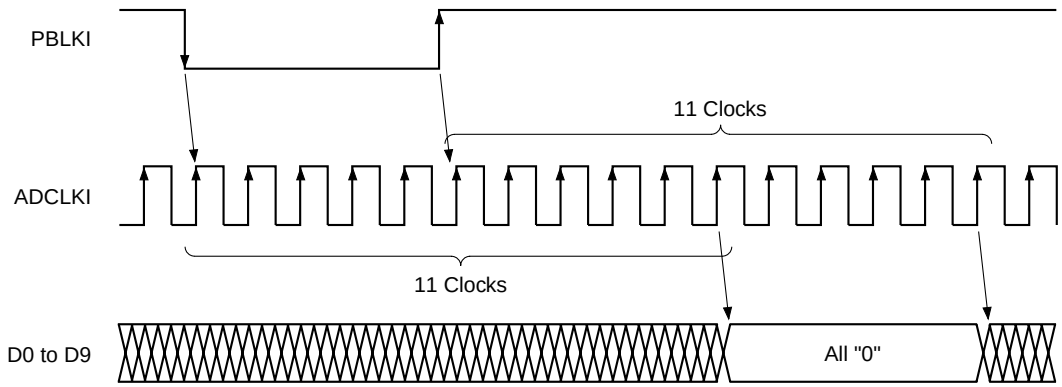


* Set the input pulse polarity setting data D13, D14 and D15 of the serial interface data to "0".

(Fc = 24.3MSPS, $DV_{DD1, 2}$ = $AV_{DD1, 2, 3, 4, 5}$ = 3.3V, Ta = 25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	ADCLKI clock period	41			ns
	ADCLKI clock duty		50		%
DL	Data latency		9		clocks

Preblanking Timing Chart



Description of Operation

Pulses output from the CXD3422GA's timing generator block are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on page 19 and thereafter.

Pin Status Table

Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
A1	NC	—				D8	C2	—			
A2	NC	—				D9	AV_{SS1}	—			
A3	SCK2	—				E1	D9	—			
A4	SSI2	—				E2	DV_{DD1}	—			
A5	TEST3	—				E3	DV_{SS1}	—			
A6	AV_{SS4}	—				E7	AV_{SS2}	—			
A7	C8	—				E8	AV_{DD2}	—			
A8	AV_{SS6}	—				E9	AV_{DD1}	—			
A9	AV_{DD5}	—				F1	DV_{SS2}	—			
B1	D2	—				F2	DV_{SS3}	—			
B2	D1	—				F3	DV_{DD2}	—			
B3	D0	—				F7	PBLKI	—			
B4	SEN2	—				F8	XSHDI	—			
B5	TEST5	—				F9	XSHPI	—			
B6	AV_{DD4}	—				G1	ADCLKI	—			
B7	C7	—				G2	CLPOBI	—			
B8	AV_{DD3}	—				G3	CLPDMI	—			
B9	AV_{SS3}	—				G7	PBLK	ACT	L	L	H
C1	D5	—				G8	XSHD	ACT	L	L	ACT
C2	D4	—				G9	XSHP	ACT	L	L	ACT
C3	D3	—				H1	ADCLK	ACT	L	L	ACT
C4	TEST4	—				H2	CLPOB	ACT	L	L	H
C5	AV_{SS5}	—				H3	CLPDM	ACT	L	L	H
C6	C9	—				H7	TEST1	—			
C7	C3	—				H8	V_{DD4}	—			
C8	C4	—				H9	V_{DD3}	—			
C9	CCDIN	—				J1	CKI	ACT	ACT	ACT	ACT
D1	D8	—				J2	CKO	ACT	ACT	L	ACT
D2	D7	—				J3	V_{SS4}	—			
D3	D6	—				J7	V_{SS3}	—			
D7	C1	—				J8	H1	ACT	L	L	ACT

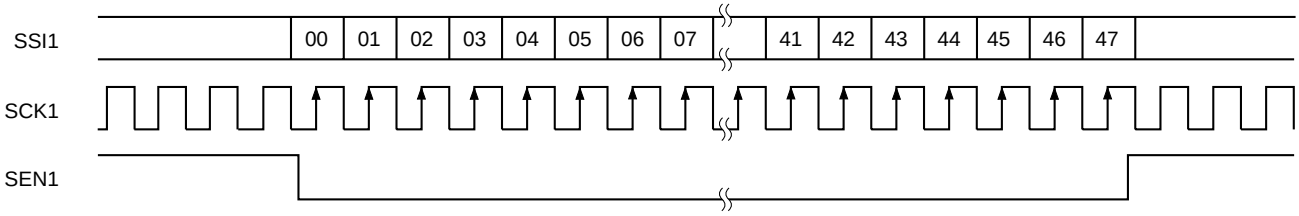
Pin No.	Symbol	CAM	SLP	STB	RST	Pin No.	Symbol	CAM	SLP	STB	RST
J9	H2	ACT	L	L	ACT	M2	VD*1	ACT	L	L	H
K1	OSCO	ACT	ACT	ACT	ACT	M3	VM	—			
K2	MCKO	ACT	ACT	L	ACT	M4	V2 (NC)	ACT	VM	VM	VM
K3	V_{DD5}	—				M5	V5B (V3B)	ACT	VH	VH	VL
K7	V_{DD2}	—				M6	VL	—			
K8	RG	ACT	L	L	ACT	M7	SUB	ACT	VH	VH	VL
K9	V_{SS2}	—				M8	RST	ACT	ACT	ACT	L
L1	OSCI	ACT	ACT	ACT	ACT	M9	WEN/FLD	ACT	L	L	L
L2	SSI1	ACT	ACT	ACT	DIS	N1	SEN1	ACT	ACT	ACT	DIS
L3	TEST2	—				N2	HD*1	ACT	L	L	H
L4	V4 (V2)	ACT	VM	VM	VM	N3	V_{SS5}	—			
L5	VH	—				N4	V5A (V3A)	ACT	VH	VH	VL
L6	V3A (V1A)	ACT	VH	VH	VM	N5	V1 (NC)	ACT	VH	VH	VM
L7	V_{SS1}	—				N6	V3B (V1B)	ACT	VH	VH	VM
L8	SSGSL	ACT	ACT	ACT	ACT	N7	V6 (V4)	ACT	VH	VH	VL
L9	V_{DD1}	—				N8	SNCSL	ACT	ACT	ACT	ACT
M1	SCK1	ACT	ACT	ACT	DIS	N9	ID/EXP	ACT	L	L	L

*1 It is for output. For input, all items are "ACT".

Note) ACT means that the circuit is operating, and DIS means that loading is stopped.
L indicates a low output level, and H a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin L5), VM (Pin M3) and VL (Pin M6), respectively, in the controlled status.

Timing Generator Block Serial Interface Control

The CXD3422GA's timing generator block basically loads and reflects the timing generator block serial interface data sent in the following format in the readout portion at the falling edge of HD. Here, readout portion specifies the horizontal period during which V3A/B and V5A/B, etc. take the ternary value.
Note that some items reflect the timing generator block serial interface data at the falling edge of VD or the rising edge of SEN1.



There are two categories of timing generator block serial interface data: CXD3422GA timing generator block drive control data (hereafter "control data") and electronic shutter data (hereafter "shutter data").
The details of each data are described below.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08	CTG	Category switching	See D08 CTG.		0
D09 to D11	—	—	—	—	All 0
D12, D13	MODE	Drive mode switching	See D12, D13 MODE.		0
D14, D15	—	—	—	—	0
D16	NTPL	Internal SSG function switching*1	NTSC	PAL	0
D17	CCD	CCD switching*1	ICX432	ICX284/434	0
D18, D19	—	—	—	—	0
D20	SMD	Electronic shutter mode switching*2	OFF	ON	0
D21	HTSG	HTSG control switching*2	OFF	ON	0
D22 to D30	—	—	—	—	All 0
D31	FLD	WEN/FLD output switching	WEN	FLD	0
D32	FGOB	Wide CLPOB generation switching	OFF	ON	0
D33	EXP	ID/EXP output switching	ID	EXP	0
D34, D35	PTOB	CLPOB waveform pattern switching	See D34, D35 PTOB.		All 0
D36, D37	LDAD	ADCLK logic phase adjustment	See D36, D37 LDAD.		All 0
D38, D39	STB	Standby control	See D38, D39 STB.		All 0
D40 to D47	—	—	—	—	All 0

*1 See D12, D13 MODE.

*2 See D20 SMD.

Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08	CTG	Category switching	See D08 CTG.		0
D09	—	—	—		0
D10 to D19	SVD	Electronic shutter vertical period specification	See D10 to D19 SVD.		All 0
D20 to D31	SHD	Electronic shutter horizontal period specification	See D20 to D31 SHD.		All 0
D32 to D41	SPL	High-speed shutter position specification	See D32 to D41 SPL.		All 0
D42 to D47	—	—	—		All 0

Detailed Description of Each Data

Shared data: D08 CTG [Category]

Of the data provided to the CXD3422GA by the timing generator block serial interface, the CXD3422GA loads D12 and subsequent data to each data register as shown in the table below according to D08.

D08	Description of operation
0	Loading to control data register
1	Loading to shutter data register

Note that the CXD3422GA can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D12, D13 MODE [Drive mode]

The CXD3422GA drive mode can be switched as follows. However, the drive mode bits are loaded to the CXD3422GA and reflected at the falling edge of VD.

D13	D12	Description of operation
0	0	Draft mode (default)
0	1	Frame mode
1	0	AF mode*1
1	1	Test mode

*1 The test mode results in ICX284/434 mode.

Draft mode is the pulse elimination drive mode. This is a high frame rate drive mode that can be used for purposes such as monitoring and moving pictures.
AF mode is the drive mode for applications with an even higher frame rate, and is used for auto focus (AF).
Frame mode is the drive mode in which the data for all lines of the ICX284/432/434 are read.

Control data: D16 NTPL [SSG function switching]

The CXD3422GA internal SSG output pattern can be switched as follows. However, the drive mode bits are loaded to the CXD3422GA and reflected at the falling edge of VD. The default is "NTSC".

D16	Description of operation
0	NTSC equivalent pattern output (internal SSG)
1	PAL equivalent pattern output (internal SSG)

Control data: D17 CCD [Used CCD switching]

This specifies the CCD image sensor to be used. However, like the drive mode bits, the CCD switching bits are loaded to the CXD3422GA and reflected at the falling edge of VD. The default is "ICX432".

D17	Description of operation
0	ICX432
1	ICX284/ICX434

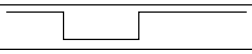
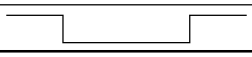
Control data: D32 FGOB [Wide CLPOB generation]

This controls wide CLPOB generation during the vertical OPB period. See the Timing Charts for the actual operation. The default is "OFF".

D32	Description of operation
0	Wide CLPOB generation OFF
1	Wide CLPOB generation ON

Control data: D34, D35 PTOB [CLPOB waveform pattern]

This indicates the CLPOB waveform pattern. The default is "Normal".

D35	D34	Waveform pattern
0	0	 (Normal)
0	1	 (Shifted rearward)
1	0	 (Shifted forward)
1	1	 (Wide)

Control data: D36, D37 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is "90°" relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: D38, D39 STB [Standby]

The operating mode is switched as follows. However, the standby bits are loaded to the CXD3422GA and control is applied immediately at the rising edge of SEN1.

D39	D38	Symbol	Operating mode
X	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	1	STB	Standby mode

See the Pin Status Table for the pin status in each mode.

Control data/shutter data: [Electronic shutter]

The CXD3422GA realizes various electronic shutter functions by using control data D20 SMD and D21 HTSG and shutter data D10 to D19 SVD, D20 to D31 SHD and D32 to D41 SPL.
These functions are described in detail below.
First, the various modes are shown below. These modes are switched using control data D20 SMD.

D20	Description of operation
0	Electronic shutter stopped mode
1	Electronic shutter mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHD as an example. However, MSB (D31) is a reserve bit for the future specification, and it is handled as a dummy on this IC.

MSB											LSB
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

→ SHD is expressed as 1C3h.

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.
SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[High-speed/low-speed shutter mode]

During this mode, the shutter data items have the following meanings.

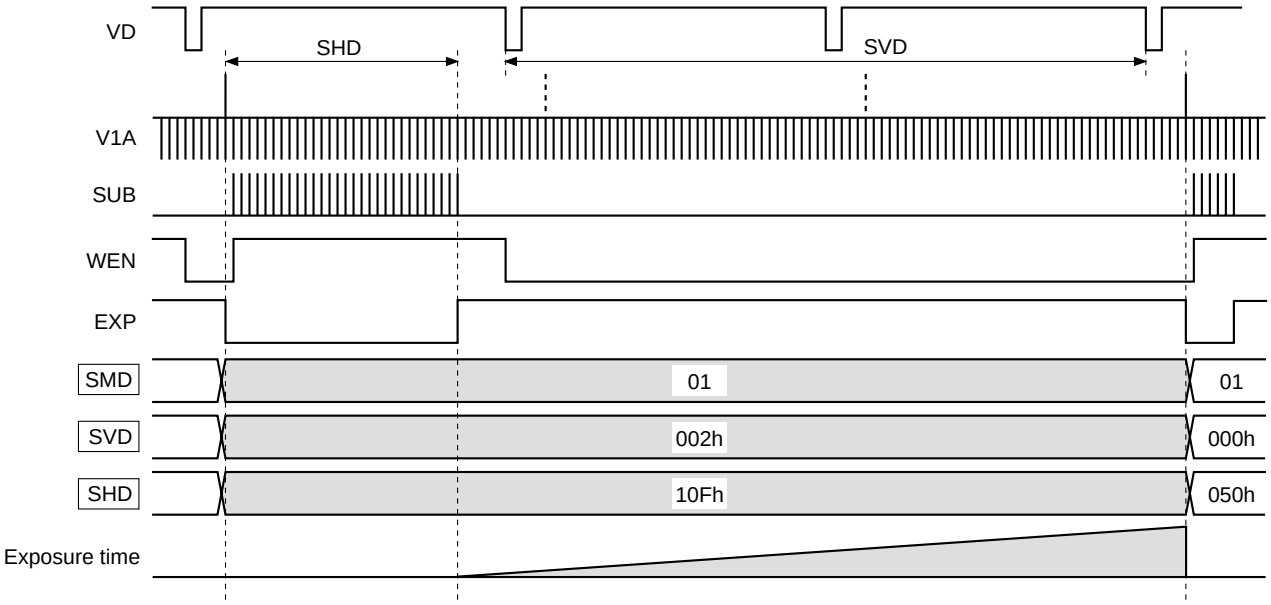
Symbol	Data	Description
SVD	D10 to D19	Number of vertical periods specification (000h ≤ SVD ≤ 3FFh)
SHD	D20 to D31	Number of horizontal periods specification (000h ≤ SHD ≤ 7FFh)
SPL	D32 to D41	Vertical period specification for high-speed shutter operation (000h ≤ SPL ≤ 3FFh)

Note) The bit data definition area is assured in terms of the CXD3422GA functions, and does not assure the CCD characteristics.

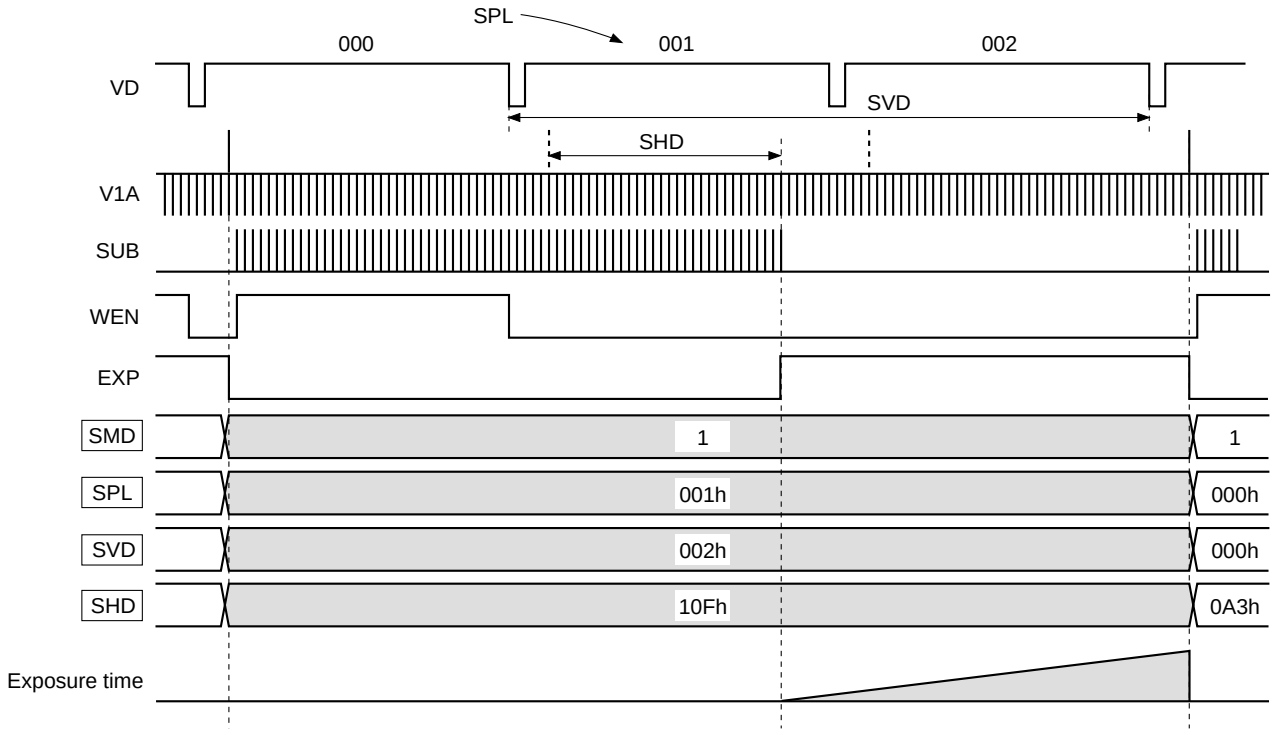
The period during which SVD and SHD are specified together is the shutter speed. An image of the exposure time calculation formula is shown below. In actual operation, the precise exposure time is calculated from the operating frequency, VD and HD periods, decoding value during the horizontal period, and other factors.

$$\text{(Exposure time)} = \text{SVD} \times \text{(1V period)} + \{\text{(number of HD per 1V)} - \text{(SHD + 1)}\} \times \text{(1H period)} + \text{(distance from SUB to SG during the readout period)}$$

Concretely, when specifying high-speed shutter, SVD is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVD is set to "001h" or higher, the serial interface data is not loaded until this period is finished.
The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHD can be considered as (number of SUB pulses – 1).



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.
In the case below, SUB is output based on SHD at the SPL vertical period out of (SVD + 1) vertical periods.

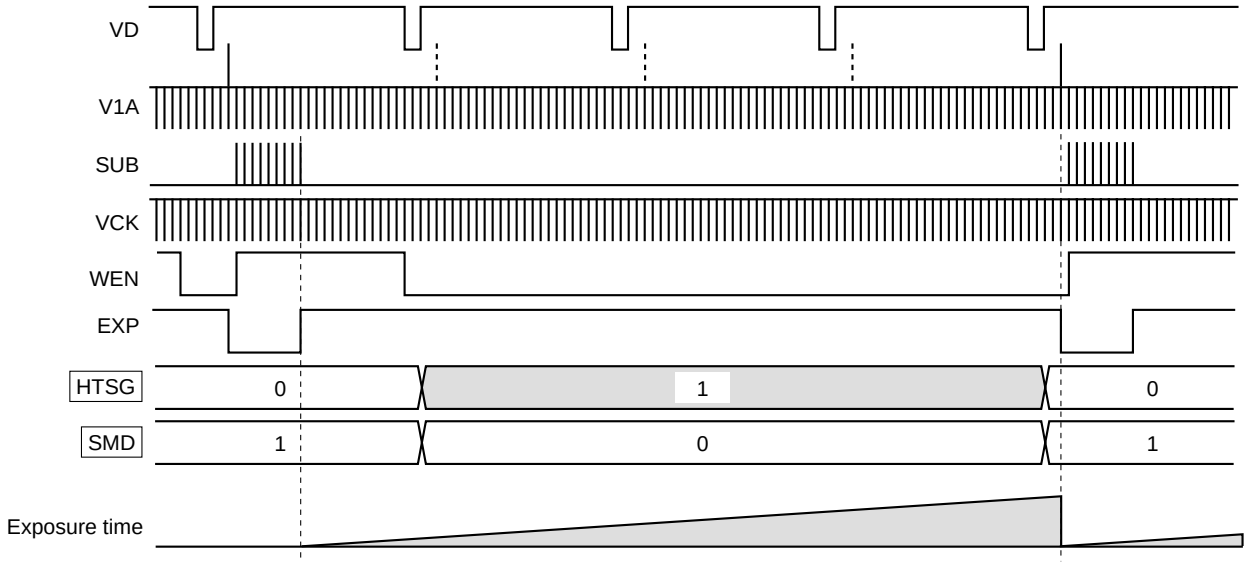


Incidentally, SPL is counted as "000h", "001h", "002h" and so on in conformance with SVD.
Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

[HTSG control mode]

This mode controls the ternary level outputs of V1,V3A/B,V5A/B (readout pulse block) using D21 HTSG.

D21	Description of operation
0	Readout pulse (SG) normal operation
1	HTSG control mode



[EXP pulse]

The ID/EXP pin (Pin N9) output can be switched between the ID pulse or the EXP pulse using D33 EXP. The default is the "ID" pulse. See the Timing Charts for the ID pulse. The EXP pulse indicates the exposure time when it is high. In principle, the transition points are the last SUB pulse falling edge and the readout pulse falling edge, that is to say from the time the charge is completely discharged until transfer ends. However, when the readout pulse timing differs within the same readout portion such as in draft mode, the average value is used. Then, when there is no SUB pulse in the next field, the readout pulse falling edge is defined as the start position, but in this case the transition points overlap and disappear, so a tentative start position is defined.

This is shown below.

		SG↓	Tentative start position
[ICX432]	Frame mode	1460	1480
	Draft/AF mode	1682	1784
[ICX284/434]	Frame mode	A: 1071	1091
		B: 1175	1195
	Draft mode	1123	1175

See the EXP pulse indicated in the explanatory diagrams under [Electronic shutter] for an image of operation.

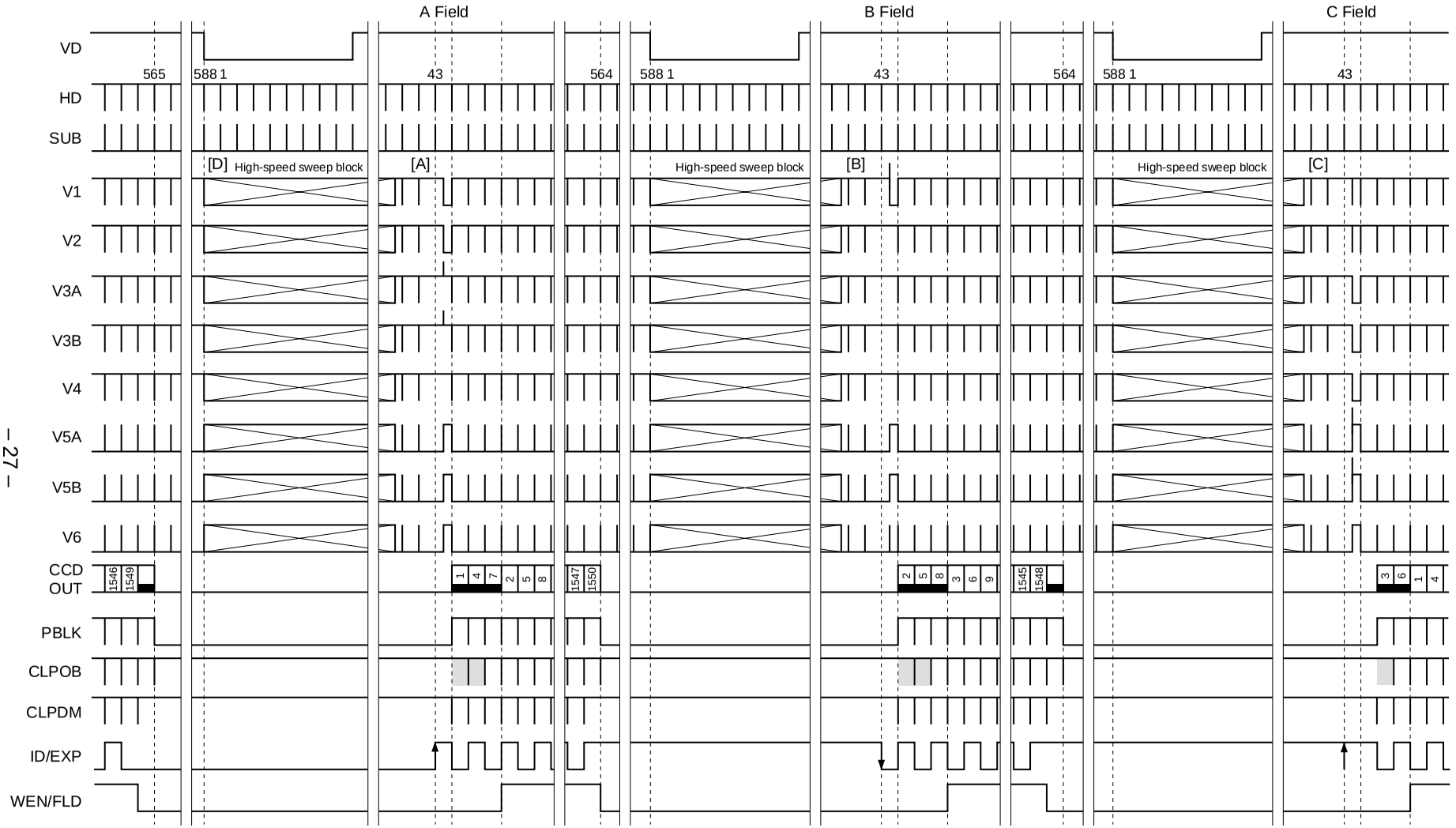
Chart-A1 Vertical Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX432



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to (high, low, low) in the horizontal periods of each readout portion (A, B, C).
* WEN/FLD of this chart shows WEN.
* The shaded portion of CLPOB shows the range over which the wide CLPOB can be set by the serial interface data.
* VD of this chart is indicated in NTSC equivalent pattern 587H (1H: 2760ck) + 1500ck units. For PAL equivalent pattern, it is 704H + 960ck units.

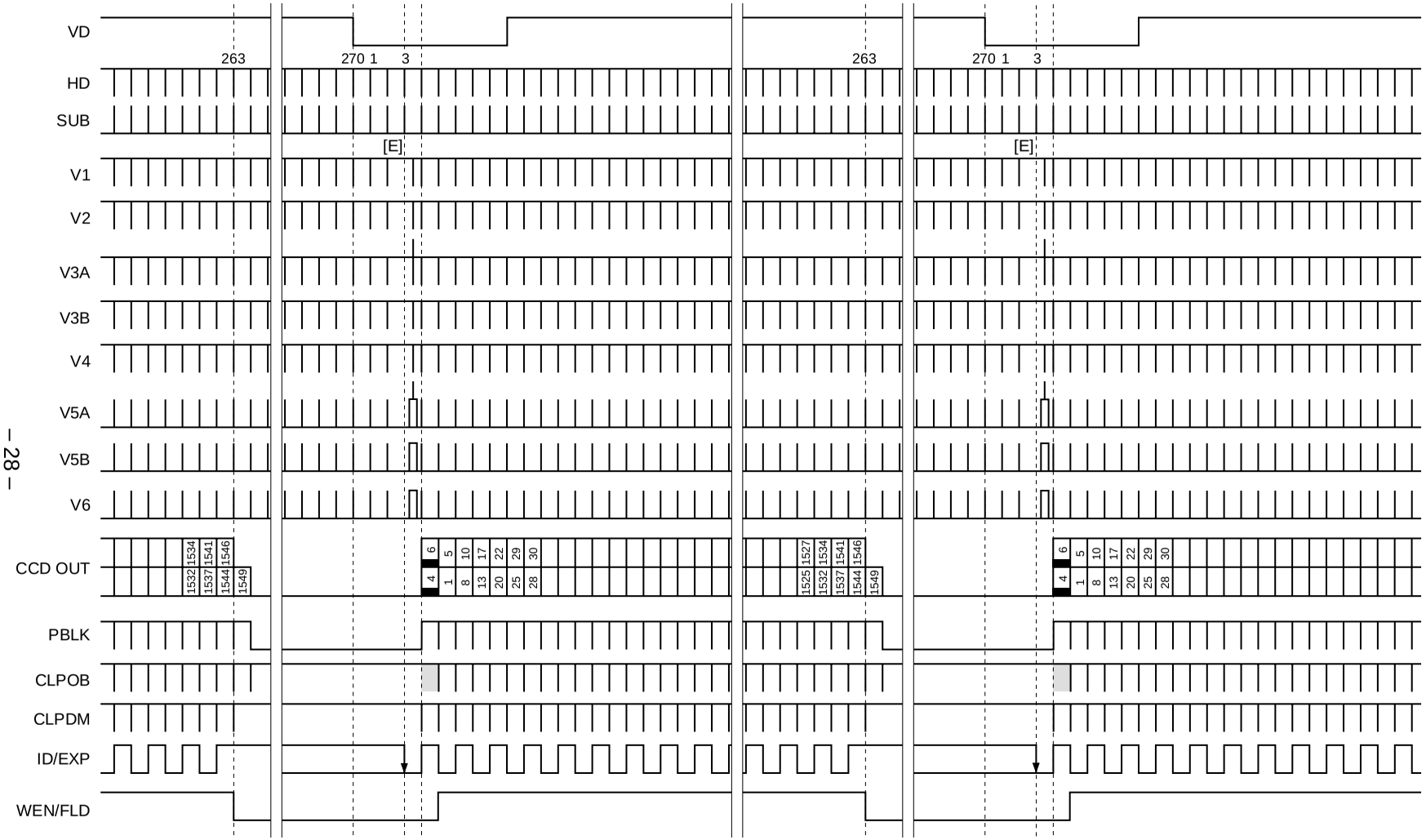
Chart-A2 Vertical Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX432



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to low in the horizontal periods of each readout portion (E).
* WEN/FLD of this chart shows WEN.
* The shaded portion of CLPOB shows the range over which the wide CLPOB can be set by the serial interface data.
* VD of this chart is indicated in NTSC equivalent pattern 269H (1H: 3004ck) + 2734ck units. For PAL equivalent pattern, it is 323H + 1708ck units.

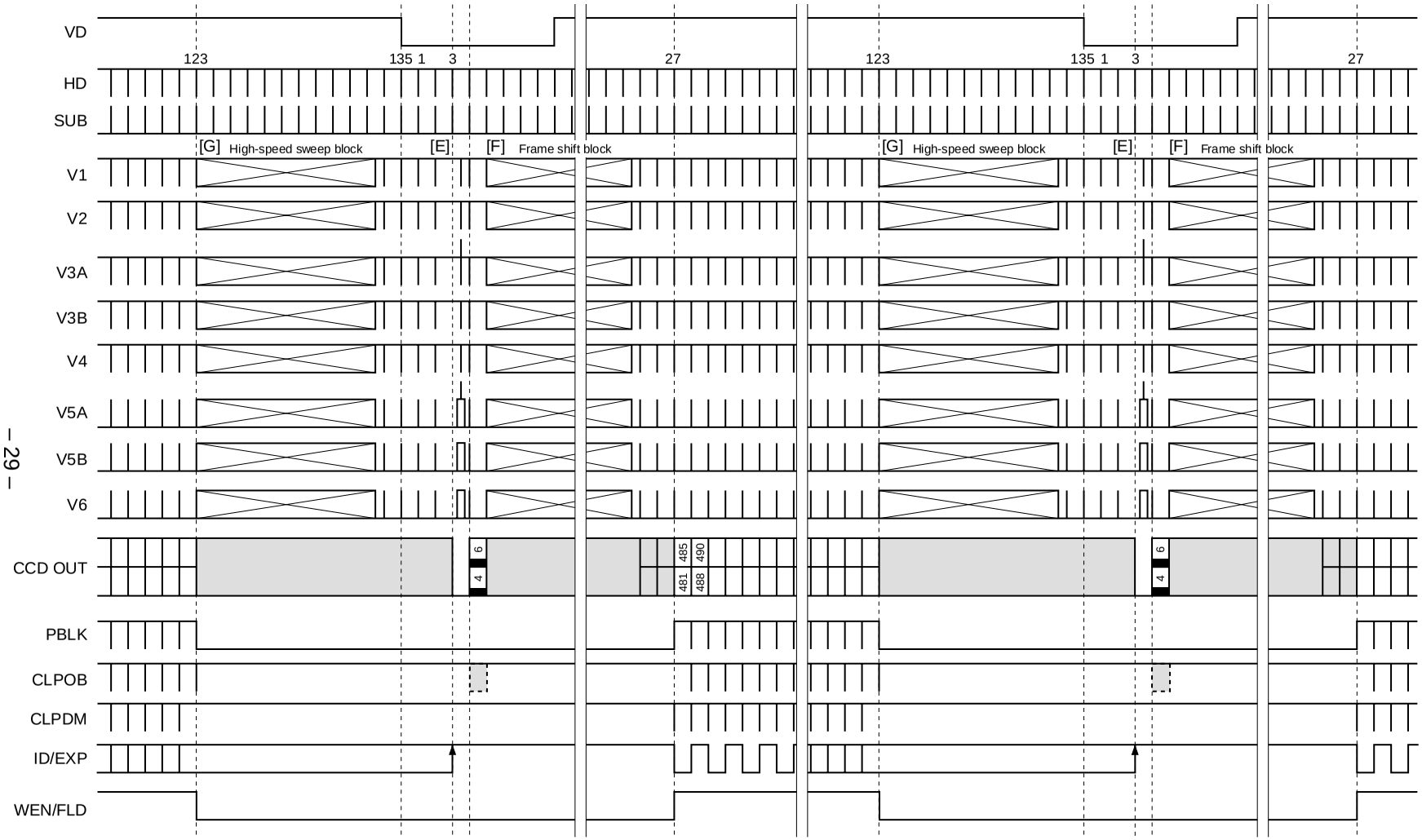
Chart-A3 Vertical Direction Timing Chart

MODE

AF mode

Applicable CCD image sensor

• ICX432



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to high in the horizontal periods of each readout portion (E).
* WEN/FLD of this chart shows WEN.
* The shaded portion of CLPOB shows the range over which the wide CLPOB can be set by the serial interface data.
* VD of this chart is indicated in NTSC equivalent pattern 134H (1H: 3004ck) + 2869ck units. For PAL equivalent pattern, it is 161H + 2356ck units. In addition, for PAL equivalent pattern, the high-speed sweep block starts from 150H.

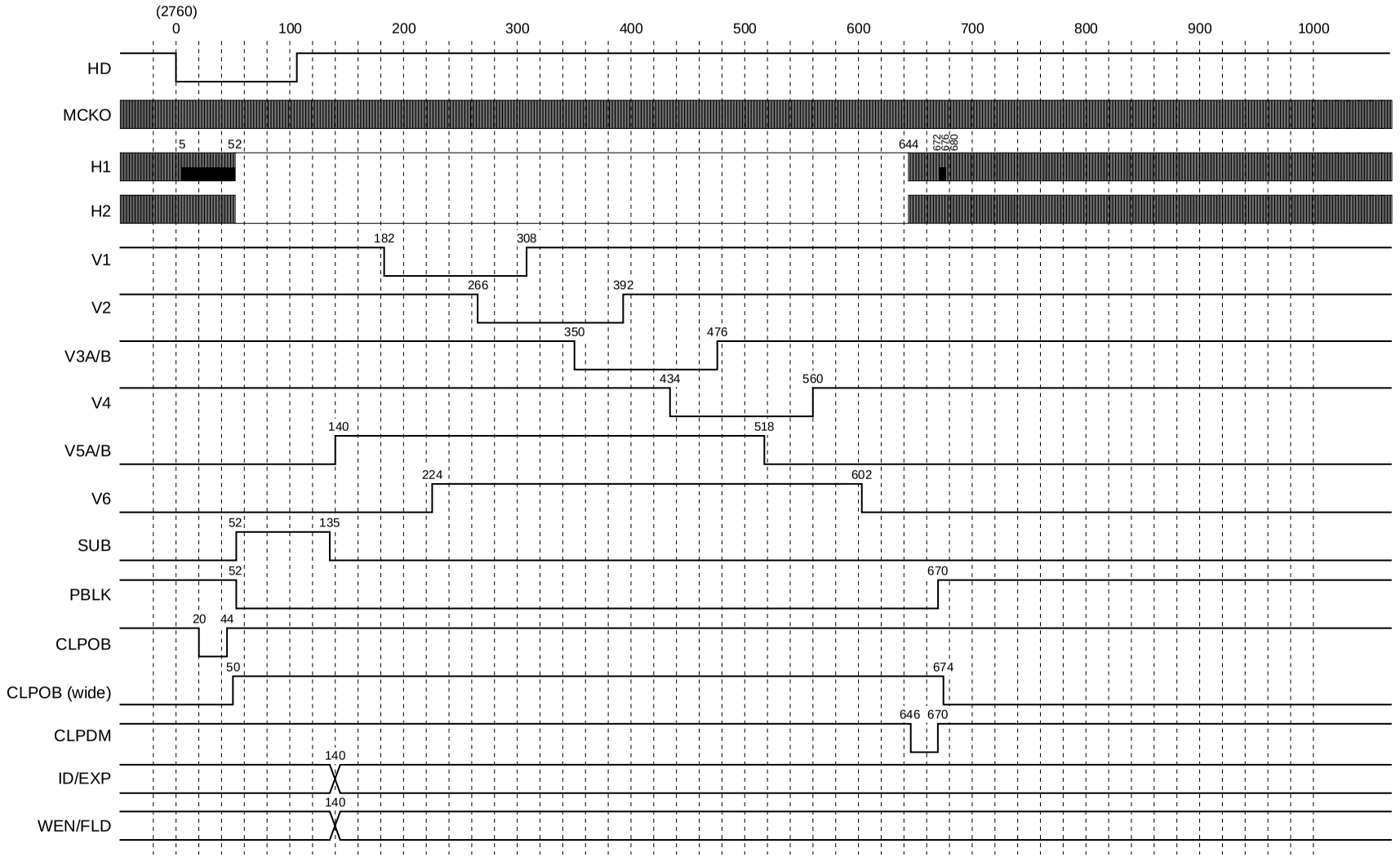
Chart-A4 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-A1.
* CLPOB also has patterns of 14-38, 26-50 and 14-50 for a total of four patterns. CLPOB (wide) is output in the shaded portions shown in Chart-A1. These timings can be switched by the serial interface data.

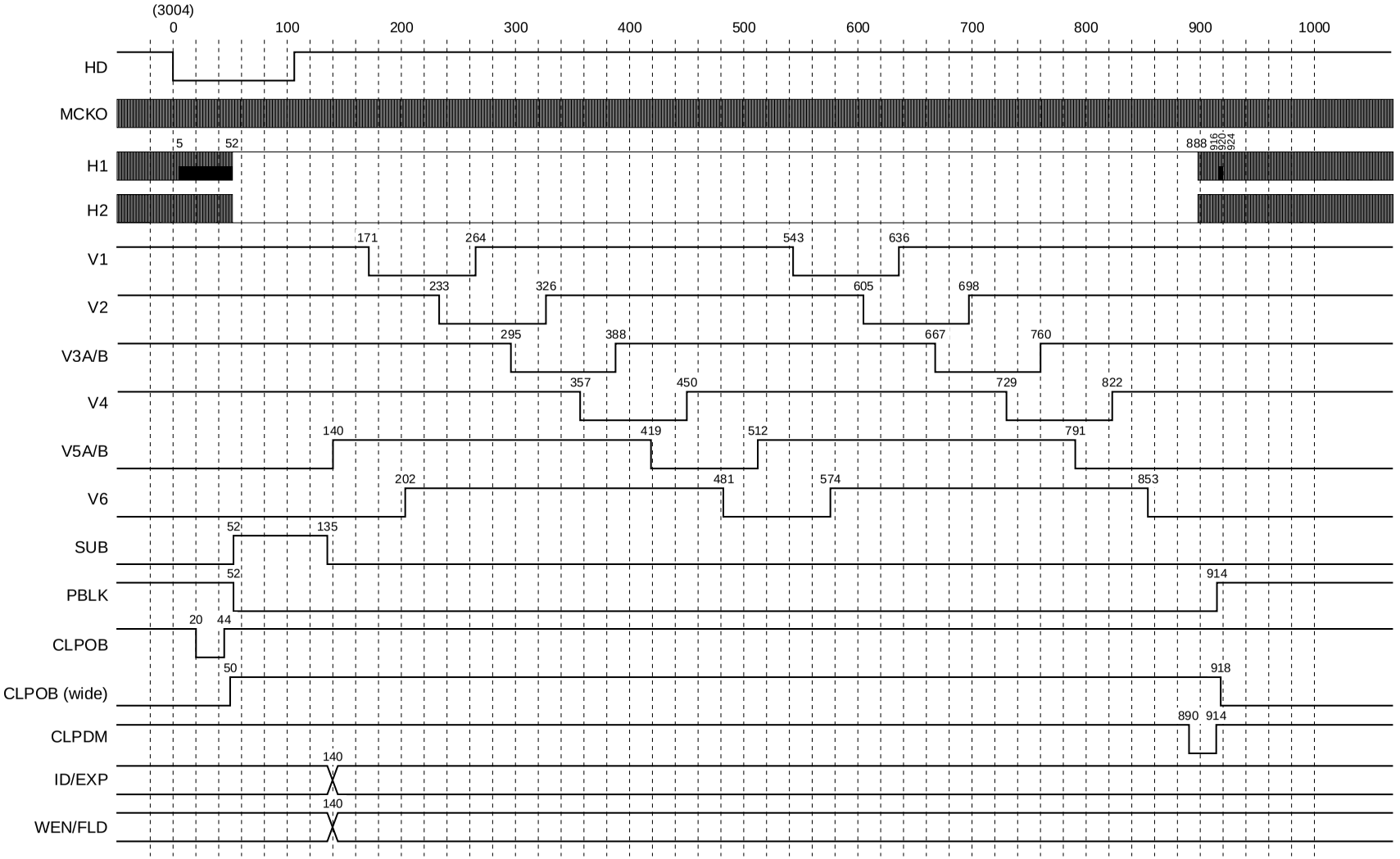
Chart-A5 Horizontal Direction Timing Chart

MODE

Draft/AF mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-A2 and A3.
* CLPOB also has patterns of 14-38, 26-50 and 14-50 for a total of four patterns. CLPOB (wide) is output in the shaded portions shown in Chart-A2 and A3. These timings can be switched by the serial interface data.

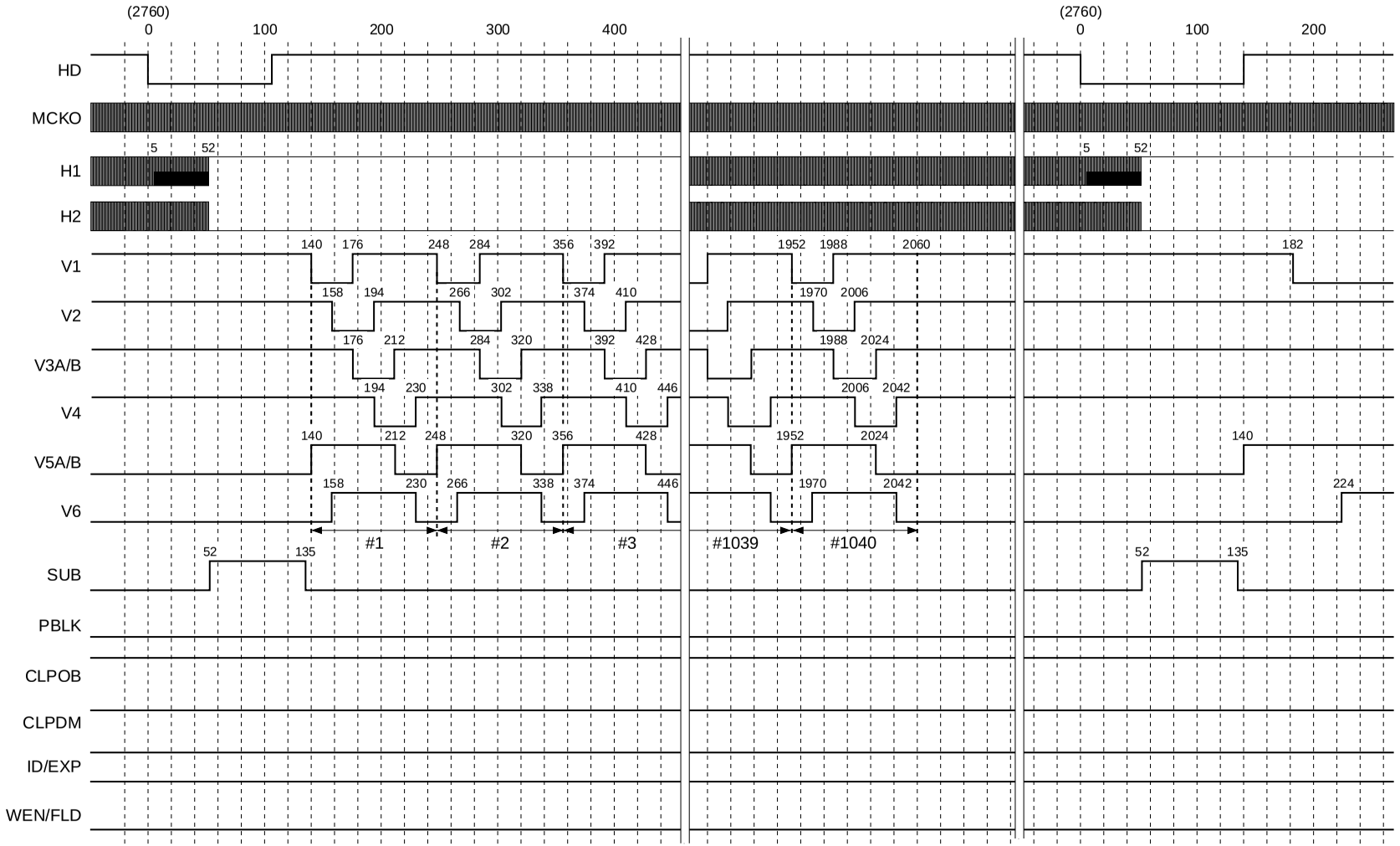
Chart-A6 Horizontal Direction Timing Chart (High-speed sweep: D)

MODE

Frame mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

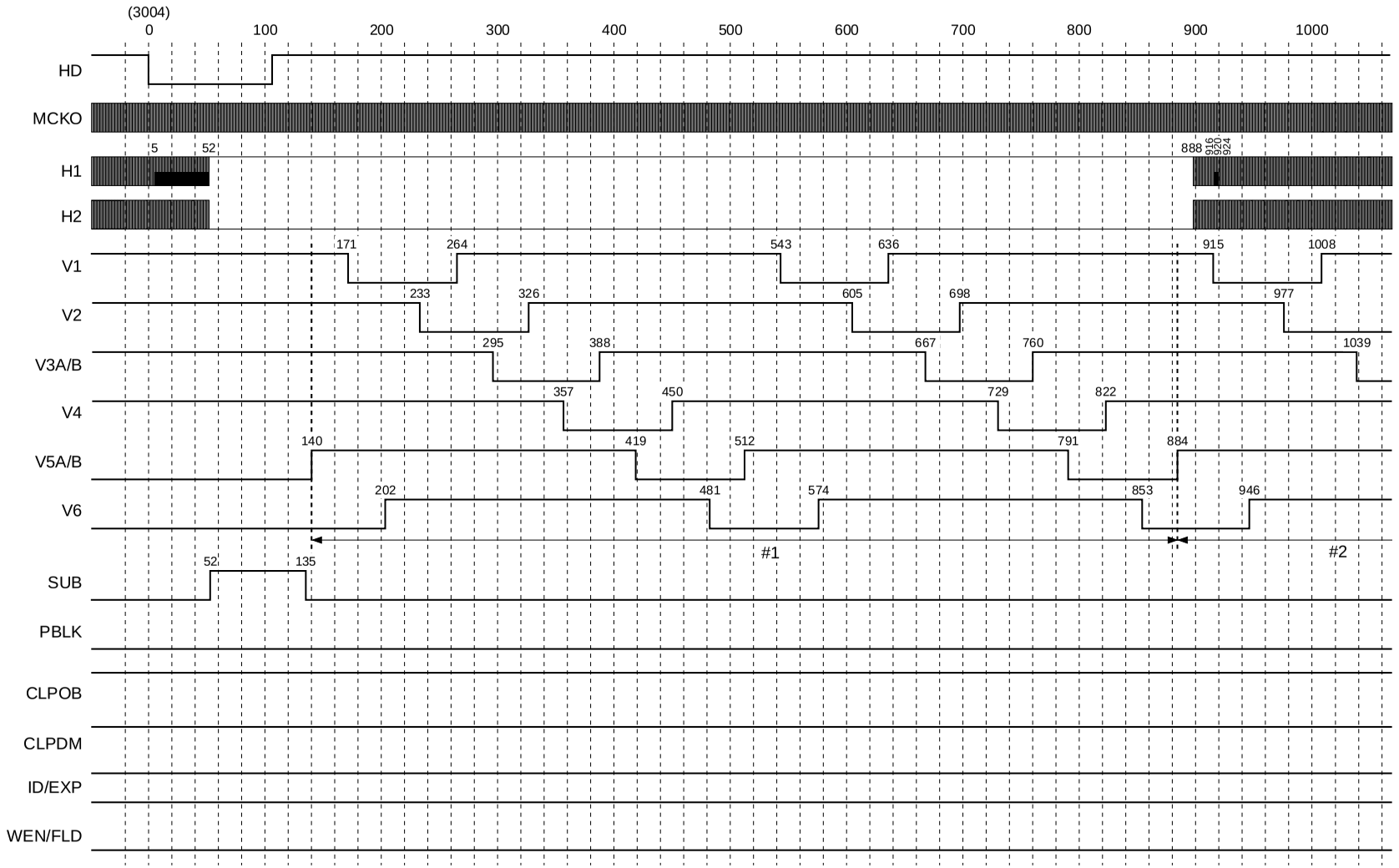
Chart-A7 Horizontal Direction Timing Chart (Frame shift: F)

MODE

AF mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* Frame shift of V1, V2, V3A/B, V4, V5A/B and V6 is performed up to 24H 1096ck (#78).

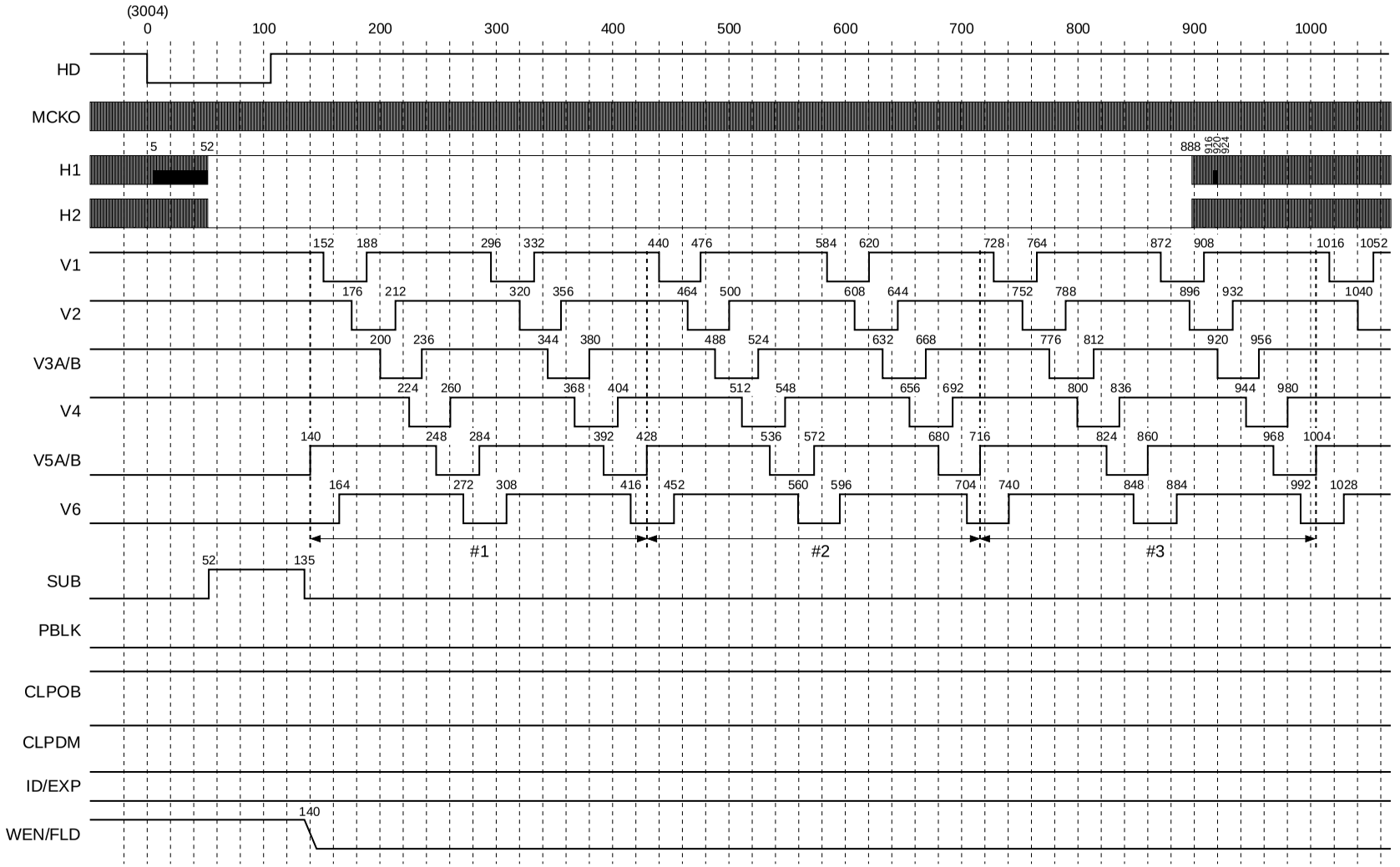
Chart-A8 Horizontal Direction Timing Chart (High-speed sweep: G)

MODE

AF mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1, V2, V3A/B, V4, V5A/B and V6 is performed up to 133H 2932ck (#114).

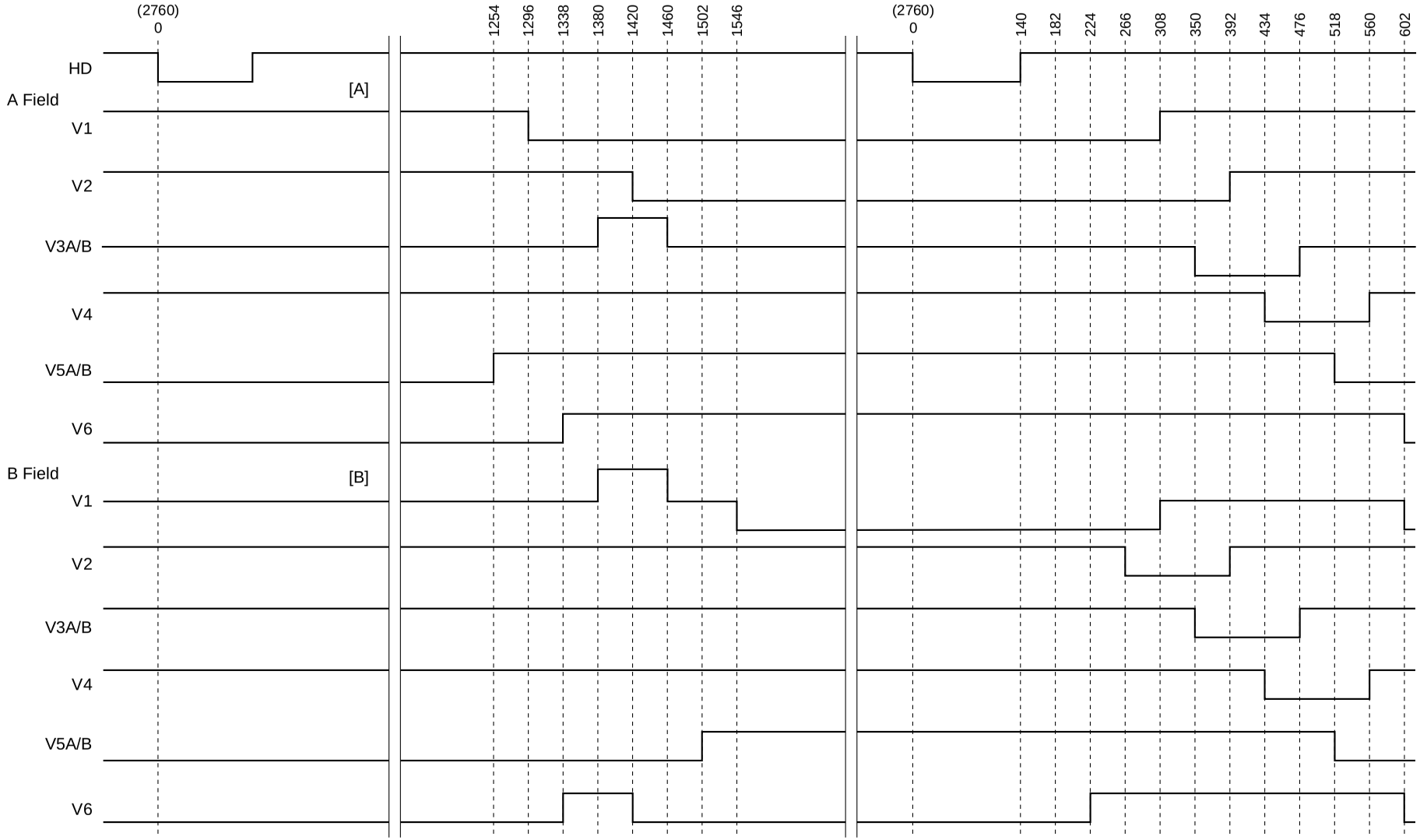
Chart-A9a Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX432



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

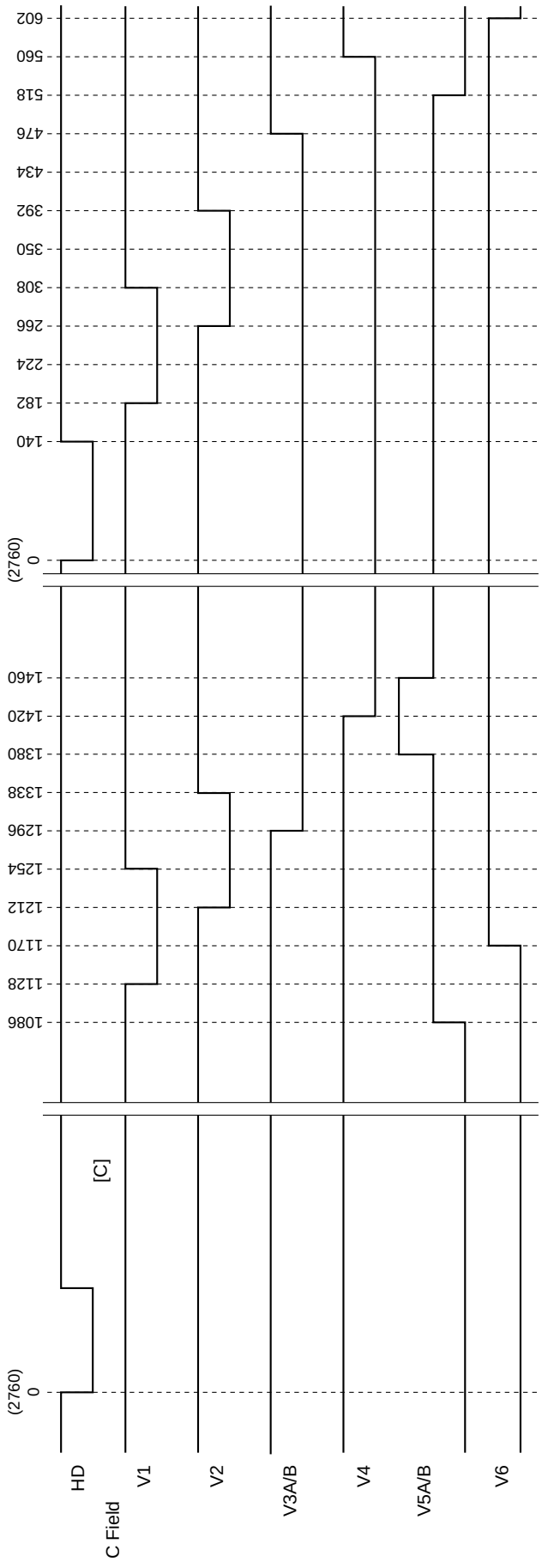
Chart-A9b Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX432

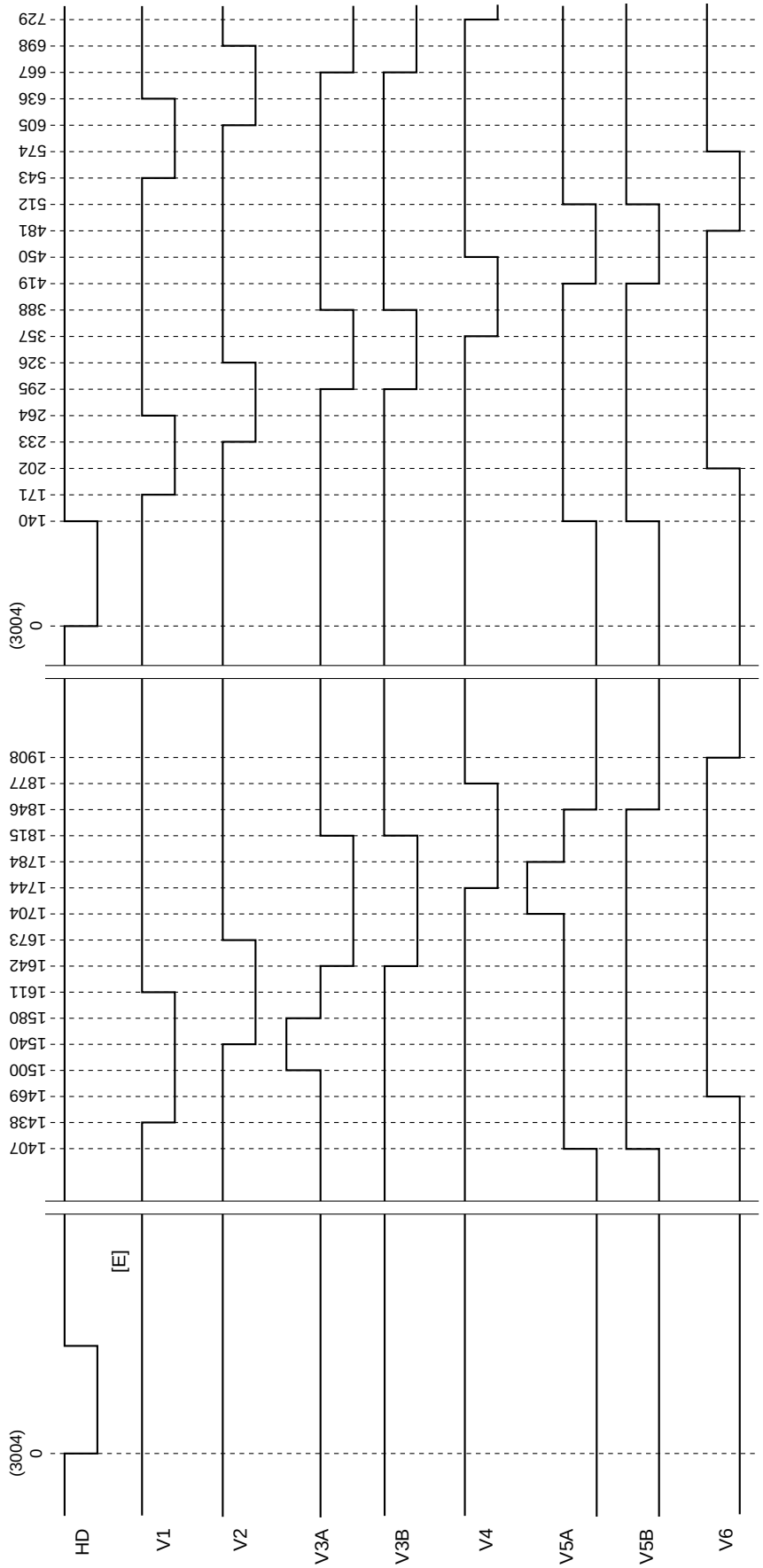


* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

Chart-A10 Horizontal Direction Timing Chart

Applicable CCD image sensor
• ICX432

MODE
Draft/AF mode



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

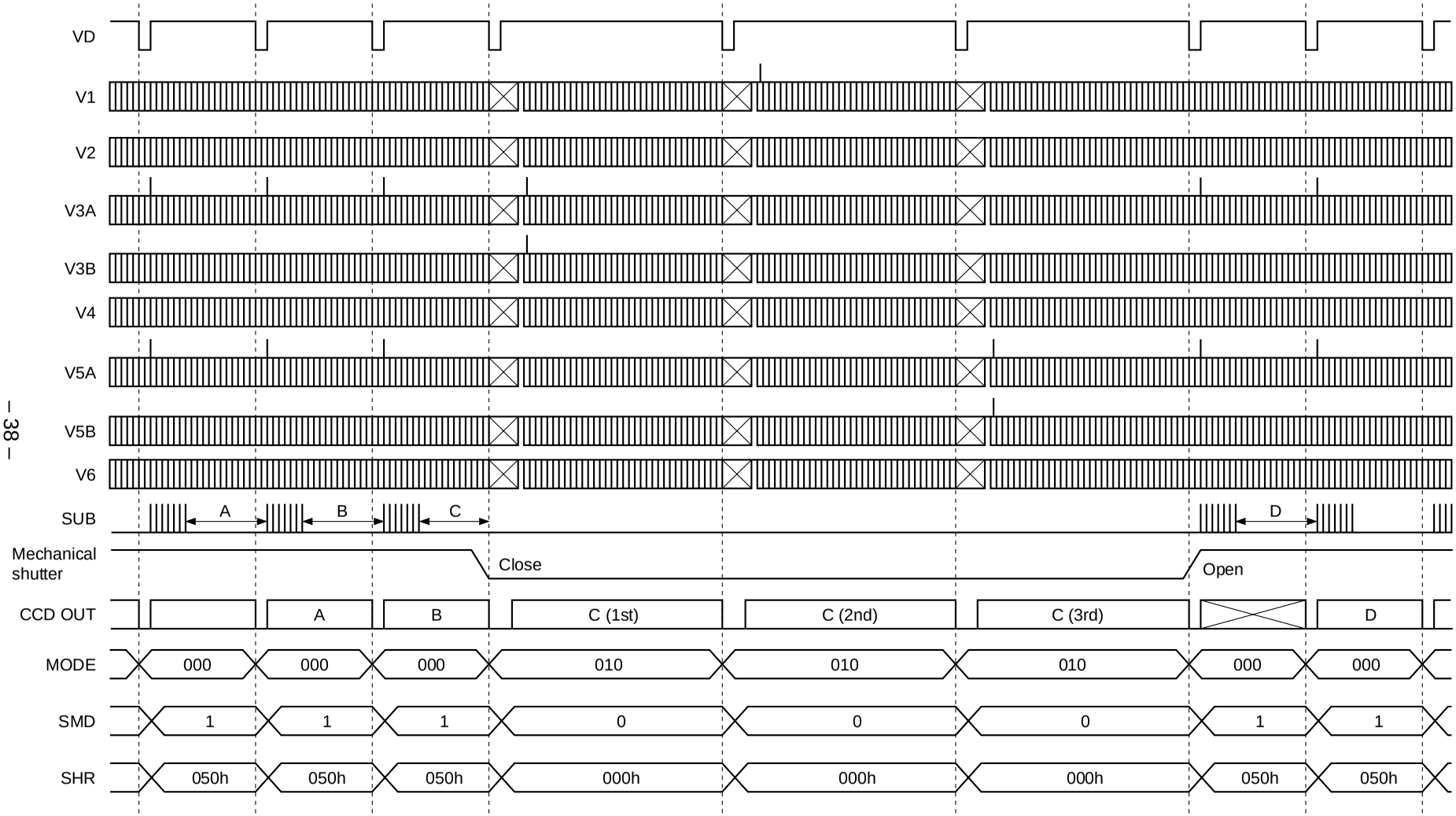
Chart-A11 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

Applicable CCD image sensor

• ICX432



* This chart is a driving timing chart example of electronic shutter normal operation.
* Data exposed at B includes a blooming component. For details, see the CCD image sensor data sheet.
* The CXD3422GA does not generate the pulse to control mechanical shutter operation.
* The drive mode and the electronic shutter data are not switched at the same timing.

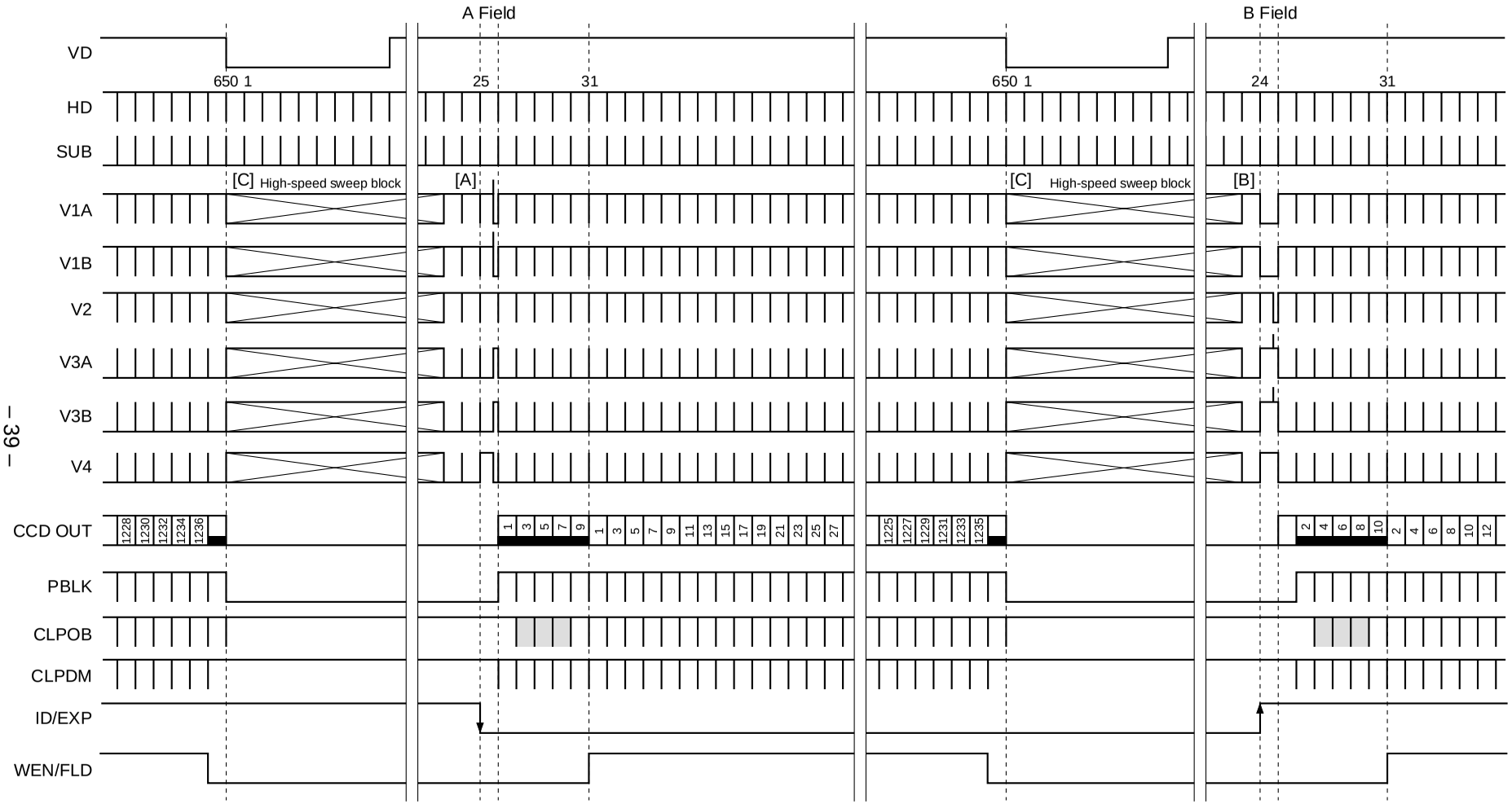
Chart-B1 Vertical Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to (high, low) in the horizontal periods of each readout portion (A, B).
* WEN/FLD of this chart shows WEN.
* VD of this chart is indicated in NTSC equivalent pattern 650H (1H: 1848ck) units. For PAL equivalent pattern, it is 779H + 408ck units.
* This chart shows the pin configuration for the ICX434. (See page 3.)

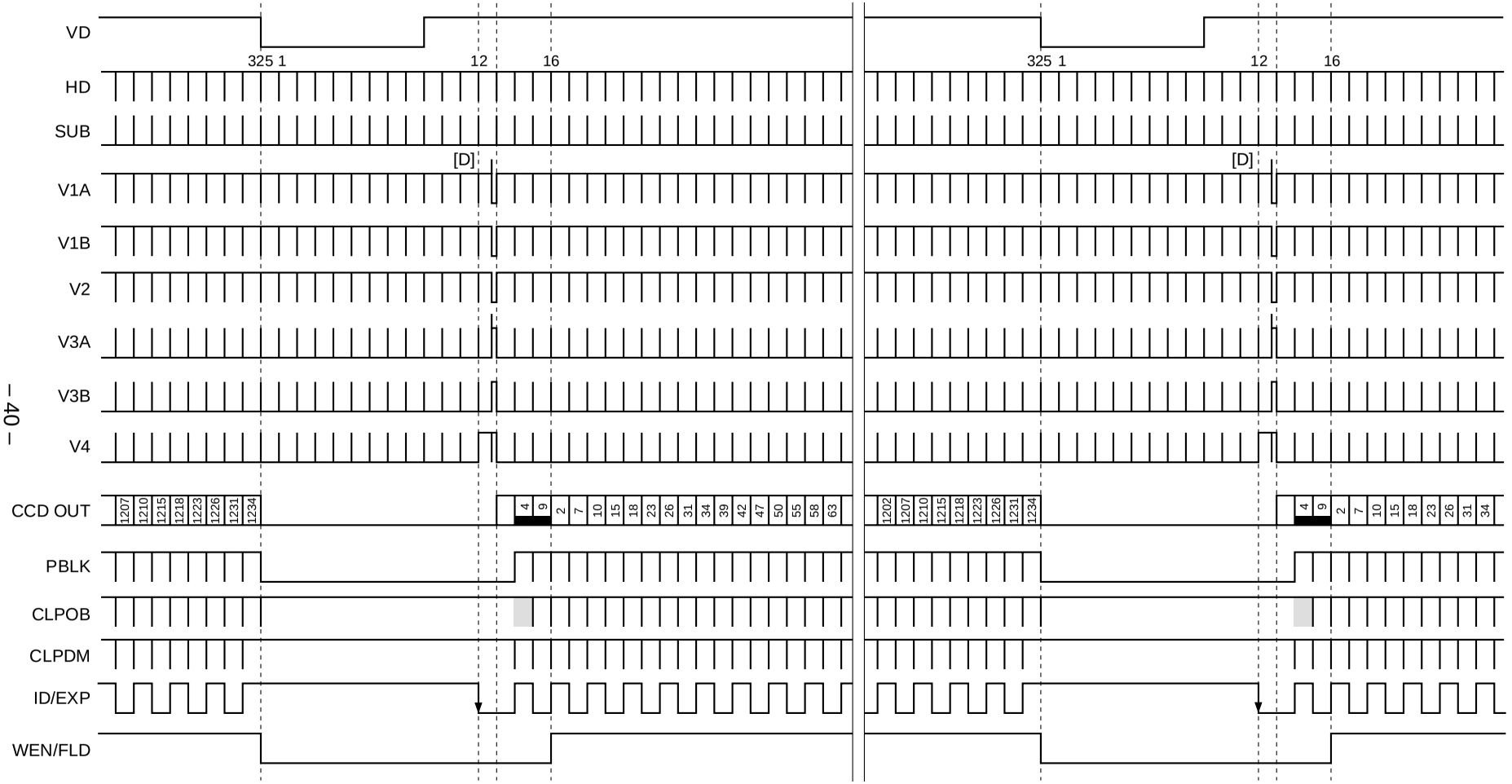
Chart-B2 Vertical Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX434



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to high in the horizontal periods of each readout portion (D).
* WEN/FLD of this chart shows WEN.
* VD of this chart is indicated in NTSC equivalent pattern 325H (1H: 1848ck) units. For PAL equivalent pattern, it is 389H + 1128ck units.
* This chart shows the pin configuration for the ICX434. (See page 3.)

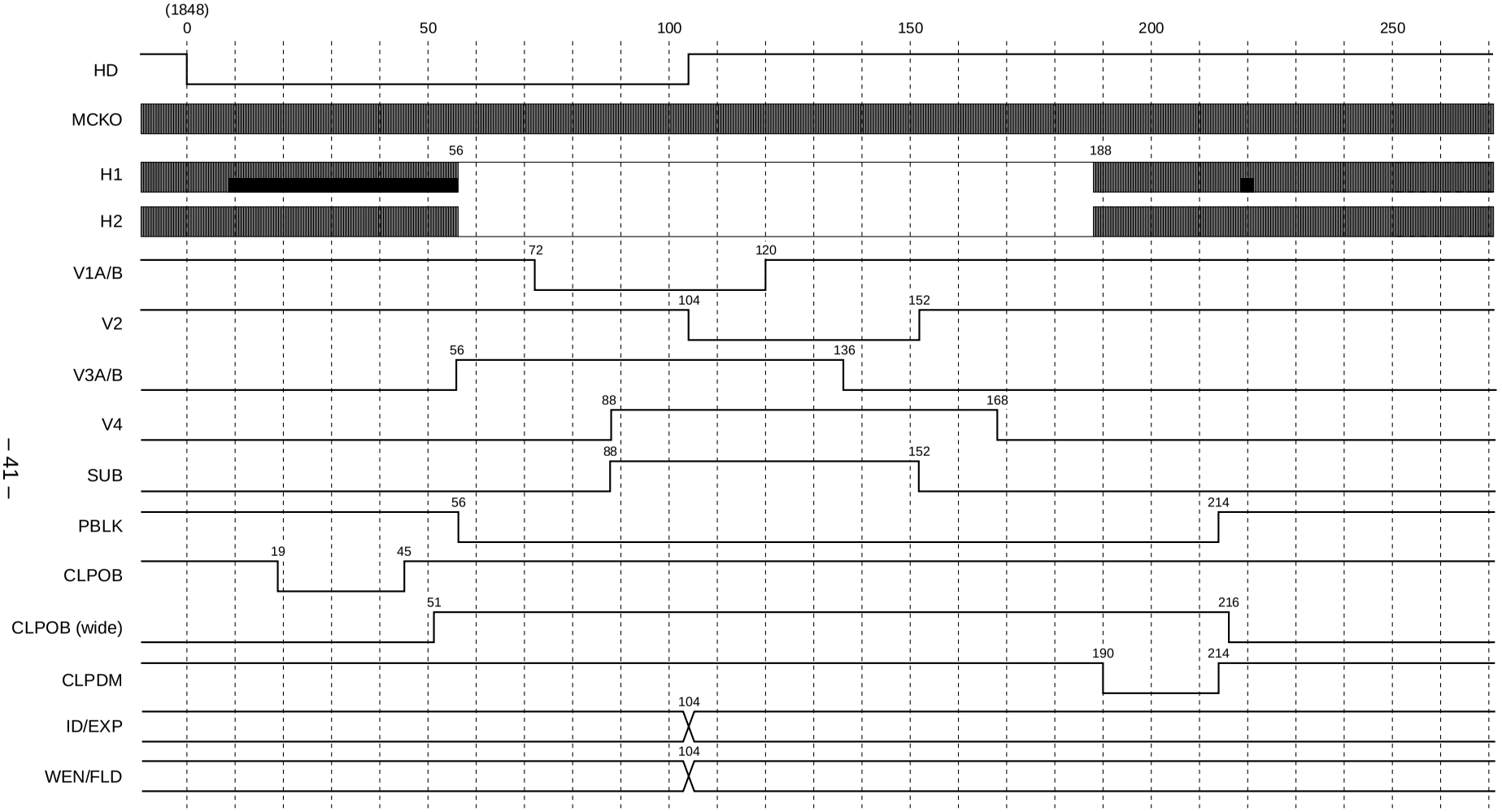
Chart-B3 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B1.
* CLPOB also has patterns of 13-39, 25-51 and 13-51 for a total of four patterns. CLPOB (wide) is output in the shaded portions shown in Chart-B1. These timings can be switched by the serial interface data.
* This chart shows the pin configuration for the ICX434. (See page 3.)

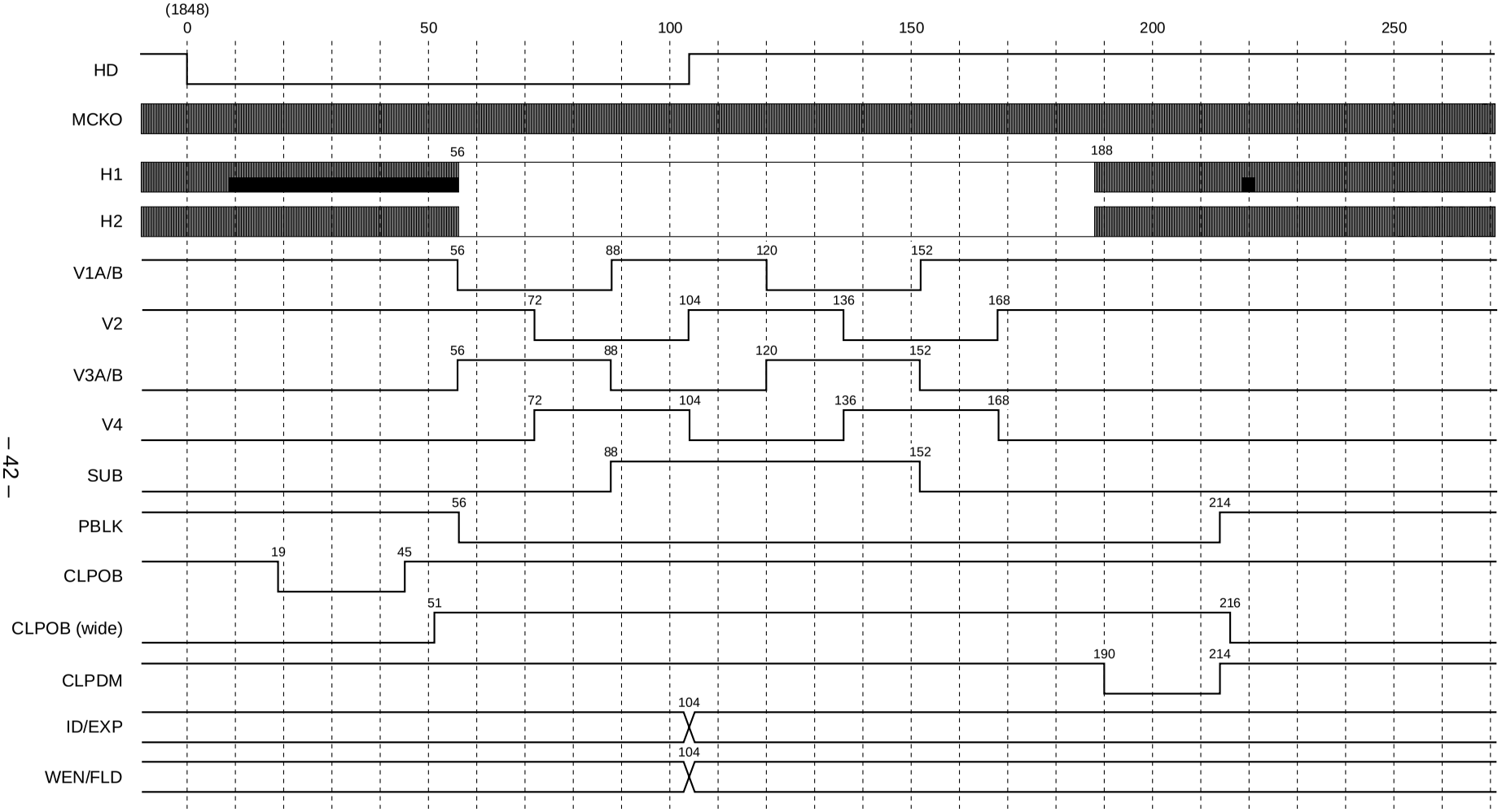
Chart-B4 Horizontal Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX434



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B2.
* CLPOB also has patterns of 13-39, 25-51 and 13-51 for a total of four patterns. CLPOB (wide) is output in the shaded portions shown in Chart-B2. These timings can be switched by the serial interface data.
* This chart shows the pin configuration for the ICX434. (See page 3.)

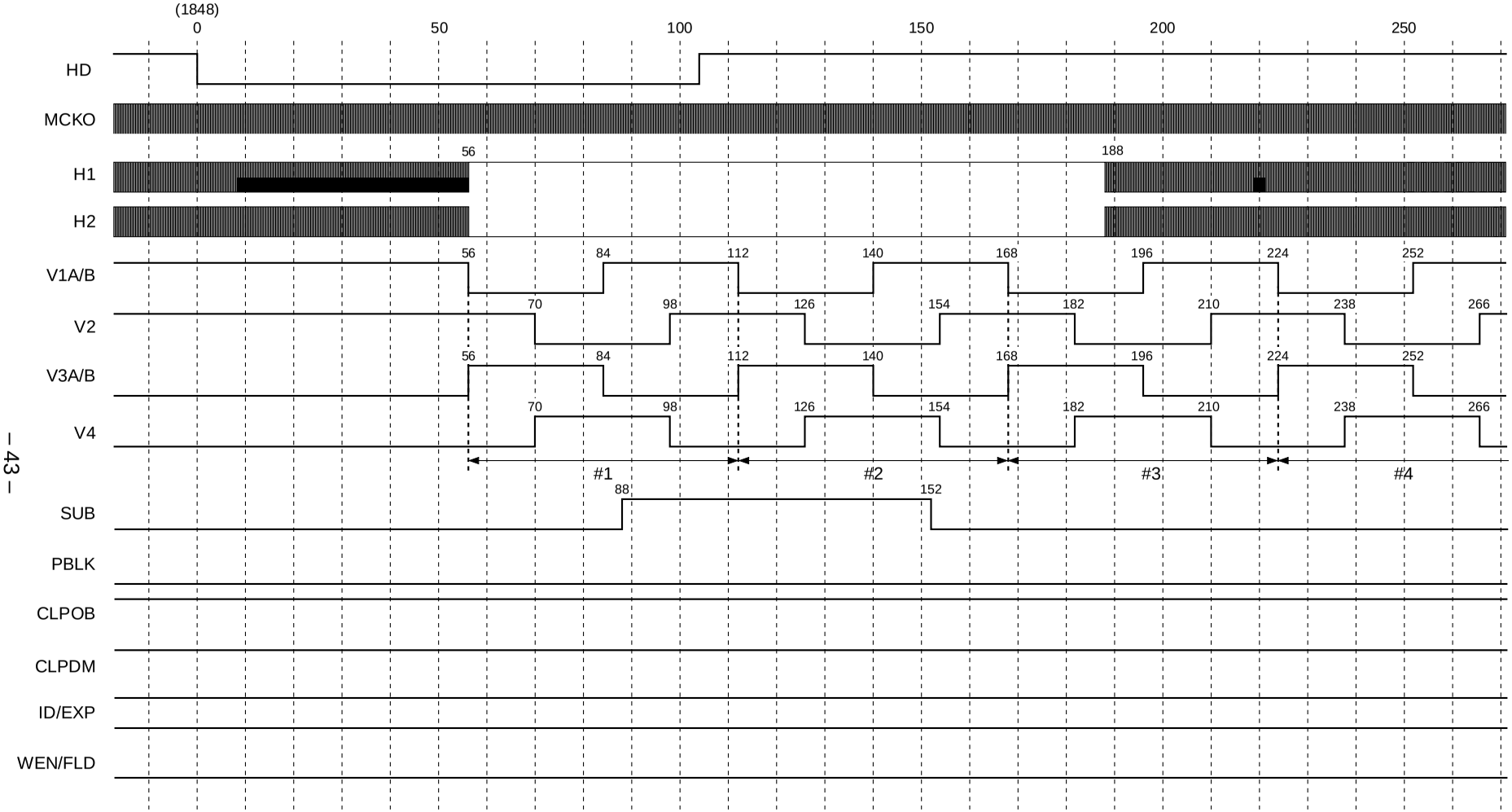
Chart-B5 Horizontal Direction Timing Chart (High-speed sweep: C)

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B1.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 22H 1848ck (#758).
* This chart shows the pin configuration for the ICX434. (See page 3.)

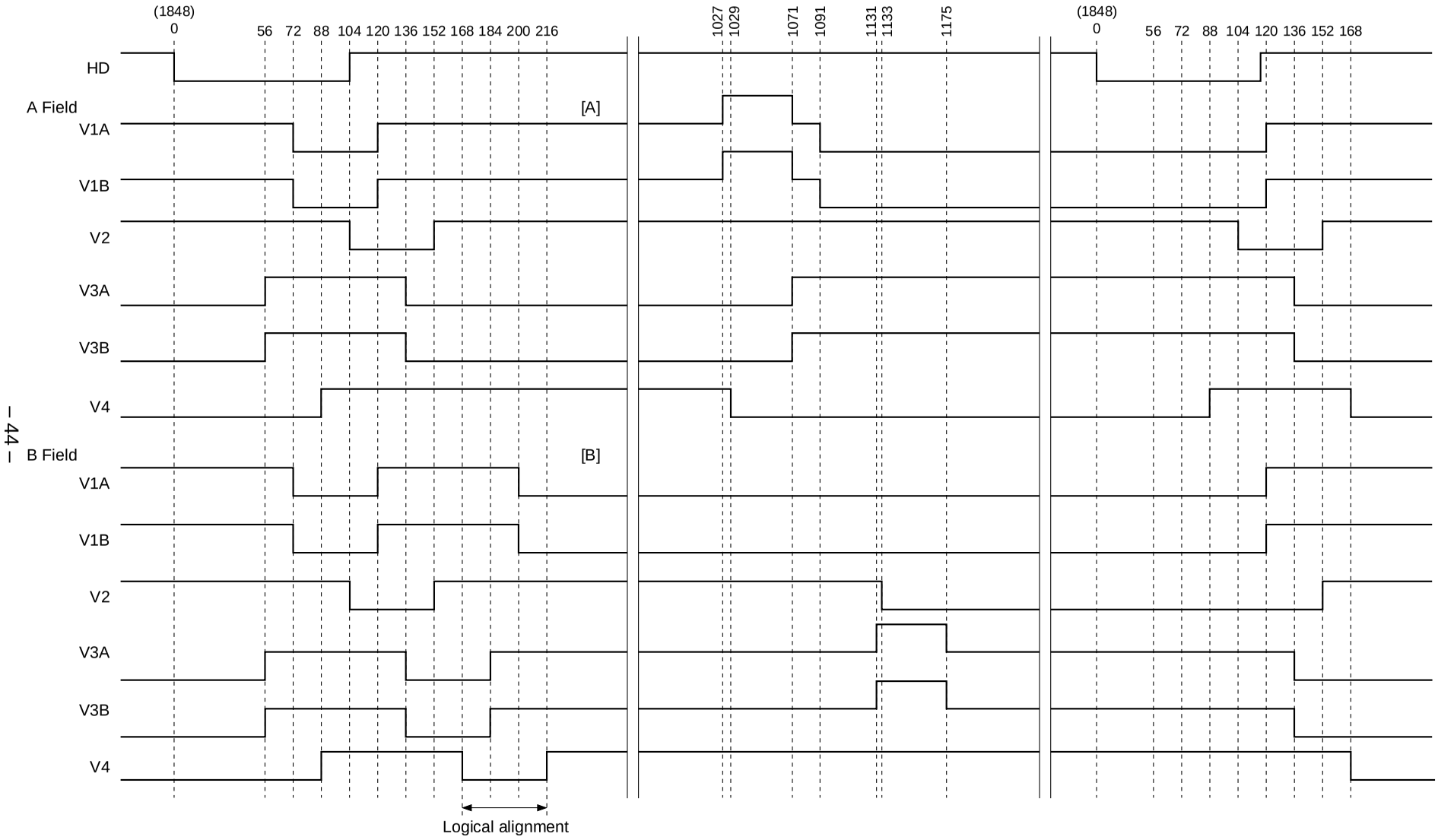
Chart-B6 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximately 3.0 to 13.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* This chart shows the pin configuration for the ICX434. (See page 3.)

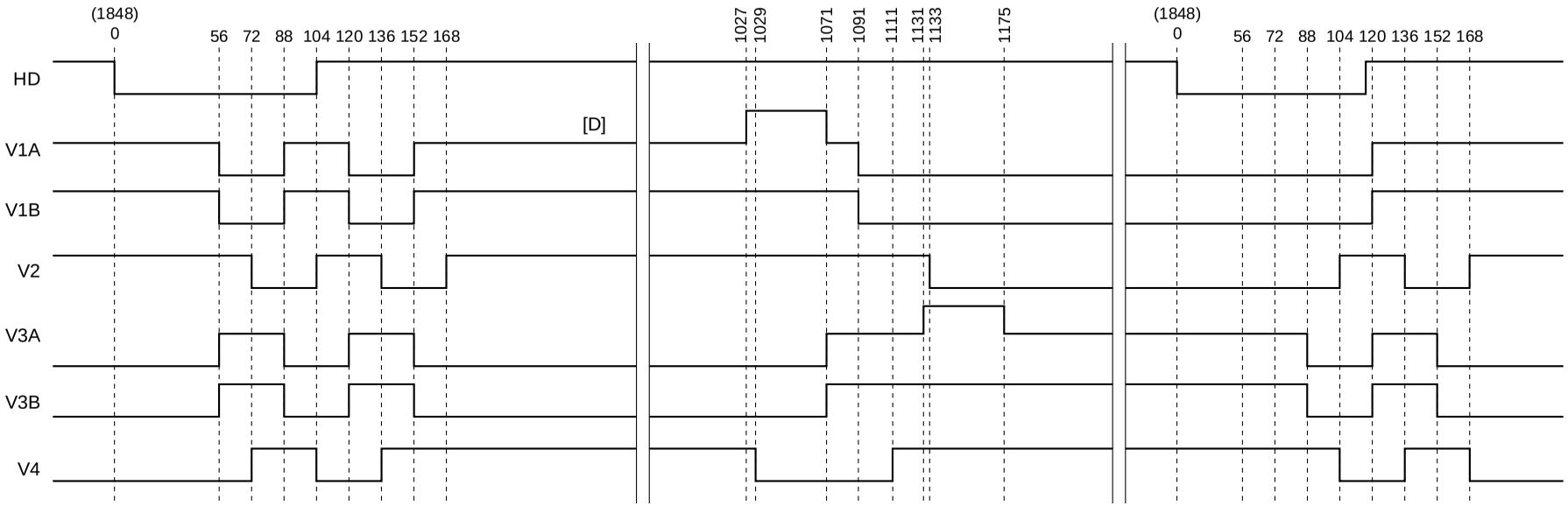
Chart-B7 Horizontal Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX434



* HD of this chart indicates the actual CXD3422GA load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HD.
* The HD fall period should be between approximates (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* This chart shows the pin configuration for the ICX434. (See page 3.)

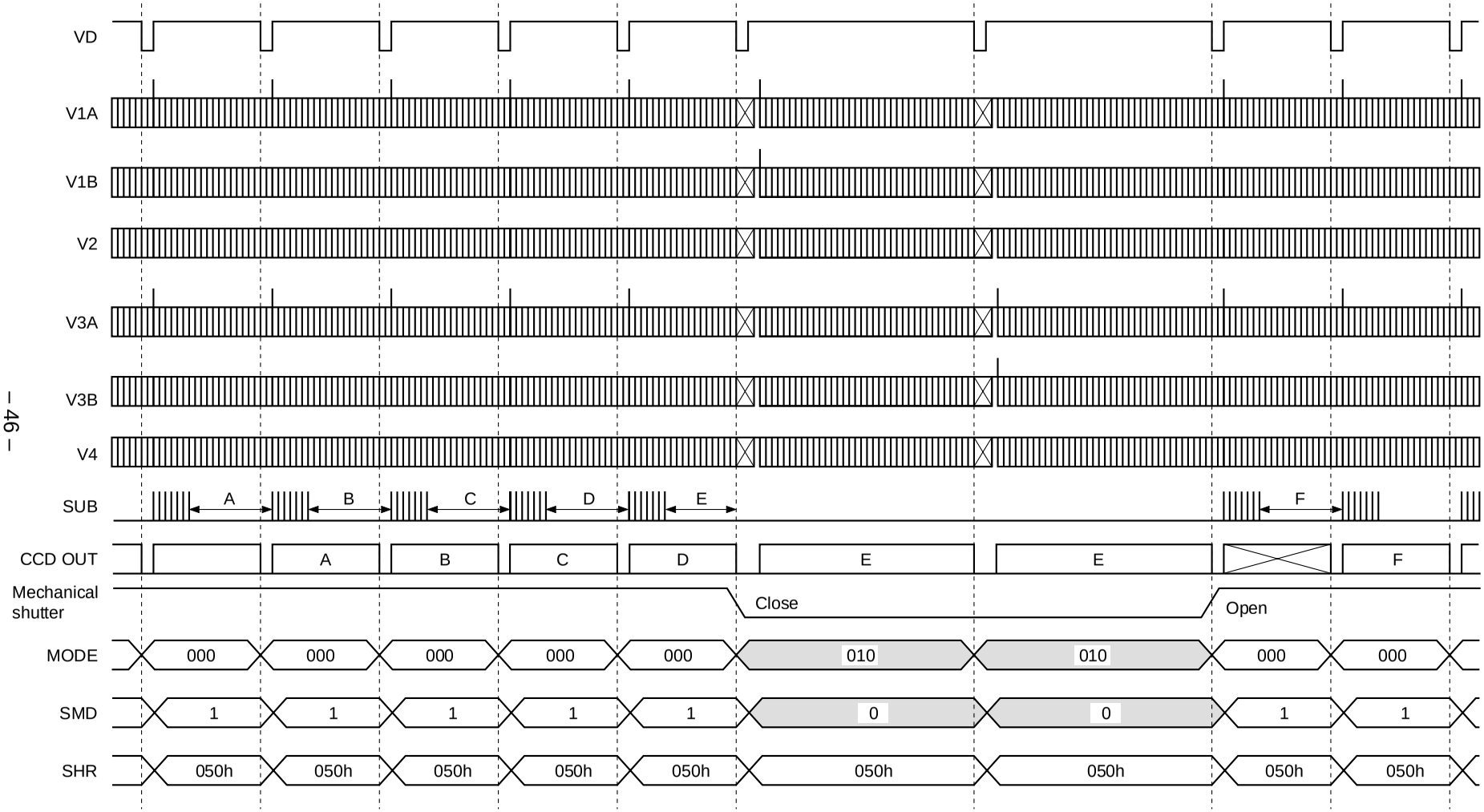
Chart-B8 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

Applicable CCD image sensor

• ICX434

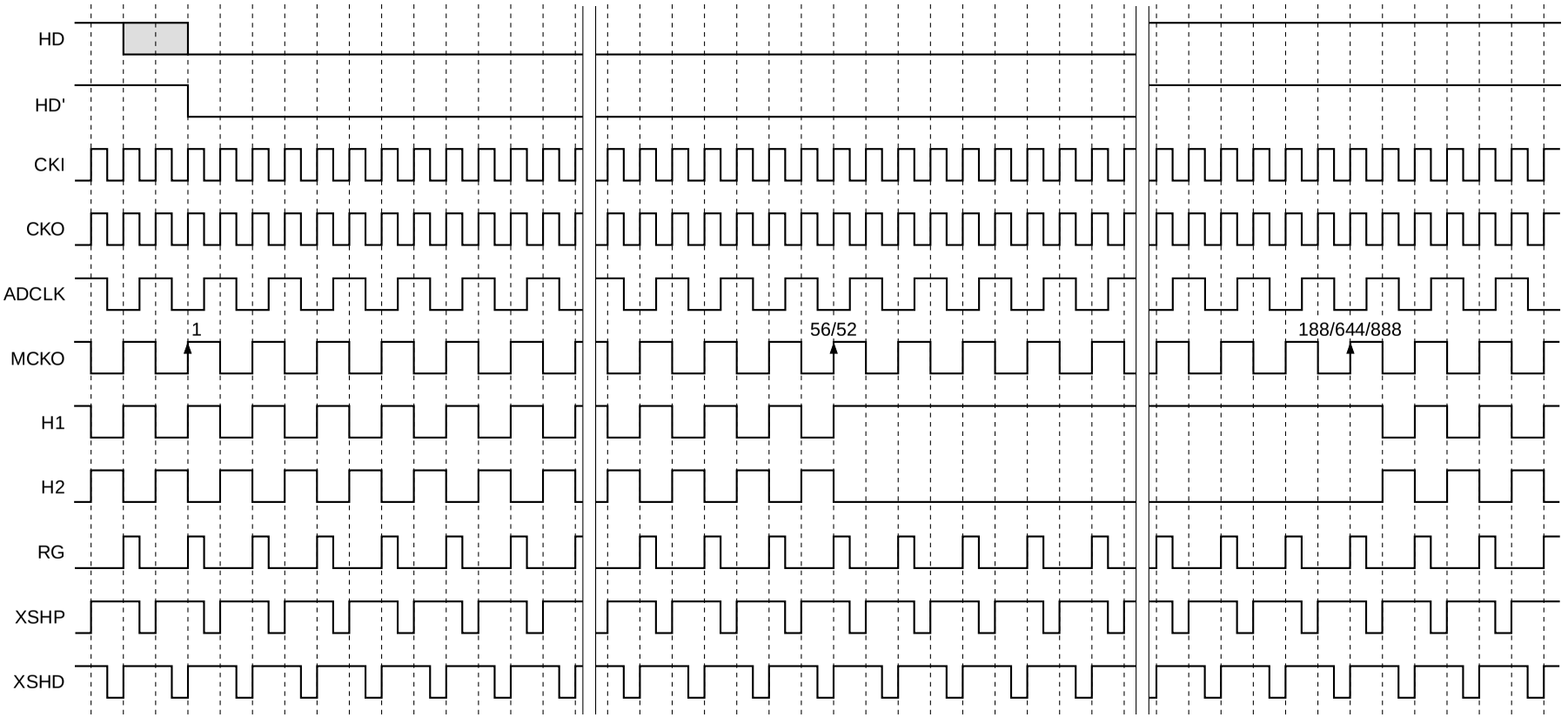


* This chart is a driving timing chart example of electronic shutter normal operation.
* Data exposed at D includes a blooming component. For details, see the CCD image sensor data sheet.
* The CXD3422GA does not generate the pulse to control mechanical shutter operation.
* The drive mode and the electronic shutter data are not switched at the same timing.
* This chart shows the pin configuration for the ICX434. (See page 3.)

Chart-Z High-Speed Phase Timing Chart

MODE

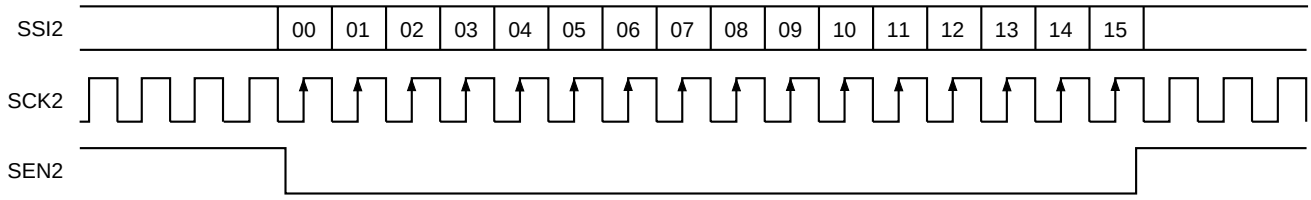
Applicable CCD image sensor
• ICX432/ICX434



* HD' indicates the HD which is the actual CXD3422GA load timing.
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phase of ADCLK can be specified by the serial interface data.

CCD Signal Processor Block Serial Interface Control

The CXD3422GA's CCD signal processor block basically loads the CCD signal processor block serial interface data sent in the following format at the rising edge of SEN2, and the setting values are then reflected to the operation 6 ADCLKI clocks after that.
CCD signal processor block serial interface control requires clock input to ADCLKI in order to load and reflect the serial interface data to operation, so this should normally be performed when the timing generator block is in the normal operation mode.



There are four categories of CCD signal processor block serial interface data: standby control data, PGA gain setting data, OB clamp level setting data, and input pulse polarity setting data.
Note that when data from multiple categories is loaded consecutively, the data for the category loaded last is valid and data from other categories is lost. When transferring data from multiple categories, raise SEN2 for each category and wait until the setting value has been reflected to operation 6 ADCKLI clocks after that, then transmit the next category.
The details of each data are described below.

Standby Control Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to "0".	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D14	FIXED	—	Set to "all 0".	
D15	STB	Standby control	Normal operation mode	Standby mode

PGA Gain Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to "0".	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04, D05	FIXED	—	Set to "all 0".	
D06 to D15	GAIN	PGA gain setting data	See D06 to D15 GAIN.	

OB Clamp Level Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to "0".	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D11	FIXED	—	Set to "all 0".	
D12 to D15	OBLVL	OB clamp level setting data	See D12 to D15 OBLVL.	

Input Pulse Polarity Setting Data

Data	Symbol	Function	Data = 0	Data = 1
D00	TEST	Test code	Set to "0".	
D01 to D03	CTG	Category switching	D01 to D03 CTG	
D04 to D12	FIXED	—	Set to "all 0".	
D13 to D15	POL	Input pulse polarity setting data	Set to "all 0".	

Detailed Description of Each Data

Shared data: D01 to D03 CTG [Category]

Of the data provided to the CXD3422GA by the CCD signal processor block serial interface, the CXD3422GA loads D04 and subsequent data to each data register as shown in the table below according to the combination of D01 to D03.

D01	D02	D03	Description of operation
0	0	0	Loading to standby control data register
0	0	1	Loading to PGA gain setting data register
0	1	0	Loading to OB clamp level setting data register
0	1	1	Loading to input pulse polarity setting data register
1	x	x	Access prohibited

Standby control data: D15 STB [Standby]

The operating mode of the CCD signal processor block is switched as follows. When the CCD signal processor block is in standby mode, only the serial interface is valid.

D15	Description of operation
0	Normal operating mode
1	Standby mode

PGA gain setting data: D06 to D15 GAIN [PGA gain]

The CXD3422GA can set the programmable gain amplifier (PGA) gain from –6dB to +42dB in 1024 steps by using PGA gain setting data D06 to D15 GAIN.

The PGA gain setting data is expressed as shown in the table below using D06 to D15 GAIN.

MSB									LSB
D06	D07	D08	D09	D10	D11	D12	D13	D14	D15
0	1	1	1	0	0	0	0	1	1
↓			↓					↓	
1			C					3	

→ GAIN is expressed as 1C3h.

For example, when GAIN is set to "000h", "080h", "220h", "348h" and "3FFh", the respective PGA gain setting values are –6dB, 0dB, +20dB, +34dB and +42dB.

OB clamp level setting data: D12 to D15 OBLVL [OB clamp level]

The CXD3422GA can set the OPB clamp output value from 0 to 60LSB in 4LSB steps by using CCD signal processor block control data D12 to D15 OBLVL.

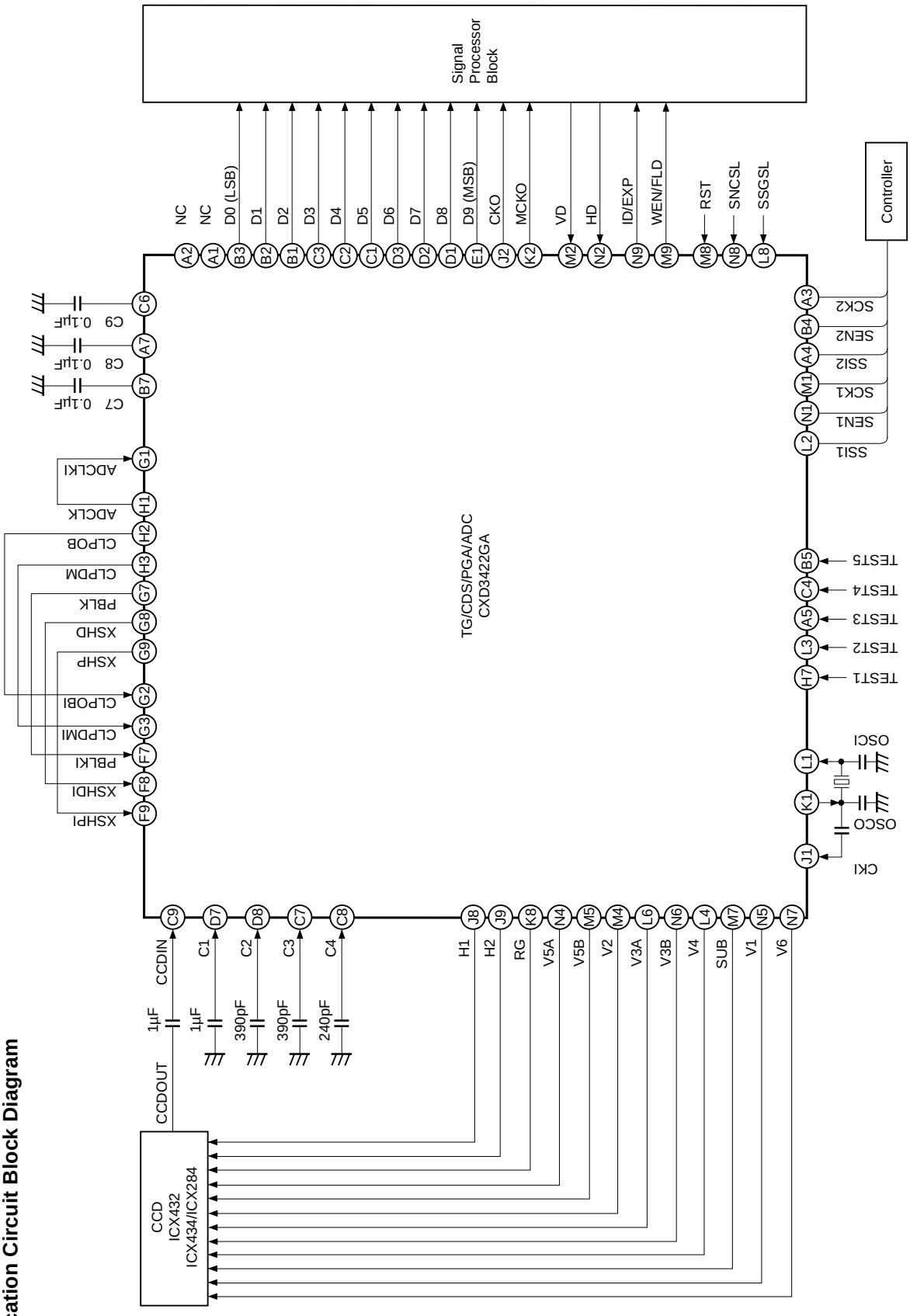
The OPB clamp output setting data is expressed as shown in the table below using D12 to D15 OBLVL.

MSB			LSB
D12	D13	D14	D15
0	1	1	0
		↓	
		6	

→ OBLVL is expressed as 6h .

For example, when OBLVL is set to "0h", "1h", "8h" and "Fh", the respective OPB clamp output setting values are 0LSB, 4LSB, 32LSB and 60LSB.

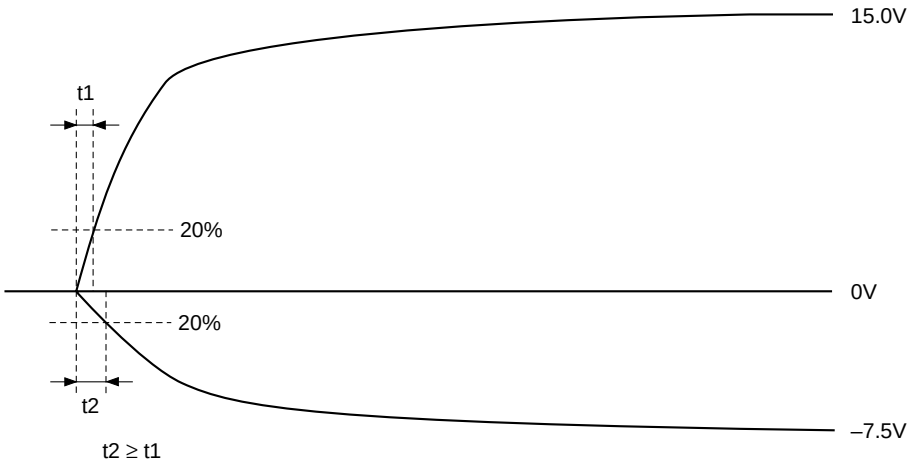
Application Circuit Block Diagram



This is the block diagram indicating the connection relations between this IC and each circuit block, and not the actual circuit diagram. Regarding the concrete connection circuit example with the CCD image sensor, see the data sheet of the CCD image sensor.
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Be sure to start up the timing generator block VL and VH pin power supplies at the timing shown in the figure below in order to prevent the SUB pin of the CCD image sensor from going to negative potential. In addition, start up the timing generator block V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} and V_{DD5} pins and CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4} and AV_{DD5} pin power supplies at the same time either before or at the same time as the VH pin power supply is started up.



2. Reset the timing generator block and CCD signal processor block during power-on. The timing generator block is reset by inputting the reset signal to the RST pin. The CCD signal processor block is reset by initializing the serial data.

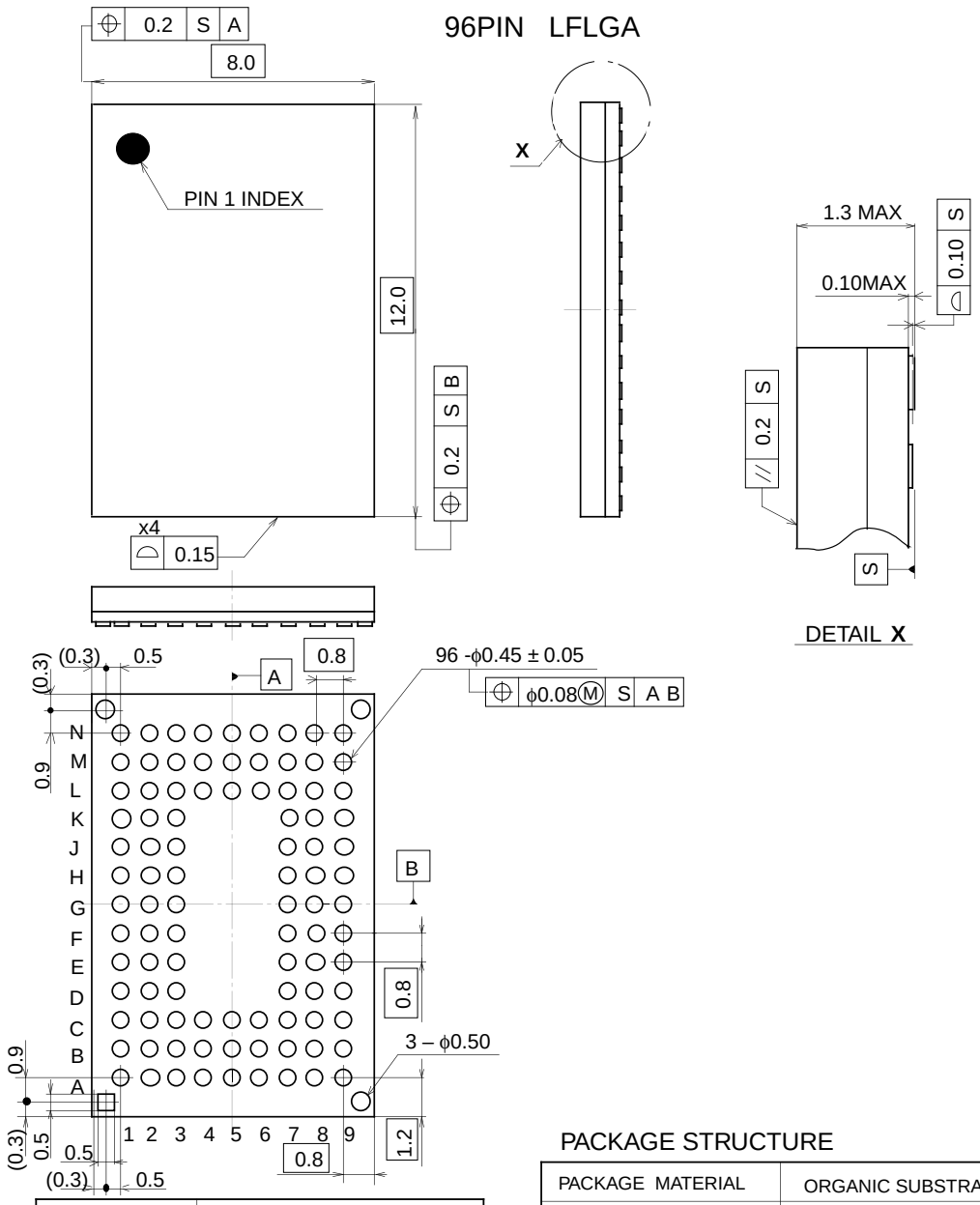
3. Separate the timing generator block V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4} and V_{DD5} pins from the CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, and AV_{DD5} pins.
   Also, the ADC output driver stage is connected to the dedicated power supply pin DV_{DD1}. Separating this pin from other power supplies is recommended to avoid affecting the internal analog circuits.

4. The difference in potential between the timing generator block V_{DD4}, pin supply voltage 3 V_{DD}c and the CCD signal processor block DV_{DD1}, DV_{DD2}, AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4} and AV_{DD5} pin supply voltages 1 V_{DD}e, 2 V_{DD}f and 3 V_{DD}g should be 0.1V or less.

5. The timing generator block and CCD signal processor block ground pins should use a shared ground which is connected outside the IC. When the set ground is divided into digital and analog blocks, connect the timing generator block ground pins to the digital ground and the CCD signal processor block ground pins to the analog ground. The difference in potential between the timing generator block V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}, V_{SS5} and VM and the CCD signal processor block DV_{SS1}, DV_{SS2}, DV_{SS3}, AV_{SS1}, AV_{SS2}, AV_{SS3}, AV_{SS4}, AV_{SS5} and AV_{SS6} should be 0.1V or less.

6. Do not perform serial communication with the CCD signal processor block during the effective image period, as this may cause the picture quality to deteriorate. In addition, using SCK2, SSI2 and SEN2, which are used by the CCD signal processor block, use of the dedicated ports is recommended. When using these pins as shared ports with the timing generator block or other ICs, be sure to thoroughly confirm the effects on picture quality before use.

Package Outline Unit: mm



SONY CODE	LFLGA-96P-02
EIAJ CODE	P-LFLGA96-12X8-0.8
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	NICKEL & GOLD PLATING
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.3g

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