SONY

CXK77B3610GB -6/7

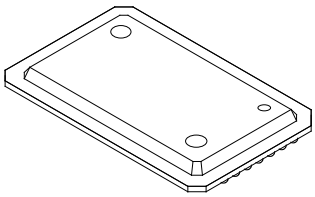
High Speed Bi-CMOS Synchronous Static RAM

Preliminary

Description

The CXK77B3610GB-6/7 is a high speed 1M bit Bi-CMOS synchronous statis RAM organized as 32768 words by 36 bits. This SRAM integrates input registers, high speed SRAM and write buffer onto a single monolithic IC and features the delayed write system to reduce the dead cycles.

119 pin BGA (Plastic)



Features

- Fast cycle time (Cycle) (Frequency)
  CXK77B3610GB-6 6ns 166MHz
  CXK77B3610GB-7 7ns 142MHz
- Inputs and outputs are LVTTL/LVCMOS compatible
- Single 3.3V power supply: 3.3V ± 0.15V
- Byte-write possible
- $\overline{OE}$ asynchronization
- JTAG test circuit
- Package 119TBGA
- 3 kinds of synchronous operation mode
  Register-Register mode (R-R mode)
  Register-Flow Thru mode (R-F mode)
  Register-Latch mode (R-L mode)

Function

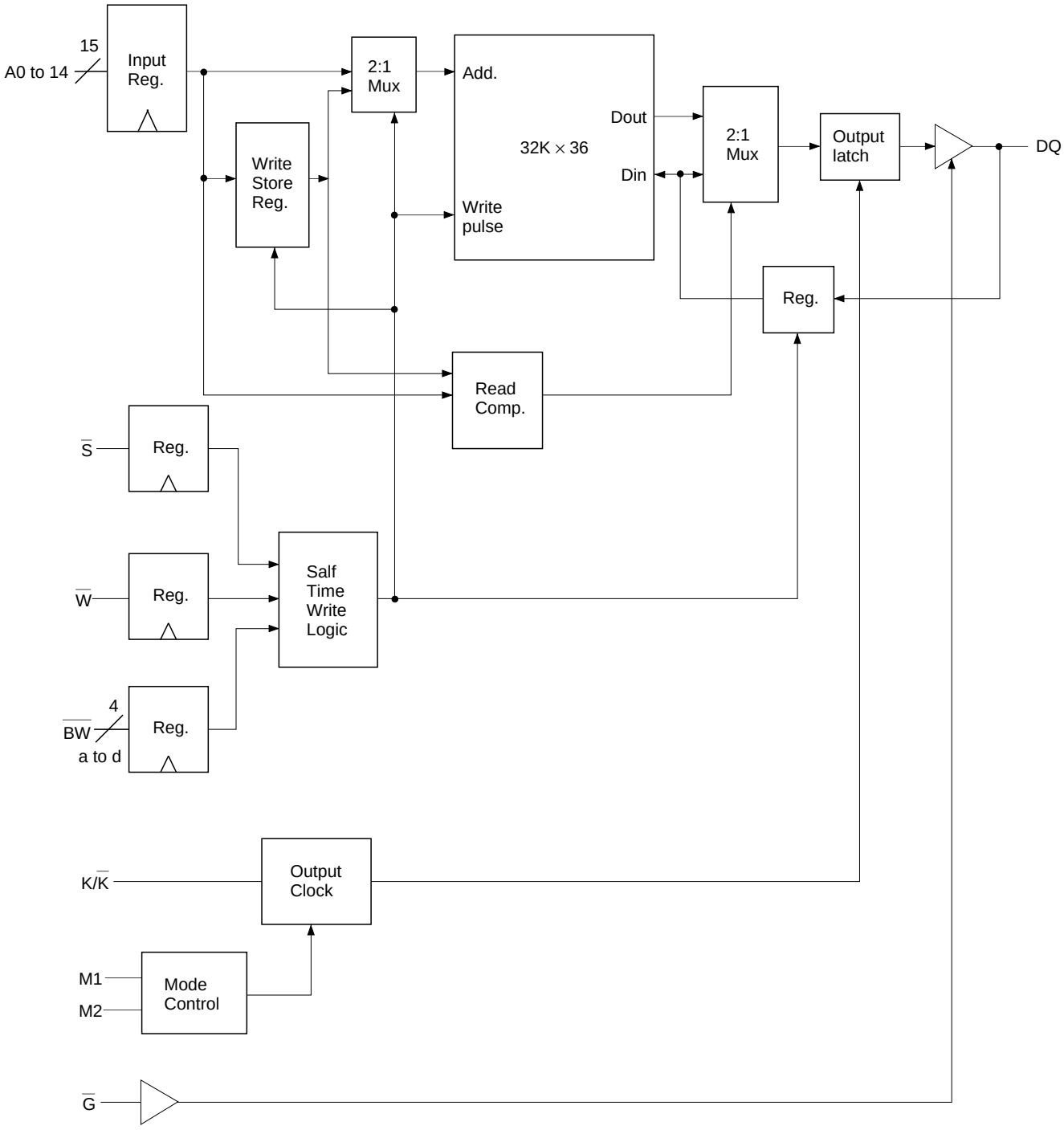
32768 word × 36bit High Speed Bi-CMOS Synchronous SRAM

Structure

Silicon gate Bi-CMOS IC

PE95128-PS

Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7
A	$V_{DD}Q$	A	A	NC	A	A	$V_{DD}Q$
B	NC	NC	NC	NC	NC	NC	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{S}$	V_{SS}	DQb	DQb
F	$V_{DD}Q$	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	$V_{DD}Q$
G	DQc	DQc	$\overline{BW}$c	NC	$\overline{BW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	$V_{DD}Q$	V_{DD}	NC	V_{DD}	NC	V_{DD}	$V_{DD}Q$
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BW}$d	$\overline{K}$	$\overline{BW}$a	DQa	DQa
M	$V_{DD}Q$	DQd	V_{SS}	$\overline{W}$	V_{SS}	DQa	$V_{DD}Q$
N	DQd	DQd	V_{SS}	A	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	A	V_{SS}	DQa	DQa
R	NC	A	M1	V_{DD}	M2	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	$V_{DD}Q$	TME	TDI	TCK	TDO	NC	$V_{DD}Q$

Pin Description

Symbol	Description	Symbol	Description	Symbol	Description
A	Address Input	$\overline{G}$	Asyn Output Enable	$V_{DD}Q$	Output power supply
DQx	Data I/O in byte a to d	ZZ	Sleep Mode Select	V_{SS}	Ground
K	Positive Clock	TCK	JTAG Clock	M1, M2	Mode Select
$\overline{K}$	Negative Clock	TMS	JTAG Mode Select	NC	No Connect
$\overline{W}$	Write Enable	TDI	JTAG Data In		
$\overline{BW}$x	Byte Write Enable (a to d)	TDO	JTAG Data Out		
$\overline{S}$	Chip Select	V_{DD}	+3.3V power supply		

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +4.6	V
Input voltage	V_{IN}	–0.5 to V_{CC} +0.5 (4.6V max.)	V
Output voltage	V_O	–0.5 to V_{CC} +0.5 (4.6V max.)	V
Allowable power dissipation	P_D	TBD	W
operating temperature	Topr	0 to 70	°C
Strorage temperature	Tstg	–55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · sec

Truth Table

ZZ	$\overline{S}$ (tn)	$\overline{W}$ (tn)	$\overline{BW}$x (tn)	$\overline{G}$	Mode	DQ0 to 35 (tn)	DQ0 to 35 (tn+1)	V_{DD} Current
H	X	X	X	X	Sleep mode, Power down	Hi-Z	Hi-Z	I_{SB}
L	H	X	X	X	Deselect	X	Hi-Z	I_{CC}
L	L	H	X	H	Read	Hi-Z	Hi-Z	I_{CC}
L	L	H	X	L	Read	X	Q (tn)	I_{CC}
L	L	L	L	X	Write all bytes (bits 0 to 35)	X	D (tn)	I_{CC}
L	L	L	X	X	Write bytes with $\overline{BW}$x = L	X	D (tn)	I_{CC}
L	L	L	H	X	Aborted Write	X	X	I_{CC}

DC Recommended Operating Conditions (Ta = 25°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.15	3.3	3.45	V
Output supply voltage	$V_{DD}Q$	3.15	3.3	3.45	V
Input high voltage	V_{IH}	2.0	—	V_{DD} +0.3	V
Input low voltage	V_{IL}	–0.3	—	0.8	V
Differential clock input signal	ΔV_K	0.4	0.8	—	V
Differential clock input common mode	V_K, COM	1.2	2.0	2.2	V

Mode Select Truth Table

Item	M1	M2
Register-Resister mode	L	H
Register-Flow Thru mode	L	L
Register-Latch mode	H	L

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 3.3V ± 10%, GND = 0V, Ta = 0 to 70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	–1	—	1	µA
Output leakage current	I_{LO}	V_O = GND to V_{CC} $\overline{G}$ = V_{IH}	–10	—	10	µA
Operating power supply current	I_{CC}	Cycle = min. Duty = 100% I_{OUT} = 0mA	—	—	TBD	mA
Standby current	I_{SB}	ZZ ≥ V_{IH}			20	mA
Output high voltage	V_{OH}	I_{OH} = –2.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.0mA	—	—	0.4	V

* V_{CC} = 3.3V, Ta = 25°C

• I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
Clock input capacitance	C_{CLK}	V_{IN} = 0V	—	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	—	8	pF

Note) These parameters are sampled and are not 100% tested.

• AC Electrical Characteristics

Item	Symbol	-6		-7		Unit
		Min.	Max.	Min.	Max.	
Address access (except Register-Register mode)	t_{AA}	—	9	—	10	ns
Clock period	t_{KP}	6	—	7	—	ns
Clock pulse high	t_{KH}	2	—	3	—	ns
Clock pulse low	t_{KL}	2	—	3	—	ns
Setup time	t_S	0.5	—	1	—	ns
Hold time	t_H	1	—	1	—	ns
Clock high to output (R-R mode)	t_{KQ}	1.5*2	3	1.5*2	3.5	ns
Clock high to output (R-F mode, R-L mode)	t_{KQ1}	—	6	—	7	ns
Clock low to output (R-L mode)	t_{KQ2}	1.5*2	3	1.5*2	3.5	ns
Write cycle clock high to following Read cycle output (R-F mode, R-L mode)	t_{KQ3}		15		17	ns
Clock high to output high impedance ($\overline{S}$ deselect cycle)	t_{HZ}*2	1.5	3	1.5	3.5	ns
Write cycle clock high to output high impedance (R-F mode, R-L mode)	t_{WHZ}*2	1.5	3	1.5	3.5	ns
Clock high to output low impedance (R-R mode)	t_{LZ}*2	1.5	—	1.5	—	ns
Clock high to output low impedance (R-F mode)	t_{LZ1}*2	2	—	2	—	ns
Clock low to output low impedance (R-L mode)	t_{LZ2}*2	1.5	—	1.5	—	ns
Output enable to output valid ($\overline{G}$)	t_{OE}	—	3	—	3.5	ns
Output enable to output in low Z ($\overline{G}$)	t_{OLZ}*2	1	—	1	—	ns
Output disable to output in high Z ($\overline{G}$)	t_{OHZ}*2	—	3	—	3.5	ns

*1 All parameters are specified over the range 0 to 70°C.

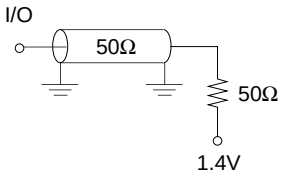
*2 These parameters are sampled and are not 100% tested.

AC characteristics

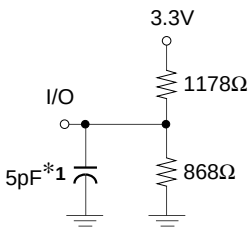
• AC test conditions (V_{DD} = 3.3V ± 0.15V, Ta = 0 to 70°C)

Item	Conditions
Input pulse high level	V_{IH} = 2.4V
Input pulse low level	V_{IL} = 0.4V
Input rise & fall time	1V/ns
Input reference level	2.0/0.8V
Clock input reference level	K/$\overline{K}$ cross; C/$\overline{C}$ cross
Clock input differential signal	0.8V
Clock input rise & fall time	1V/ns
Output reference level	1.4V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2) *2



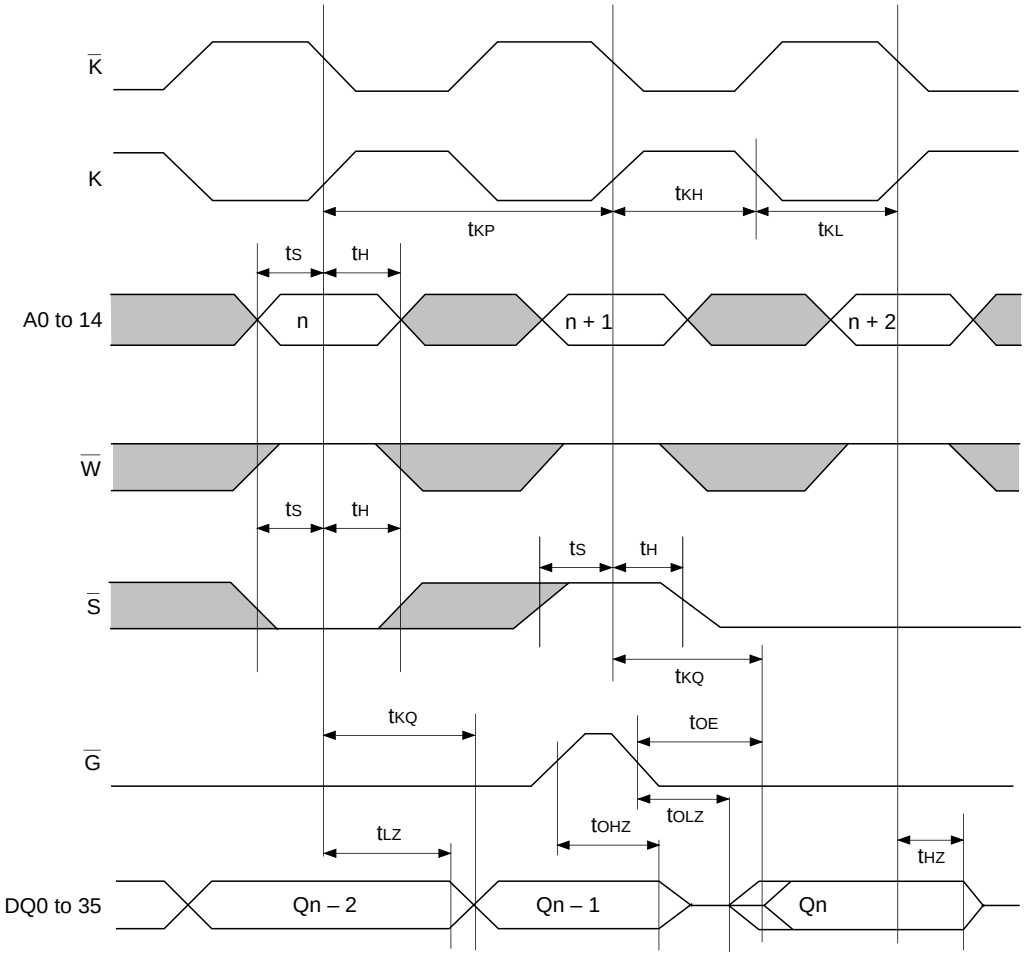
*1 Including scope and jig capacitance.

*2 For t_{LZ}, t_{HZ}.

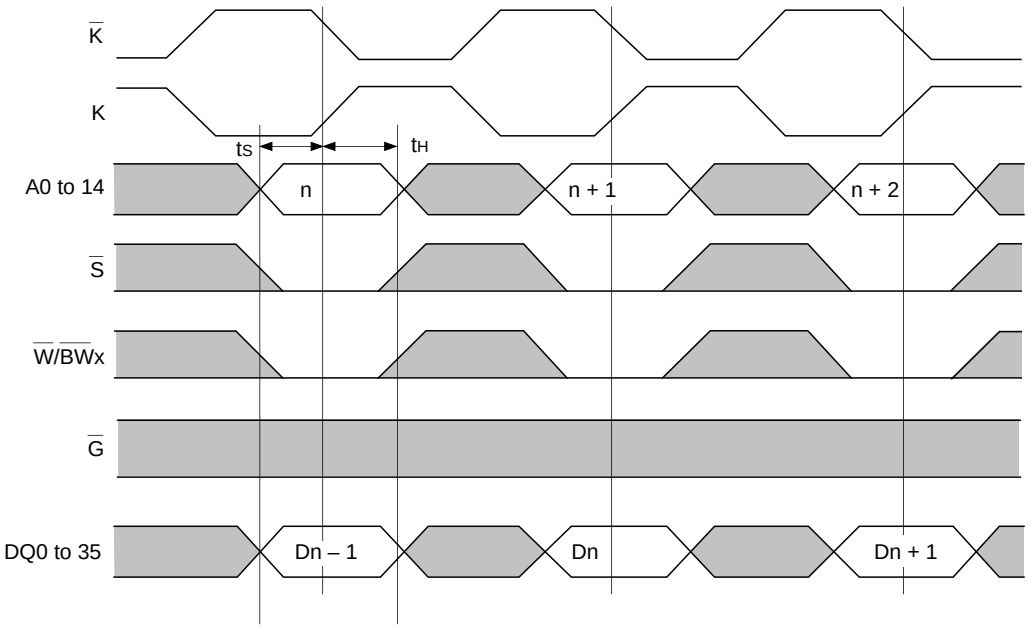
Fig. 1.

Register-Register mode

Timing waveform of READ CYCLE

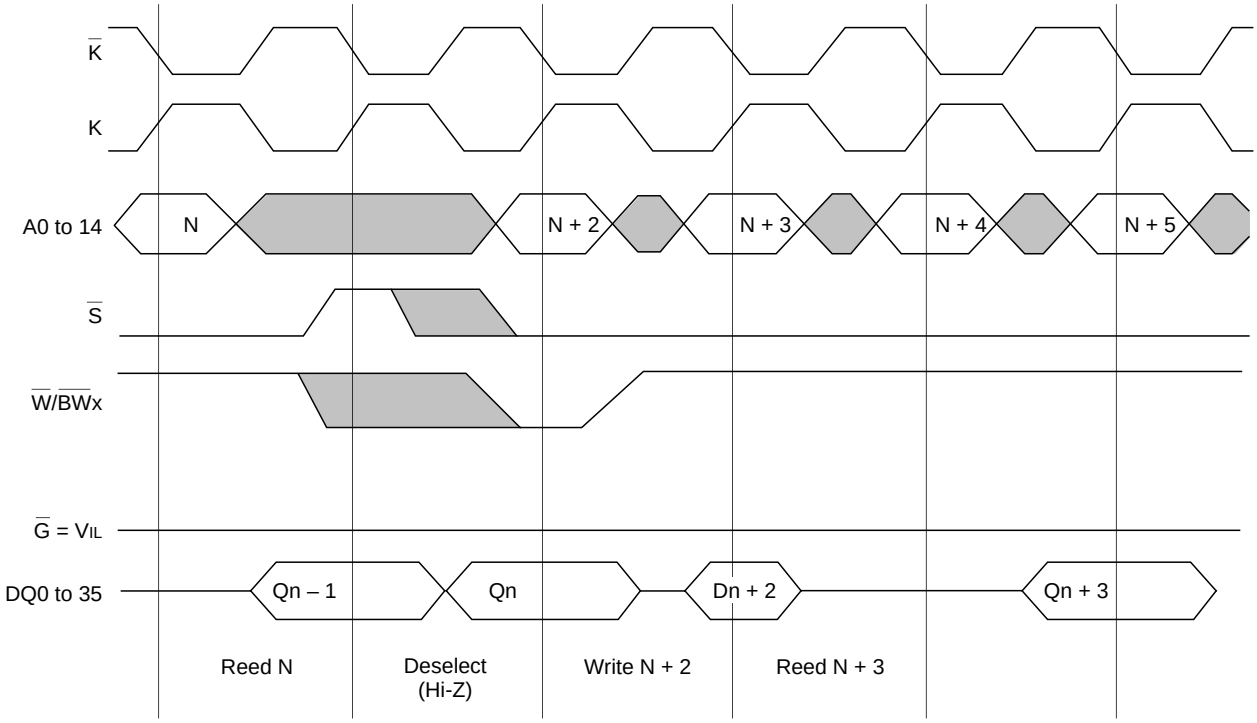


Timing waveform of WRITE CYCLE

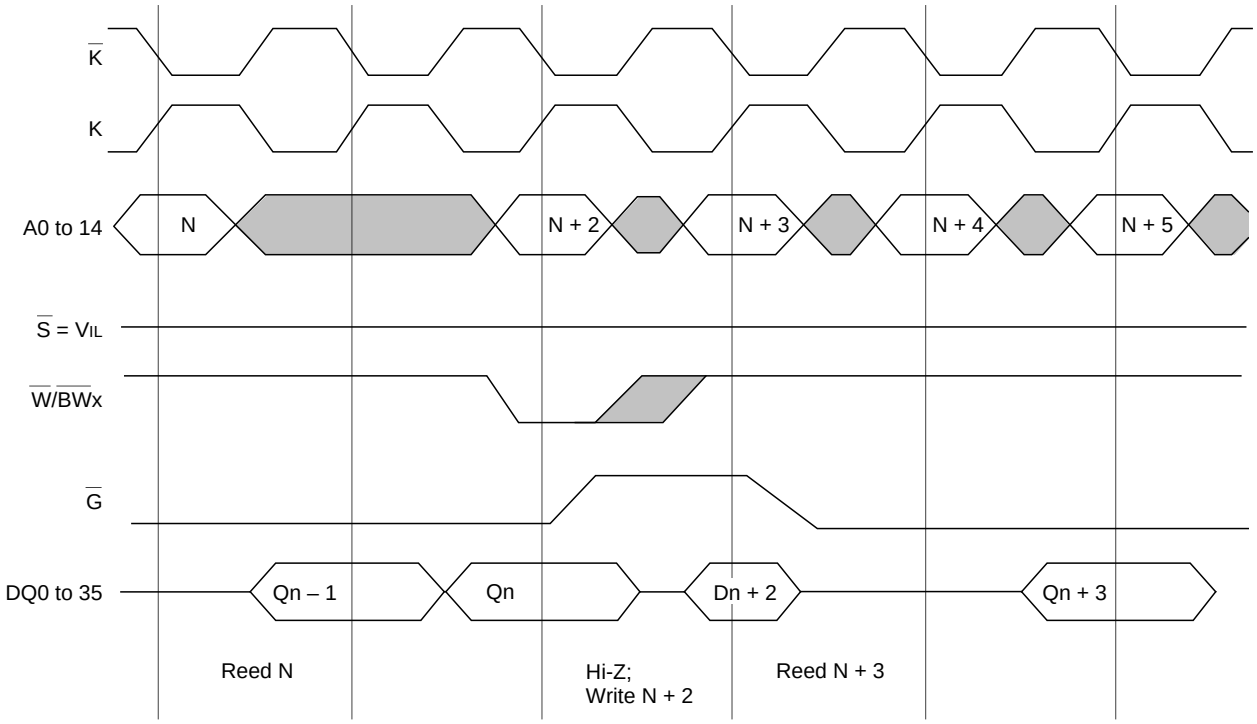


Register-Register mode

Timing waveform of READ-WRITE-READ CYCLE I ($\overline{S}$ controlled)

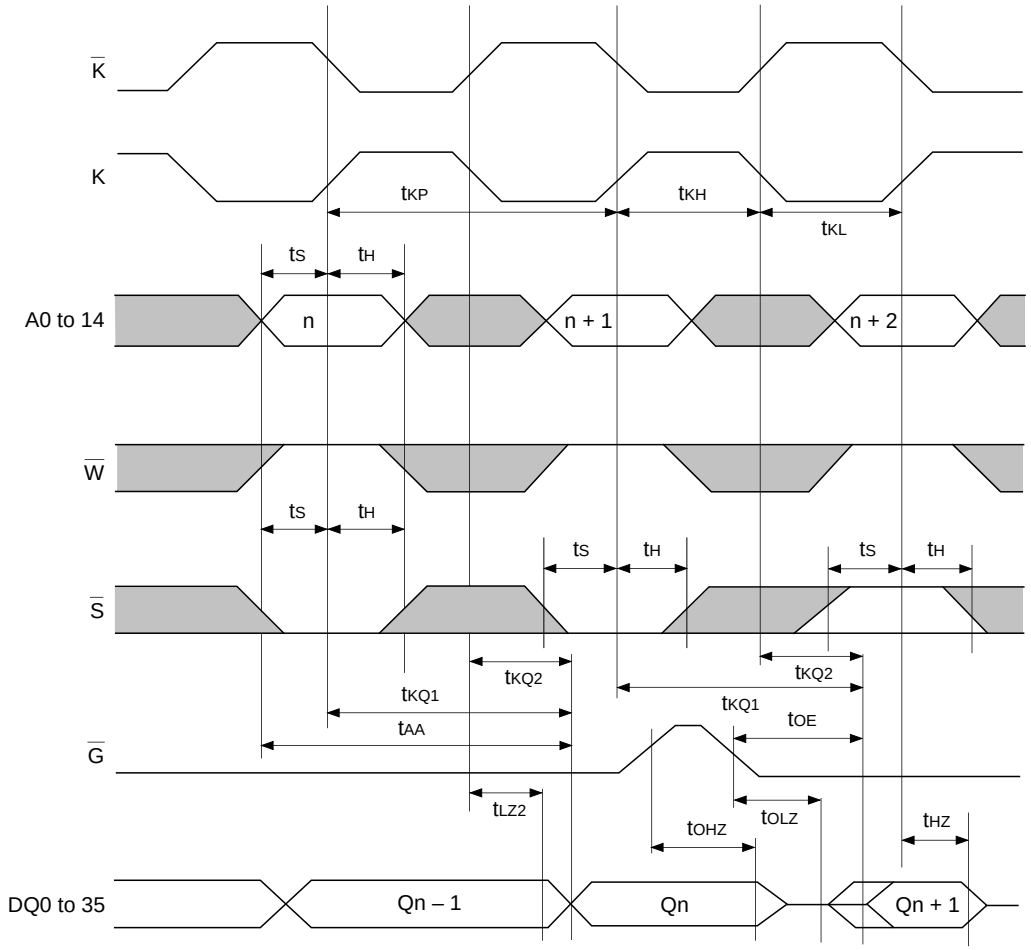


Timing waveform of READ-WRITE-READ CYCLE II ($\overline{G}$ controlled)

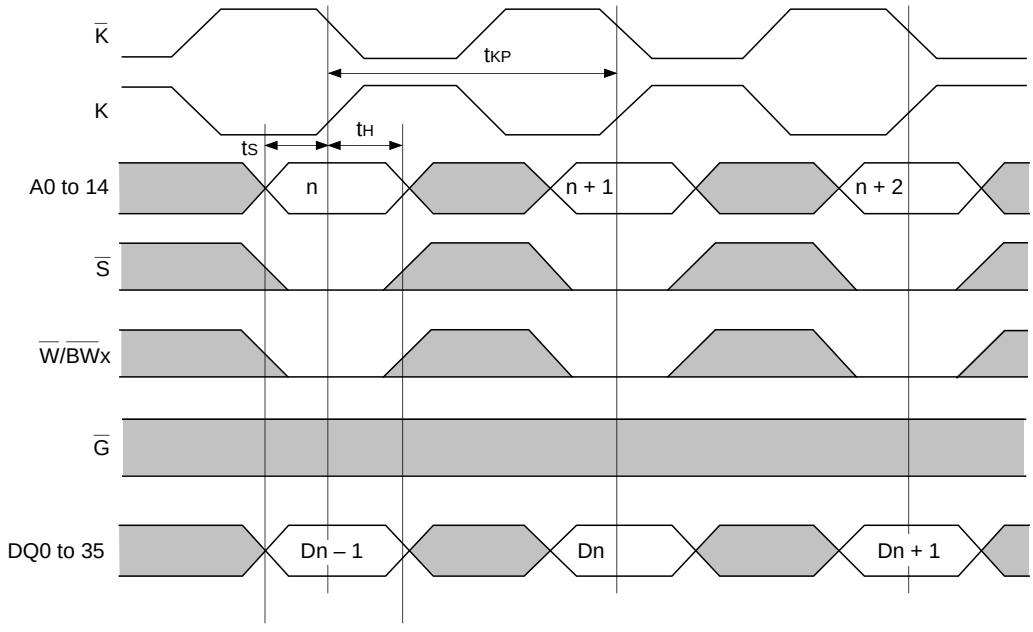


Register-Latch mode

Timing waveform of READ CYCLE

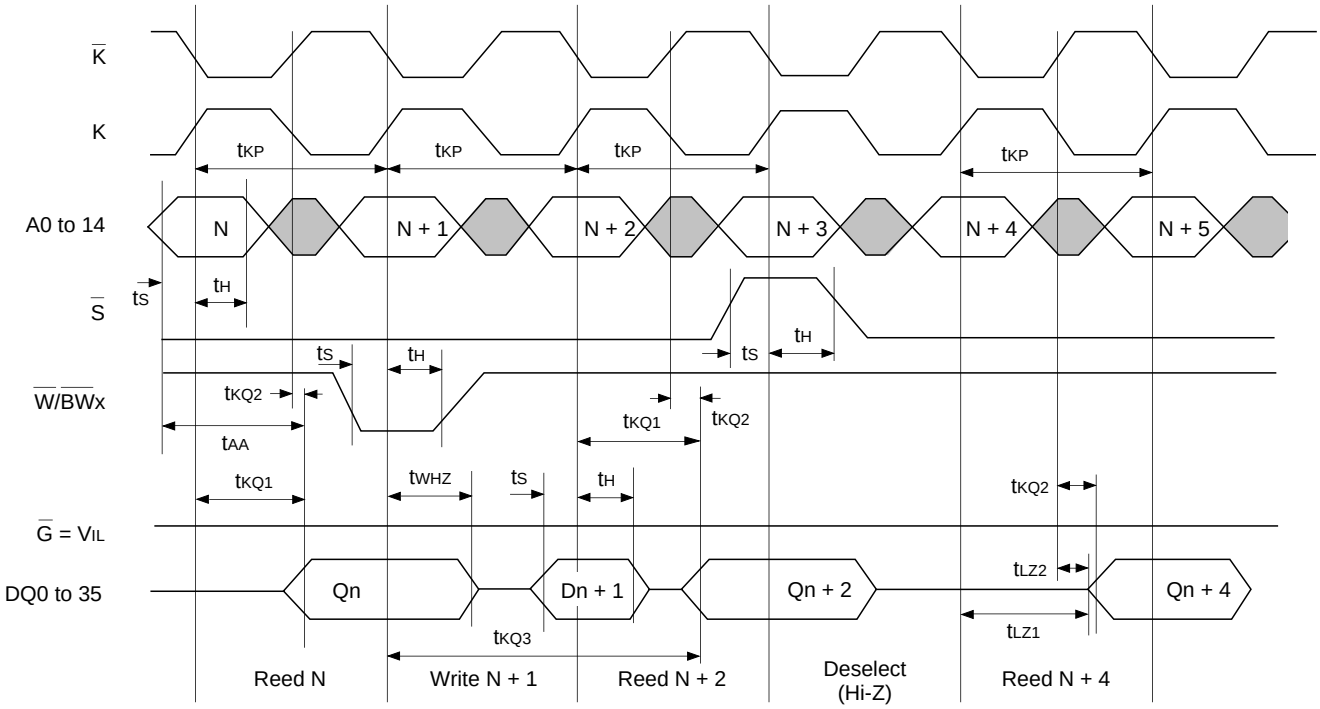


Timing waveform of WRITE CYCLE



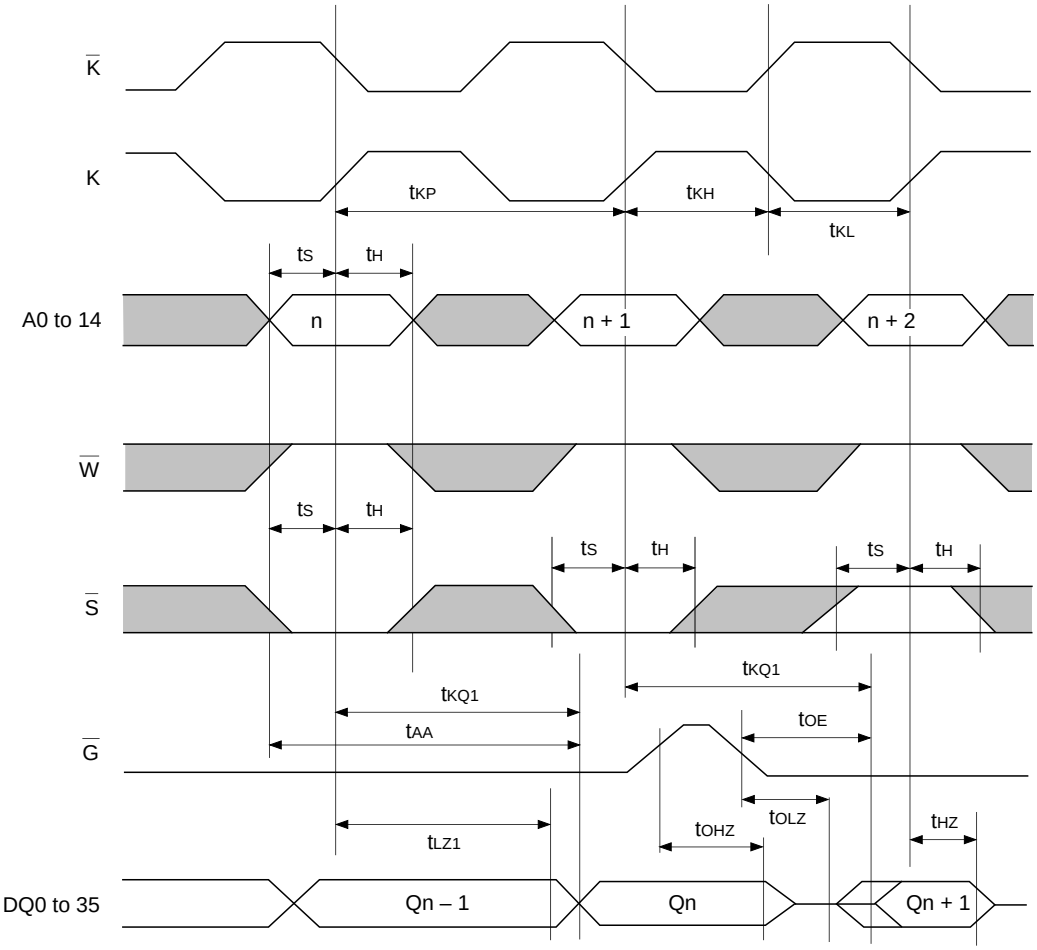
Register-Latch mode

Timing waveform of READ-WRITE-READ CYCLE

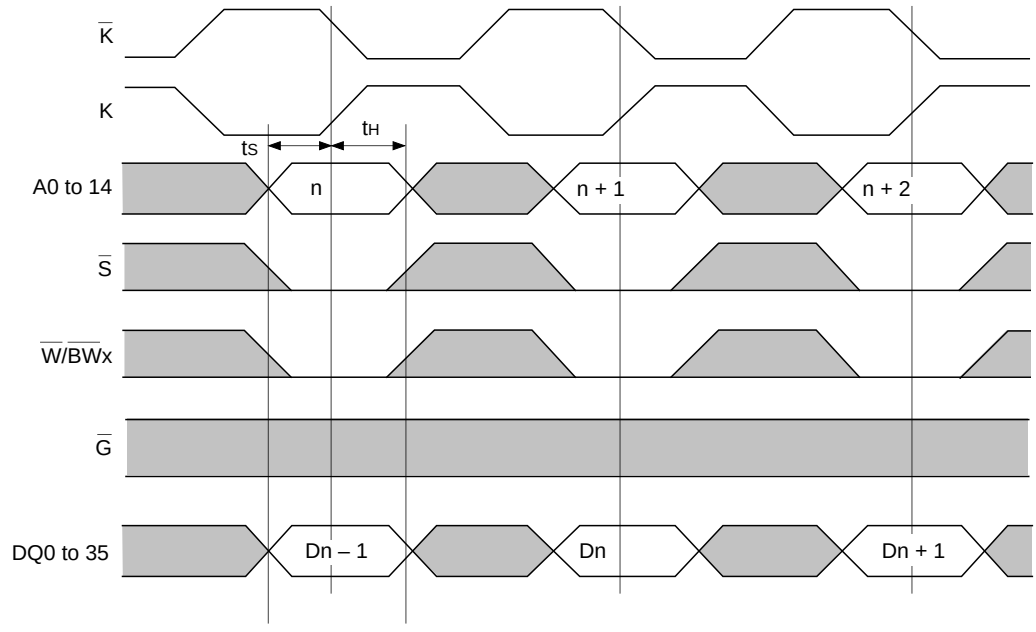


Register-Flow Thru mode

Timing waveform of READ CYCLE

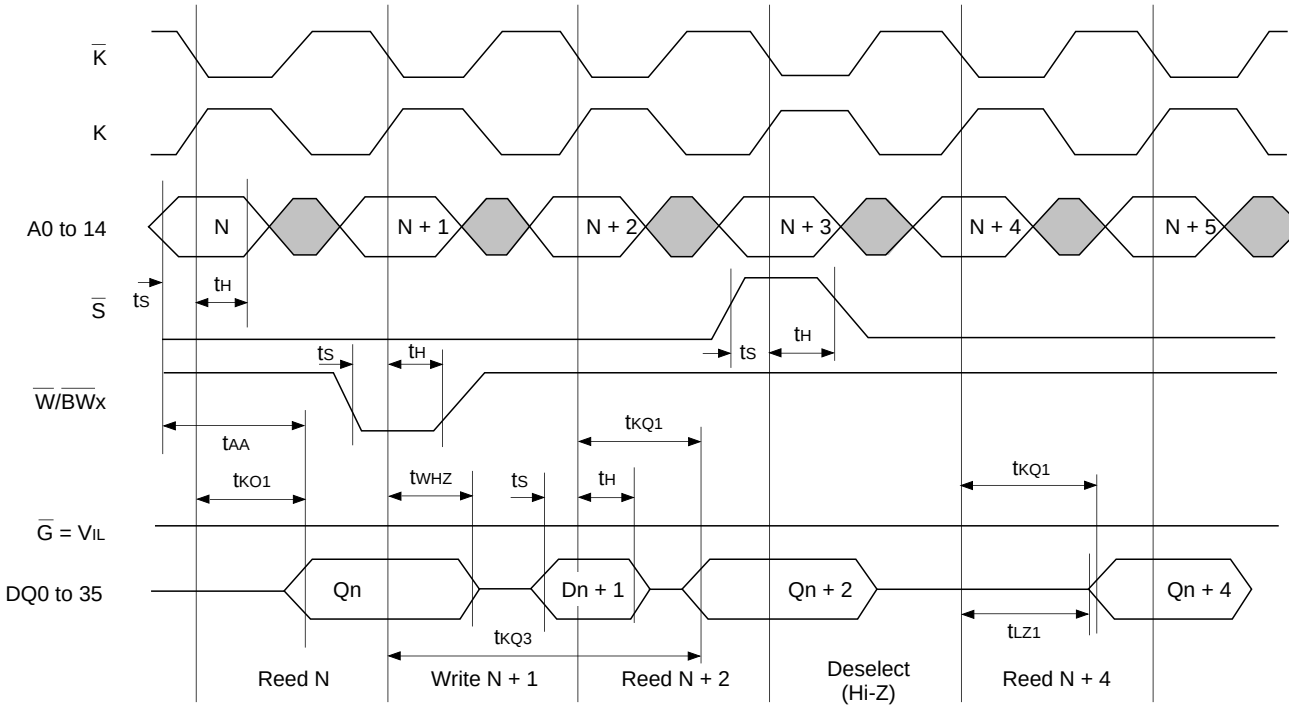


Timing waveform of WRITE CYCLE



Register-Flow Thru mode

Timing waveform of READ-WRITE-READ CYCLE



Test Mode Description

Fuctional Description

The CXK77B3610 provides JTAG boundary scan interface using IEEE std. 1149.1 protocol. The test mode is intended to provided a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs other components and print circuit board.

In conformance with IEEE std. 1149.1, the CXK77B3610 contains a TAP controller, Instruction register, Boundary scan register and Bypass register.

Test Access Port (TAP)

4 pins as defined in Pin Description table are used to perform JTAG functions. TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary scan register and Bypass register). TDO is output pin used to scan test data serially out. The TDI send the data into LSB of selected register and the MSB of the selected register feeds the data to TDO. TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI, TMS are registered on the rising edge of TCK clock and the output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP conroller is in Shift-IR state or in Shift-DR state.

TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enter reset state in one of three ways:

1. Power up
2. Apply logic 1 on TMS input pin on 5 consecutive TCK rising edges.

Instruction Resister (3 bits)

The JTAG Instruction resister is consisted of shift resister stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

Octal	MSB		LSB	Instruction
0	0	0	0	Bypass
1	0	0	1	IDCODE. read device ID
2	0	1	0	Sample-Z. Sample Inputs and tri-state DQs
3	0	1	1	Bypass
4	1	0	0	Sample. Sample Inputs.
5	1	0	1	Private. Manufacturer use only.
6	1	1	0	Bypass
7	1	1	1	Bypass

Bypass Register (1 bit)

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

ID Registers (32 bits)

The ID Register are 32 bits wide and are listed as follow:

	ID [0]	1
Sony ID	ID [11:1]	0000 1110 001
Part Number	ID [27:12]	0000 0000 0000 0000
Revision Number	ID [31:28]	xxxx*1

*1 Please contact Sony Sales Department.

Boundary Scan Register (70 bits)

The Boundary Scan Registers are 70 bits wide and are listed as follow:

DQ	36
A	15
$\overline{W}$, $\overline{BW}$x	5
$\overline{S}$, $\overline{G}$	2
K, $\overline{K}$, C, $\overline{C}$	4
ZZ	1
Mode	2
Place Holder	5

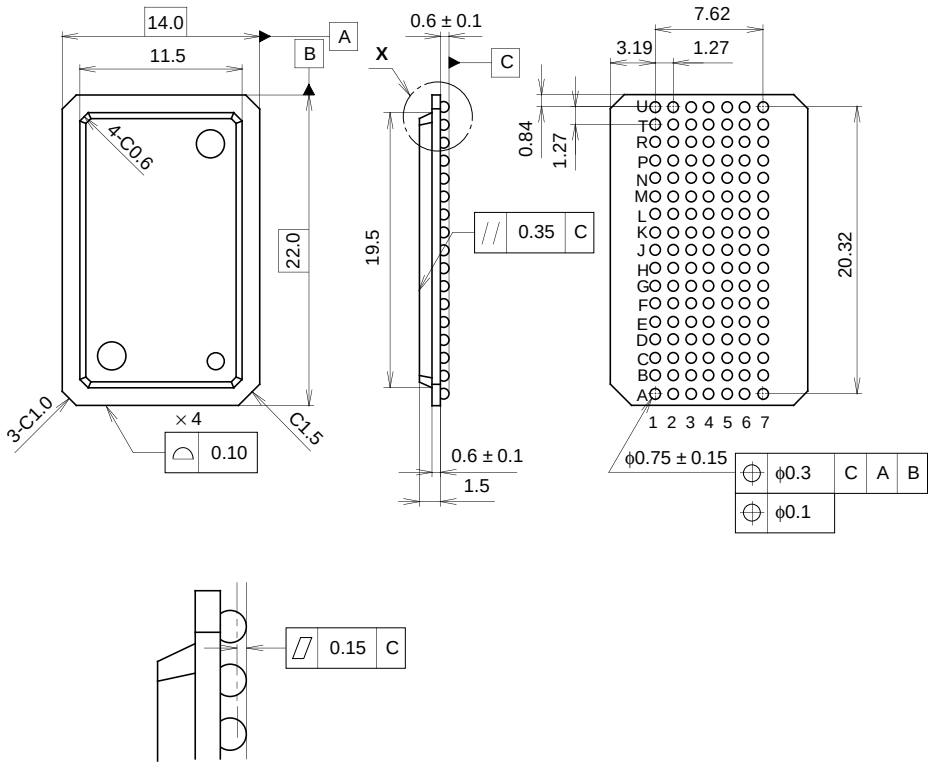
K/$\overline{K}$, C/$\overline{C}$ inputs are sampled through one differential stage and internal inverted to generate internal K/$\overline{K}$, C/$\overline{C}$ signals for scan registers. Place Holder are required for some NC pins to maintain 70 bits Scan Register for different types of same family SRAM and for density upgrade. All Place Holder Registers are connected to V_{SS} internally regardless of pin connection externally.

Scan Order (Order by exit sequence)

36	—	V_{SS}		V_{SS}	—	35
37	—	V_{SS}		V_{SS}	—	34
38	3A	A		A	5A	33
39	3C	A		A	5C	32
40	2C	A		A	6C	31
41	2A	A		A	6A	30
42	2D	DQc		DQb	6D	29
43	1D	DQc		DQb	7D	28
44	2E	DQc		DQb	6E	27
45	1E	DQc		DQb	7E	26
46	2F	DQc		DQb	6F	25
47	2G	DQc		DQb	6G	24
48	1G	DQc		DQb	7G	23
49	2H	DQc		DQb	6H	22
50	1H	DQc		DQb	7H	21
51	3G	/Wc		/Wb	5G	20
52	—	V_{SS}		/G	4F	19
53	4E	/S		K	4K	18
54	4G	/C		/K	4L	17
55	4H	C		/Wa	5L	16
56	4M	/W		DQa	7K	15
57	3L	/Wd		DQa	6K	14
58	1K	DQd		DQa	7L	13
59	2K	DQd		DQa	6L	12
60	1L	DQd		DQa	6M	11
61	2L	DQd		DQa	7N	10
62	2M	DQd		DQa	6N	9
63	1N	DQd		DQa	7P	8
64	2N	DQd		DQa	6P	7
65	1P	DQd		ZZ	7T	6
66	2P	DQd		A	5T	5
67	3T	A		A	6R	4
68	2R	A		A	4T	3
69	4N	A		A	4P	2
70	3R	M1		M2	5R	1

Package Outline Unit: mm

119 TERMINAL BGA (PLASTIC)



DETAIL **X**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
BOARD MATERIAL	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE WEIGHT	0.8g

SONY CODE	BGA-119P-01
EIAJ CODE	————
JEDEC CODE	————

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