

CMOS-CCD Signal Processor

Description

The CXL1501M is a CMOS-CCD signal processor designed for 8-mm VCR video signal processing. In combination with the 8-mm VCR video Y/C signal processing IC CXA1200Q, this IC configures a comb filter for Y/C separation in recording an image and elimination of crosstalk in playing back.

Features

- Single power supply 5V
- Low power consumption 225mW (Typ.)
- Built-in peripheral circuits
- Completely adjustment free
- Built-in quadruple progression PLL circuit
- For NTSC signals

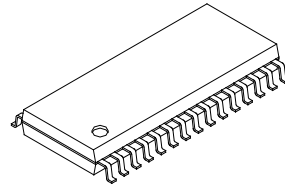
Functions

- 1H comb filter output
- Dropout compensation (D.O.C) output
- Delay time matching through output (THR)
- PLL circuit (quadruple progression)
- Clock driver
- Autobias circuit
- Sync tip clamp circuit
- Sample and hold circuit

Structure

CMOS-CCD

30 pin SOP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

- | | | | |
|-------------------------------|------------------|-------------|----|
| • Supply voltage | V _{DD} | 6 | V |
| • Operating temperature | T _{opr} | -10 to +60 | °C |
| • Storage temperature | T _{stg} | -55 to +150 | °C |
| • Allowable power dissipation | P _D | 500 | mW |

Recommended Operating Conditions (Ta = 25°C)

- | | | | |
|----------------|-----------------|--------|---|
| Supply voltage | V _{DD} | 5 ± 5% | V |
|----------------|-----------------|--------|---|

Recommended Clock Conditions (Ta = 25°C)

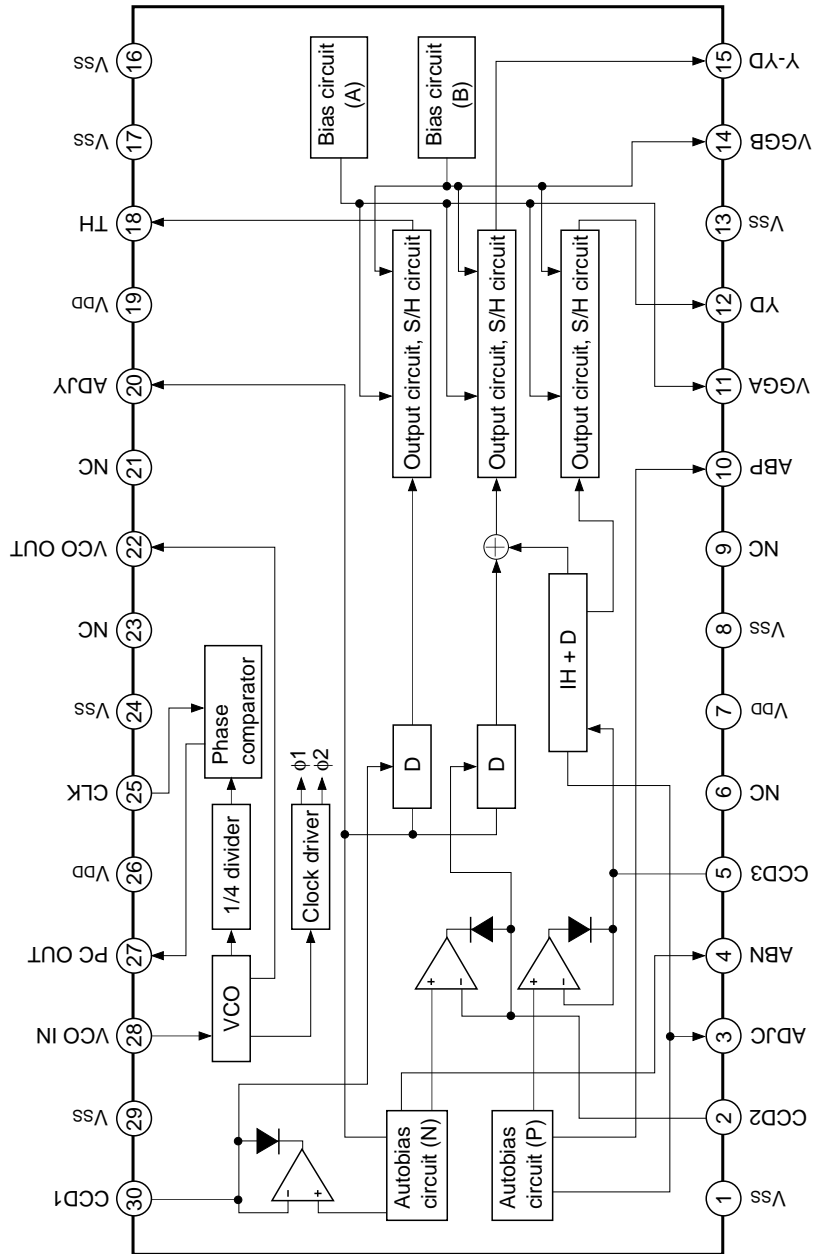
- | | | |
|-------------------------|------------------|---|
| • Input clock amplitude | V _{CLK} | 0.4 to 1.0 V _{p-p}
(0.5V _{p-p} Typ.) |
| • Clock frequency | f _{CLK} | 3.579545 MHz |
| • Input clock waveform | | sine wave |

Input Signal Amplitude

- | | | |
|------------------|-----|-----------------------------|
| V _{SIG} | 571 | mV _{p-p}
(Max.) |
|------------------|-----|-----------------------------|

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Block Diagram and Pin Configuration (Top View)



Pin Description

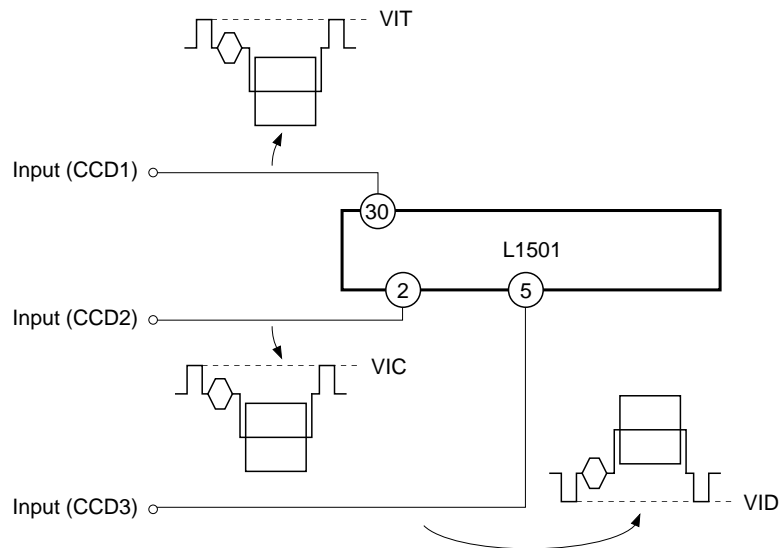
Pin No.	Symbol	I/O	Description	Impedance (Ω)
1	V _{SS}	—	GND	
2	CCD2	I	Signal input 2 (Reverse phase signal)	> 100k (at no clamp)
3	ADJC	O	Forward phase CCD bias DC output	600 to 2k
4	ABN	O	Reverse phase autobias DC output	2k to 20k
5	CCD3	I	Signal input 3 (Forward phase signal)	> 100k (at no clamp)
6	NC	—		
7	V _{DD}	—	5V power supply (For clock driver)	
8	V _{SS}	—	GND	
9	NC	—		
10	ABP	O	Forward phase autobias DC output	2k to 20k
11	VGGA	O	Gate bias (A) DC output	2k to 10k
12	YD	O	D.O.C signal output (Reverse phase signal)	40 to 500
13	V _{SS}	—	GND	
14	VGGB	O	Gate bias (B) DC output	2k to 10k
15	Y-YD	O	Comb filter signal output	40 to 500
16	V _{SS}	—	GND	
17	V _{SS}	—	GND	
18	TH	O	THR signal output (Forward phase signal)	40 to 500
19	V _{DD}	—	5V power supply (For analog)	
20	ADJY	O	Reverse phase CCD bias DC output	600 to 2k
21	NC	—		
22	VCO OUT	O	VCO output	
23	NC	—		
24	V _{SS}	—	GND	
25	CLK	I	Clock input	4k to 40k
26	V _{DD}	—	5V power supply (For digital)	
27	PC OUT	O	Phase comparator output	2k to 5k
28	VCO IN	I	VCO input	> 100k
29	V _{SS}	—	GND	
30	CCD1	I	Signal input 1 (Reverse phase signal)	> 100k (at no clamp)

Notes)

*1 Adjust the output amplitude of the inversion and the non-inversion amplifiers in the signal input block to an equal value, as well as the phase difference to a precise 180°. Also set the clock and input signal frequency accurately.

*2 VIT, VIC and VID are defined as follows:

VIT, VIC and VID are input signal clamp levels. They clamp the Video signal sync tip level. They are the pin voltages at no-input signal for pins 30, 2 and 5, respectively.



Testing of VIT, VIC and VID is executed with a voltmeter under the following SW conditions:

Item	SW conditions											Test point
	1	2	3	4	5	6	7	8	9	10	11	
VIT	—	b	b	b	a	a	a	—	—	—	—	V1
VIC	—	b	b	b	a	a	a	—	—	—	—	V2
VID	—	b	b	b	a	a	a	—	—	—	—	V3

As VIT, VIC and VID differ with each IC, they are to be tested respectively.

*3 This is the IC supply current value during clock and signal input.

*4 GLT, GLC and GLD are output gains of TH, Y-YD, and YD pins when a 500mVp-p, 196.678kHz sine wave is simultaneously fed to CCD1, CCD2, and CCD3 pins respectively.

(Example of calculation)

$$GLT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

- *5 GHT, GHC, and GHD are output gains of TH, Y-YD and YD pins when a 150mVp-p, 3.579545MHz sine wave is simultaneously fed to CCD1, CCD2, and CCD3 pins respectively. Bias at input (V_{BIAS1} , V_{BIAS2} and V_{BIAS3}) is tested respectively at $V_{IT} - 0.25V$, $V_{IC} - 0.25V$ and $V_{ID} + 0.25V$.

(Example of calculation)

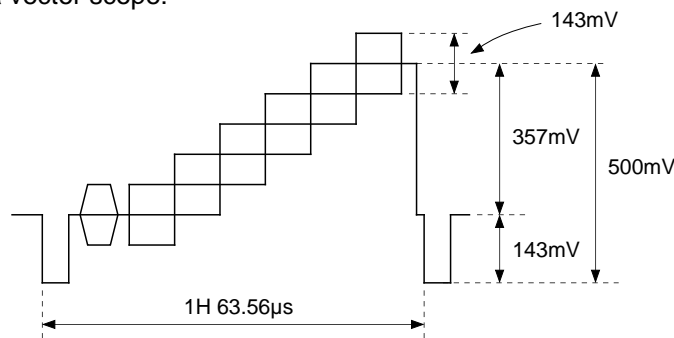
$$GHT = 20 \log \frac{\text{TH pin output voltage [mVp-p]}}{150 \text{ [mVp-p]}} \text{ [dB]}$$

- *6 Indicates the dissipation at 3.579545MHz in relation to 196.678kHz. From the output voltage at TH, Y-YD and YD pins when a 150mVp-p, 196.678kHz sine wave is simultaneously fed to CCD1, CCD2 and CCD3 pins, and from the output voltage at TH, Y-YD and YD pins when a 150mVp-p, 3.579545MHz sine wave is simultaneously fed to same, calculation is made according to the following formula. The input block bias for V_{BIAS1} , V_{BIAS2} and V_{BIAS3} is tested at $V_{IT} - 0.25V$, $V_{IC} - 0.25V$ and $V_{ID} + 0.25V$, respectively.

(Example of calculation)

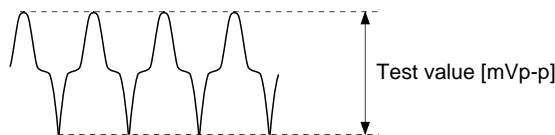
$$fT = 20 \log \frac{\text{TH pin output voltage (3.579545MHz) [mVp-p]}}{\text{TH pin output voltage (196.678kHz) [mVp-p]}} \text{ [dB]}$$

- *7 The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the following figure is fed, are tested with a vector scope:



CCD3 pin input waveform (the input waveform of CCD1 and CCD2 pins is the inverted waveform of the figure above.)

- *8 The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input block bias is tested at V_{ITV} , V_{ICV} , and $V_{ID} + 0.5V$.



*9 The noise level of output signal at no-input signal is tested with a video noise meter in the Sub Carrier Trap mode at BPF 100kHz to 4MHz. V_n [Vrms]

The signal component is determined either by testing the output voltage (the same test system as that of noise level) at input of 357mVp-p, 196.678kHz, or by performing calculation from the values of GLT, GLC, and GLD in accordance with the following formula. V_s [Vp-p]

(Example of V_s calculation)

$$V_{S-T} = 0.357 \times 10^{\frac{GLT}{20}} \quad (V_{S-T}: \text{TH output voltage})$$

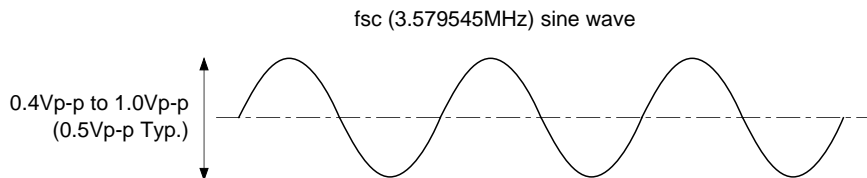
(Example of S/N ratio calculation)

$$SNT = 20 \log \frac{V_{n-T} \text{ (noise component) [Vrms]}}{V_{S-T} \text{ (signal component) [Vp-p]}} \text{ [dB]}$$

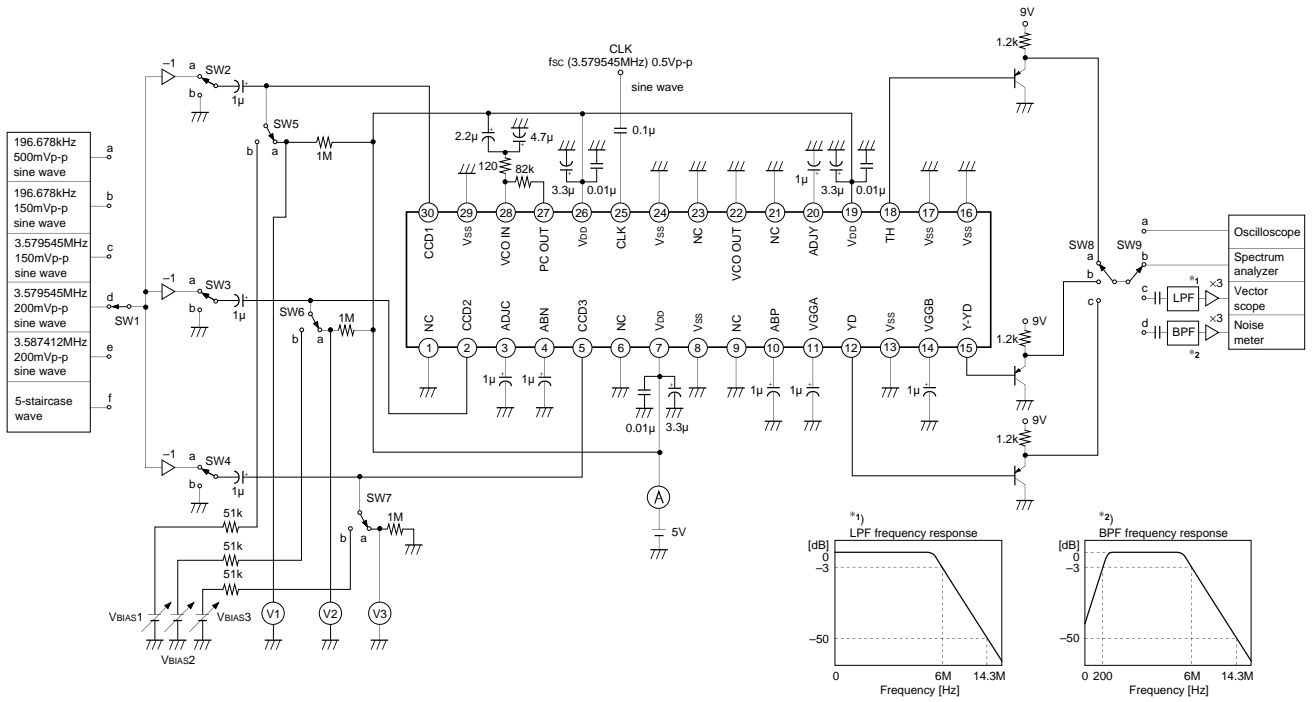
*10 C-CD is calculated in accordance with the following formula from the Y-YD pin output voltage when a 200mVp-p, 3.579545MHz sine wave is simultaneously fed to CCD1, CCD2 and CCD3 pins and from the Y-CD pin output voltage when a 200mVp-p, 3.587412MHz sine wave is simultaneously fed to same. The input block bias is set to VIT – 0.3V, VIC – 0.3V and VID + 0.3V, respectively.

$$C-CD = 20 \log \frac{\text{Y-YD pin output voltage (3.587412MHz) [mVp-p]}}{\text{Y-YD pin output voltage (3.579545MHz) [mVp-p]}} \text{ [dB]}$$

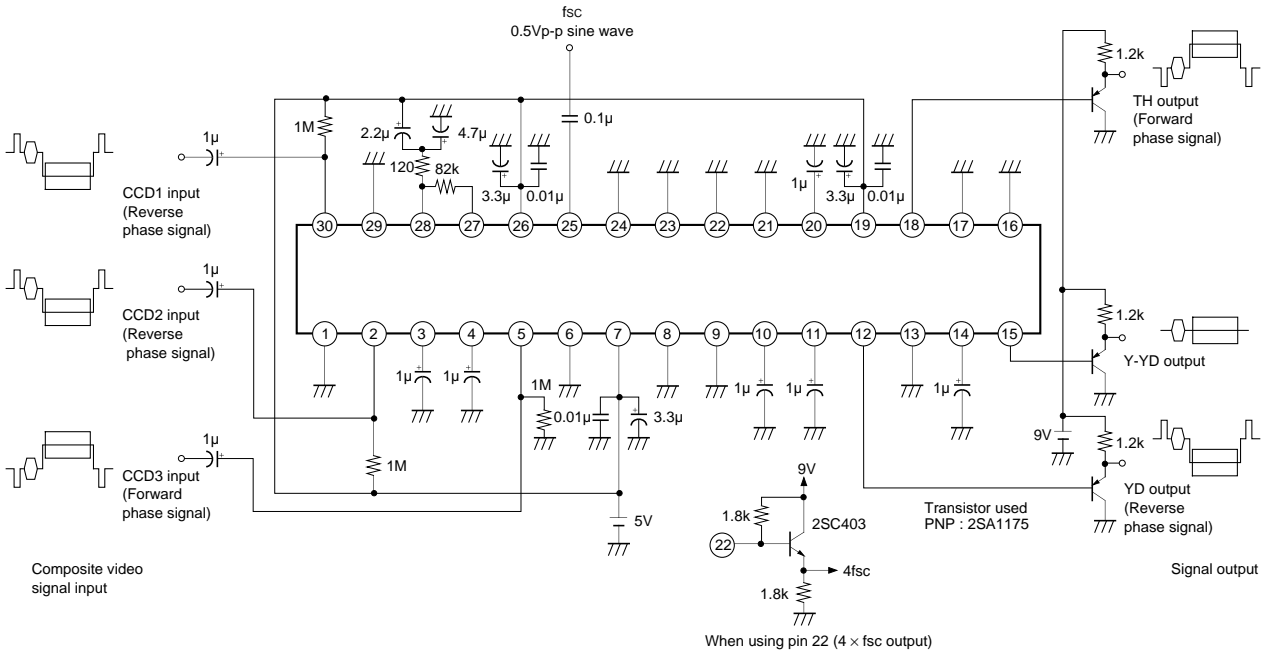
CLOCK



Electrical Characteristics Test Circuit

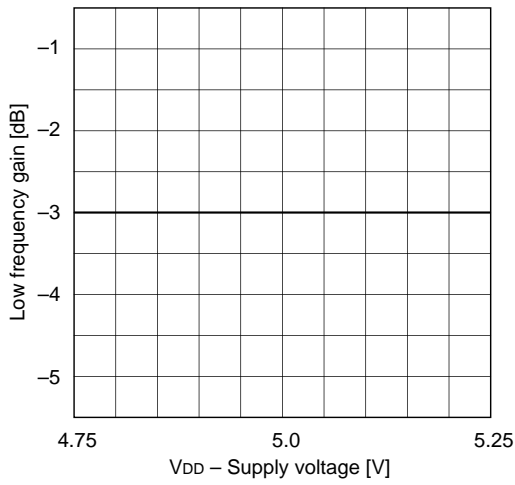


Application Circuit

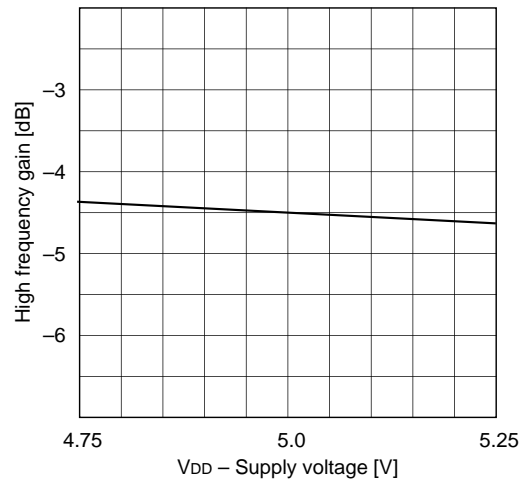


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

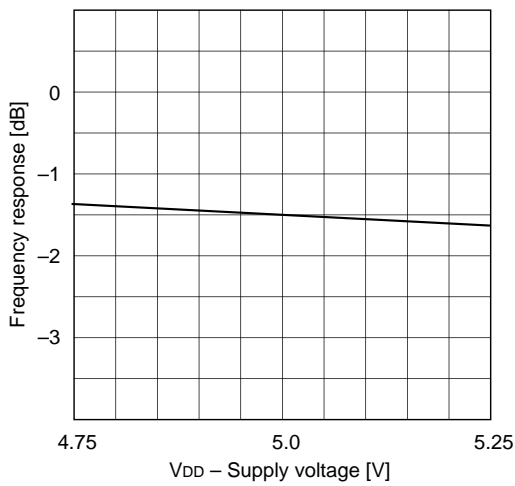
Low frequency gain vs. Supply voltage



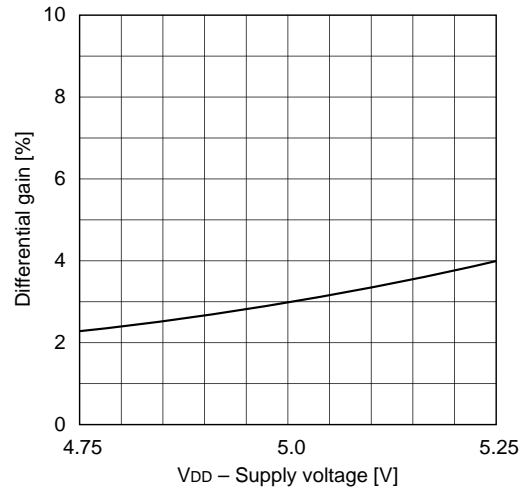
High frequency gain vs. Supply voltage



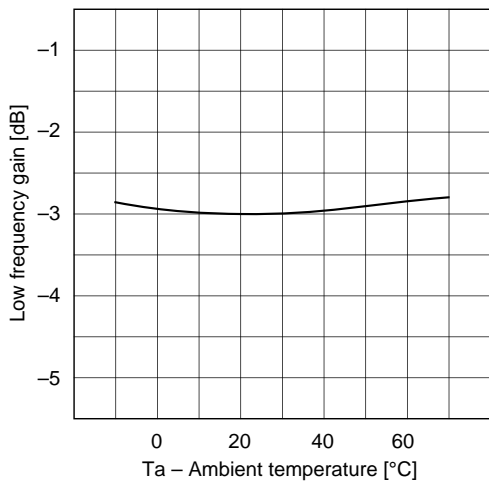
Frequency response vs. Supply voltage



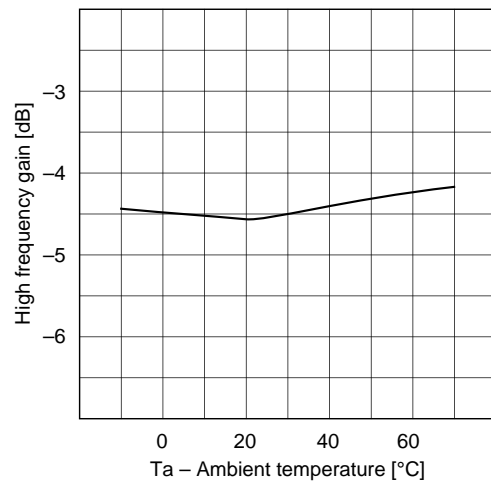
Differential gain vs. Supply voltage



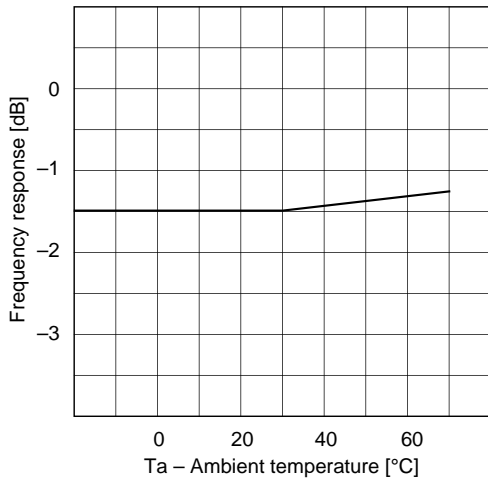
Low frequency gain vs. Ambient temperature



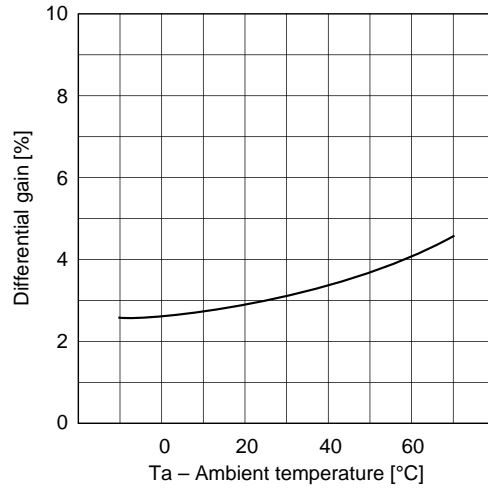
High frequency gain vs. Ambient temperature



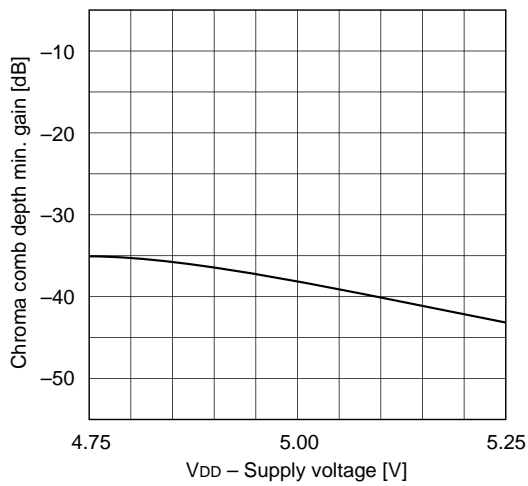
Frequency response vs. Ambient temperature



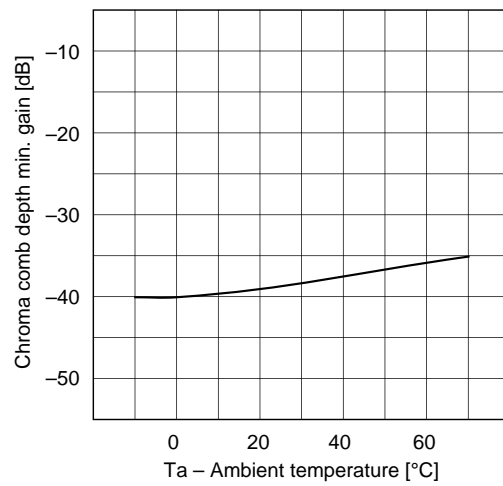
Differential gain vs. Ambient temperature



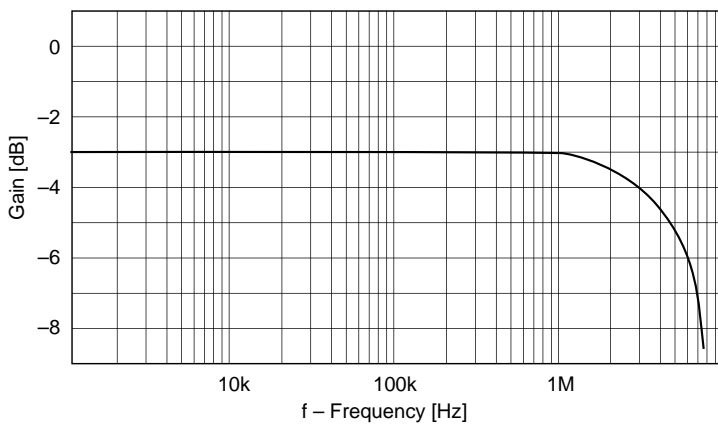
Chroma comb depth min. gain vs. Supply voltage



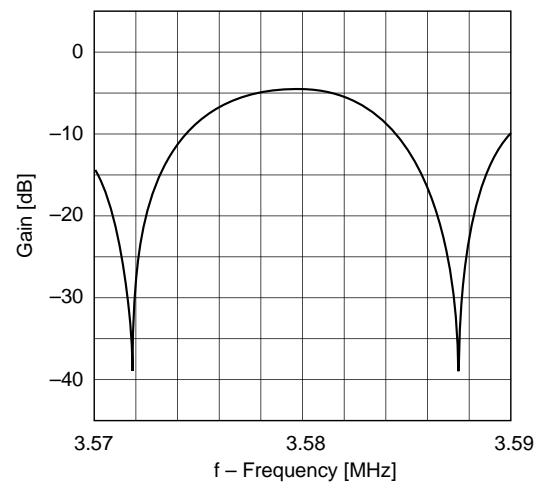
Chroma comb depth min. gain vs. Ambient temperature



Frequency response (TH, YD Output)

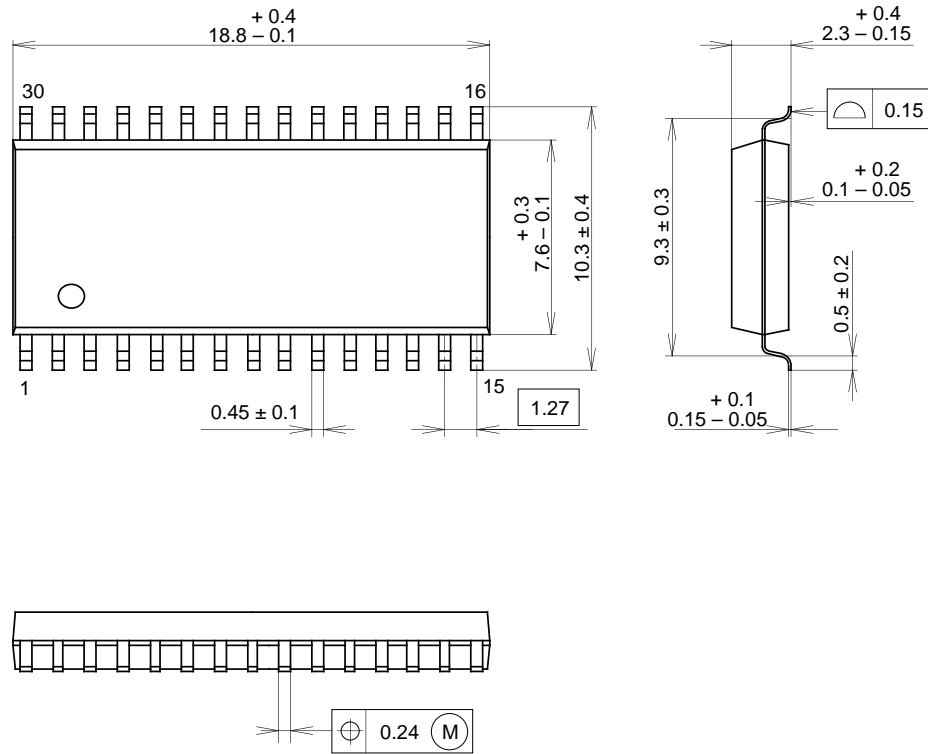


Chroma comb response (Y-YD Output)



Package Outline Unit: mm

30PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-30P-L01
EIAJ CODE	SOP030-P-0375
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.7g



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