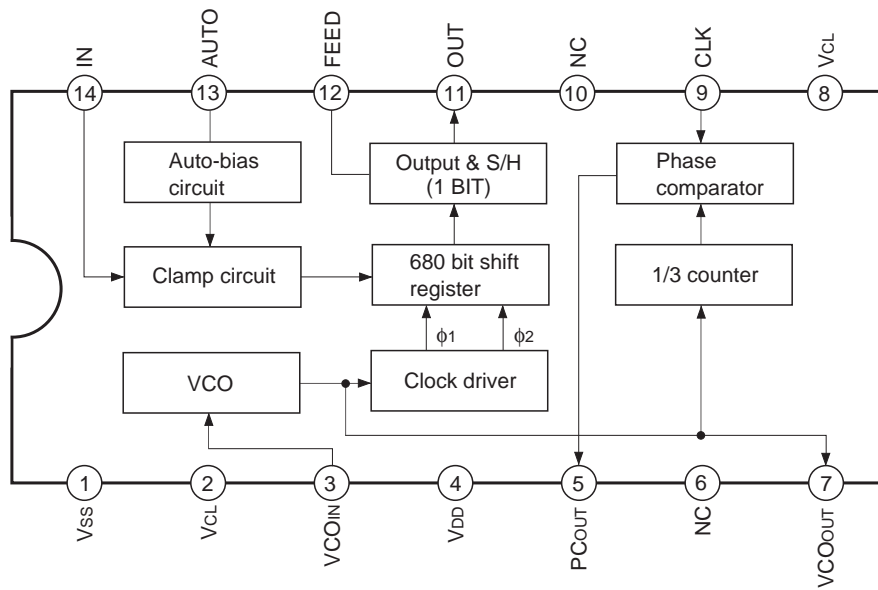


Block Diagram and Pin configuration



Pin Description

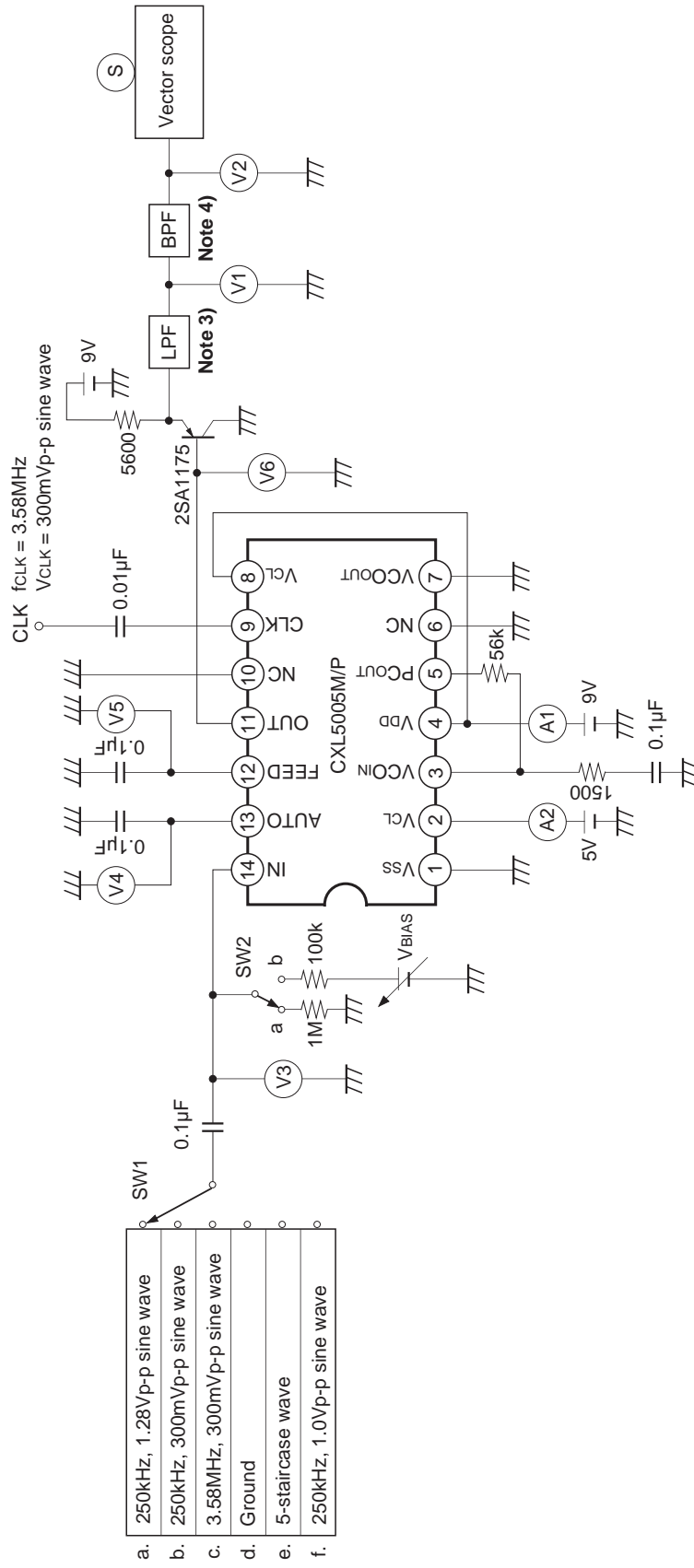
Pin No.	Symbol	Description	Impedance [Ω]
1	VSS	GND	
2	VCL	5V power supply	
3	VCO _{IN}	VCO input	> 100k
4	VDD	9V power supply	
5	PC _{OUT}	Phase comparator output	\approx 5k
6	NC		
7	VCO _{OUT}	VCO output	\approx 5k
8	VCL	5V power supply	
9	CLK	Clock input	\approx 5k
10	NC		
11	OUT	Signal output	600 to 1k
12	FEED	Feedback DC output	> 100k
13	AUTO	Autobias DC output	\approx 10k
14	IN	Signal input	> 100k

Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{DD} = 9.0\text{V}$, $V_{CL} = 5.0\text{V}$, $f_{CLK} = 3.58\text{MHz}$, $V_{CLK} = 300\text{mVp-p}$ sine wave,
See "Electrical Characteristics Test Circuit")

Item	Symbol	Test condition	SW condition		Measuring point	Min.	Typ.	Max.	Unit
			1	2					
Supply current	I _{DD}	250kHz, 1.28Vp-p, sine wave input	a	a	A1	—	4.0	5.0	mA
	I _{CL}				A2	—	9.0	12.0	mA
Insertion gain	IG	250kHz, 1.28Vp-p, sine wave input IG = 20 log (Output voltage [Vp-p] / 1.28 [Vp-p])	a	a	V1	-3.0	0.0	3.0	dB
Frequency response	fG	Dissipation at 3.58MHz in relation to 250kHz fG = 20 log (V _{3.58MHz} / V _{250kHz}) (Note 1)	b, c	b	V1	-3.0	-2.1	—	dB
Differential gain	DG	5-staircase wave input Y = 140 IRE (= 1.0Vp-p) Measure with vector scope (Note 2)	e	a	S	—	3.0	5.0	%
Differential phase	DP					—	3.0	5.0	deg
Allowable input amplitude	V _{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: Input = 250kHz, 1.0Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: Input = DC GND output (V _{rms})	d	a					
DC output voltage	V _{IN-DC}		d	a	V3	3.5	5.0	6.5	V
	V _{AUTO-DC}				V4	3.5	5.0	6.5	V
	V _{FEED-DC}	250kHz, 1.28Vp-p, sine wave input	a	a	V5	1.3	2.3	3.3	V
	V _{OUT-DC}				V6	1.7	2.7	3.7	V

Electrical Characteristics Test Circuit

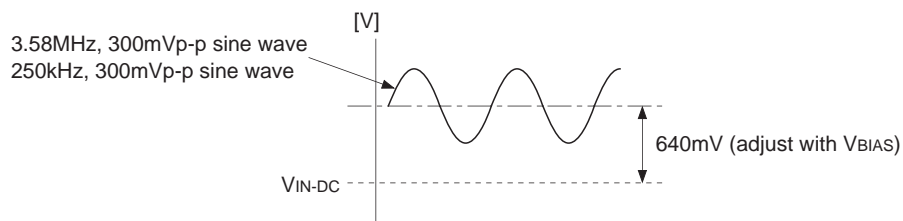


Note 1) Frequency response test condition

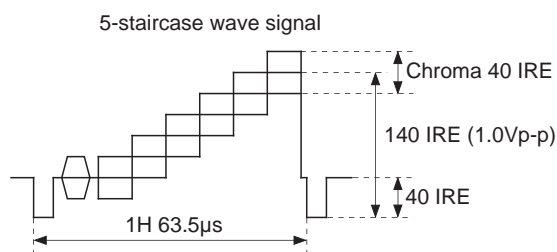
$V_{3.58\text{MHz}}$ (Output signal voltage [Vp-p] at 3.58MHz input)

$V_{250\text{kHz}}$ (Output signal voltage [Vp-p] at 250kHz input)

Set Pin 14 (IN) voltage [V] = $V_{\text{IN-DC}} + 640\text{mV}$.

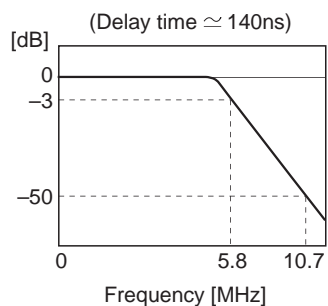


Note 2) Differential gain and differential phase test condition

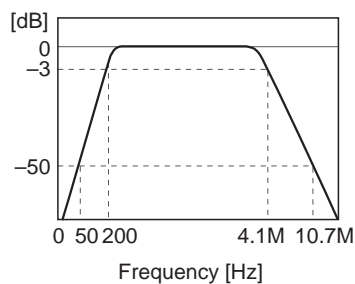


DG and DP are measured at output S point by vector scope.

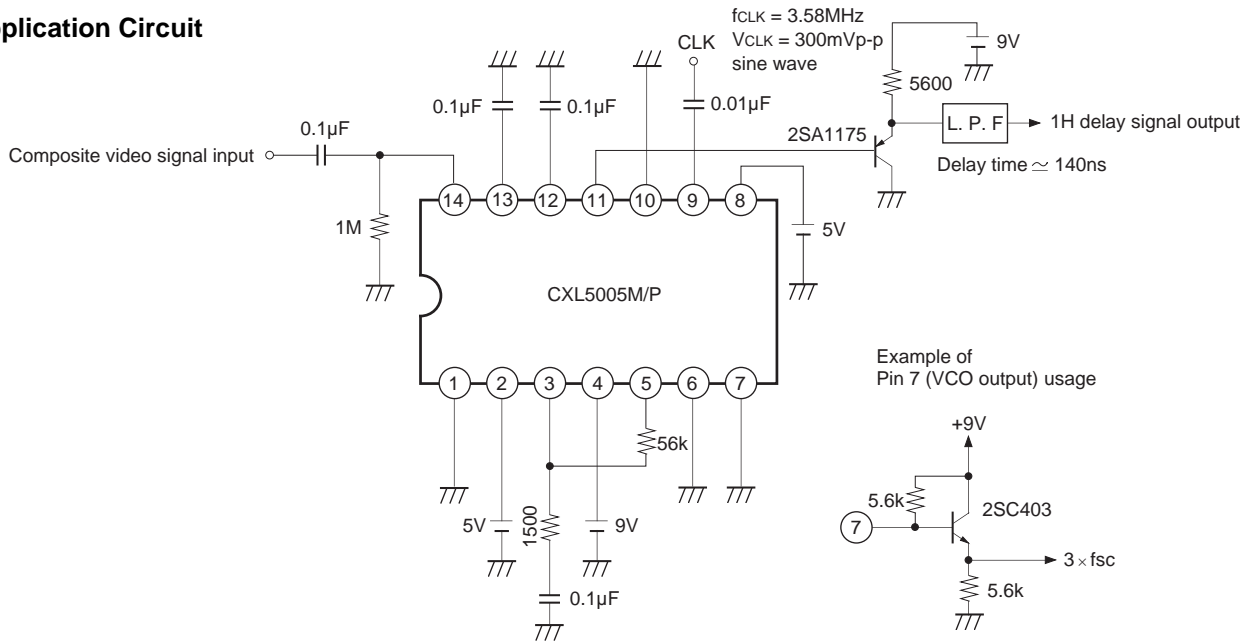
Note 3) LPF frequency response



Note 4) BPF frequency response

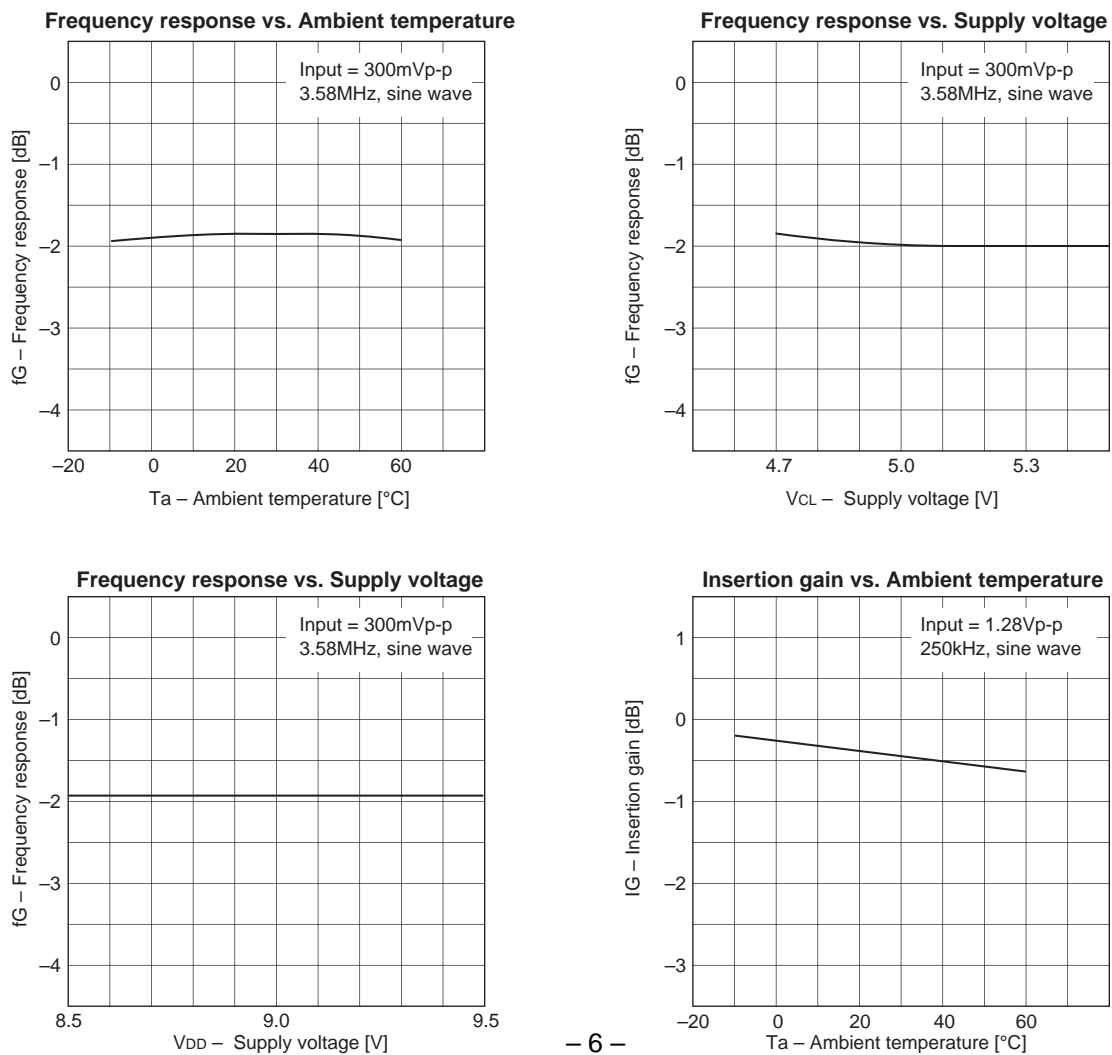


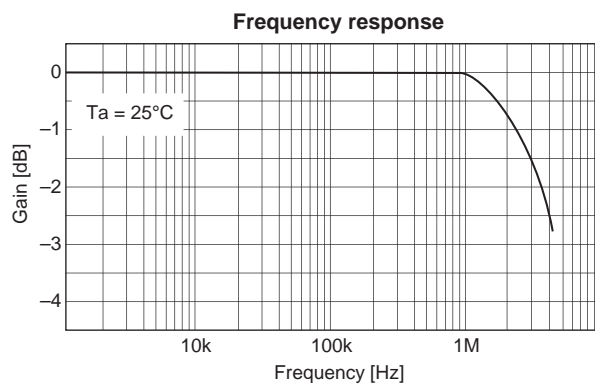
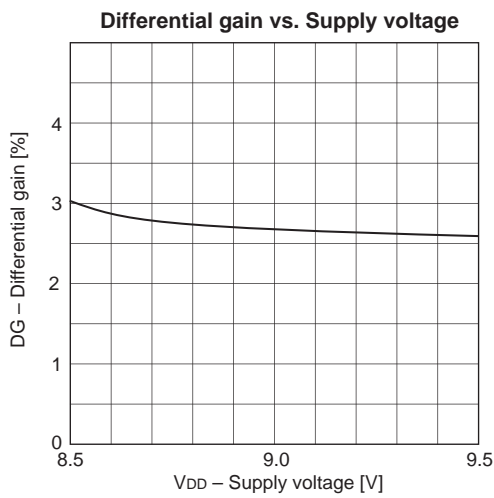
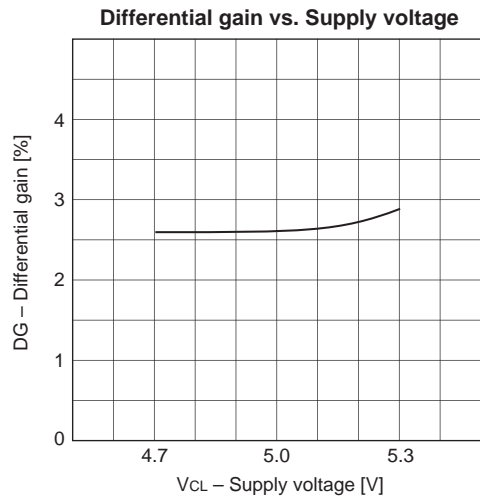
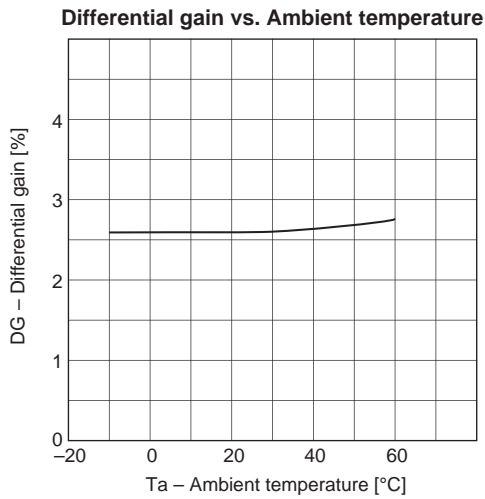
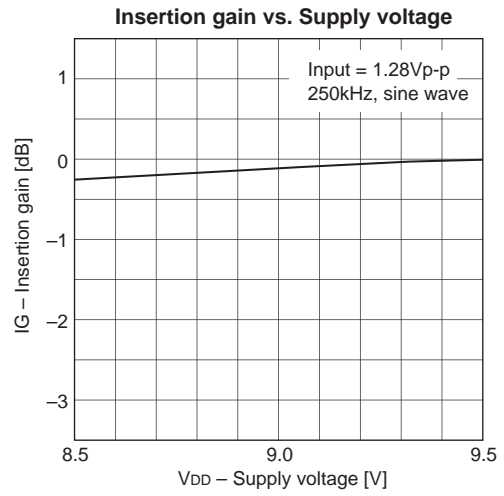
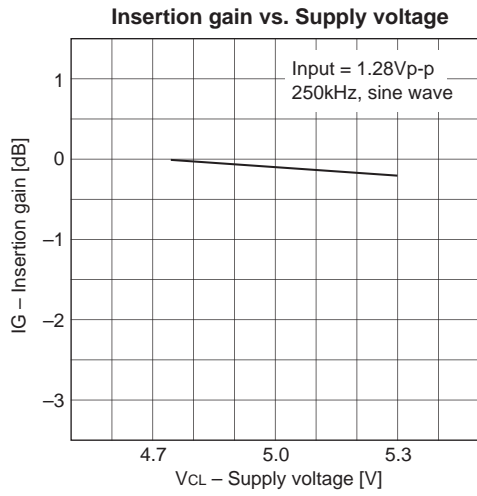
Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

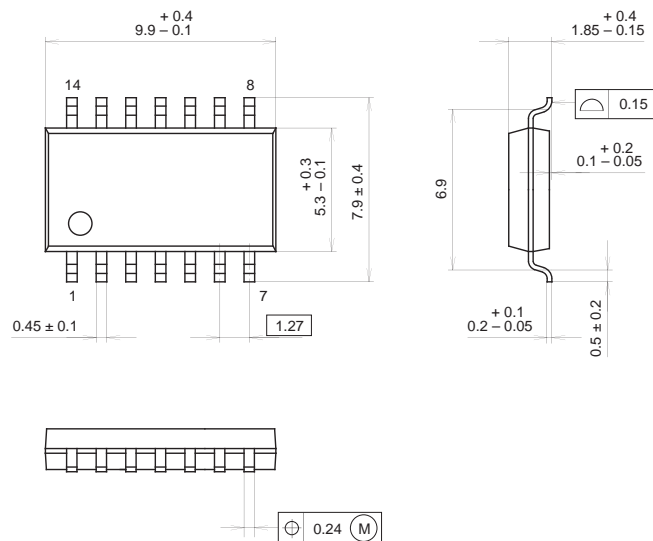




Package Outline Unit: mm

CXL5005M

14PIN SOP (PLASTIC)



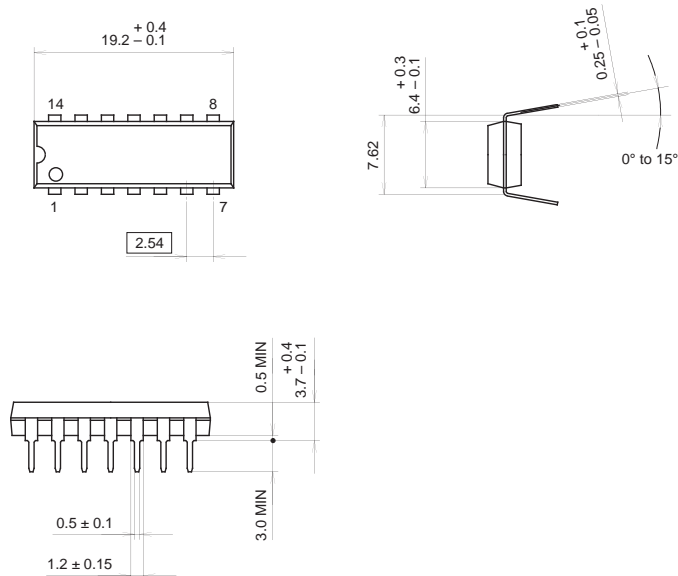
PACKAGE STRUCTURE

SONY CODE	SOP-14P-L01
EIAJ CODE	SOP014-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

CXL5005P

14PIN DIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	DIP-14P-01
EIAJ CODE	DIP014-P-0300
JEDEC CODE	Similar to MO-001-AH

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.9g

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