



# 128K x 16 Static RAM

## Features

- Low voltage range:
  - CY62136V: 2.7V-3.6V
- Ultra-low active, standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

## Functional Description

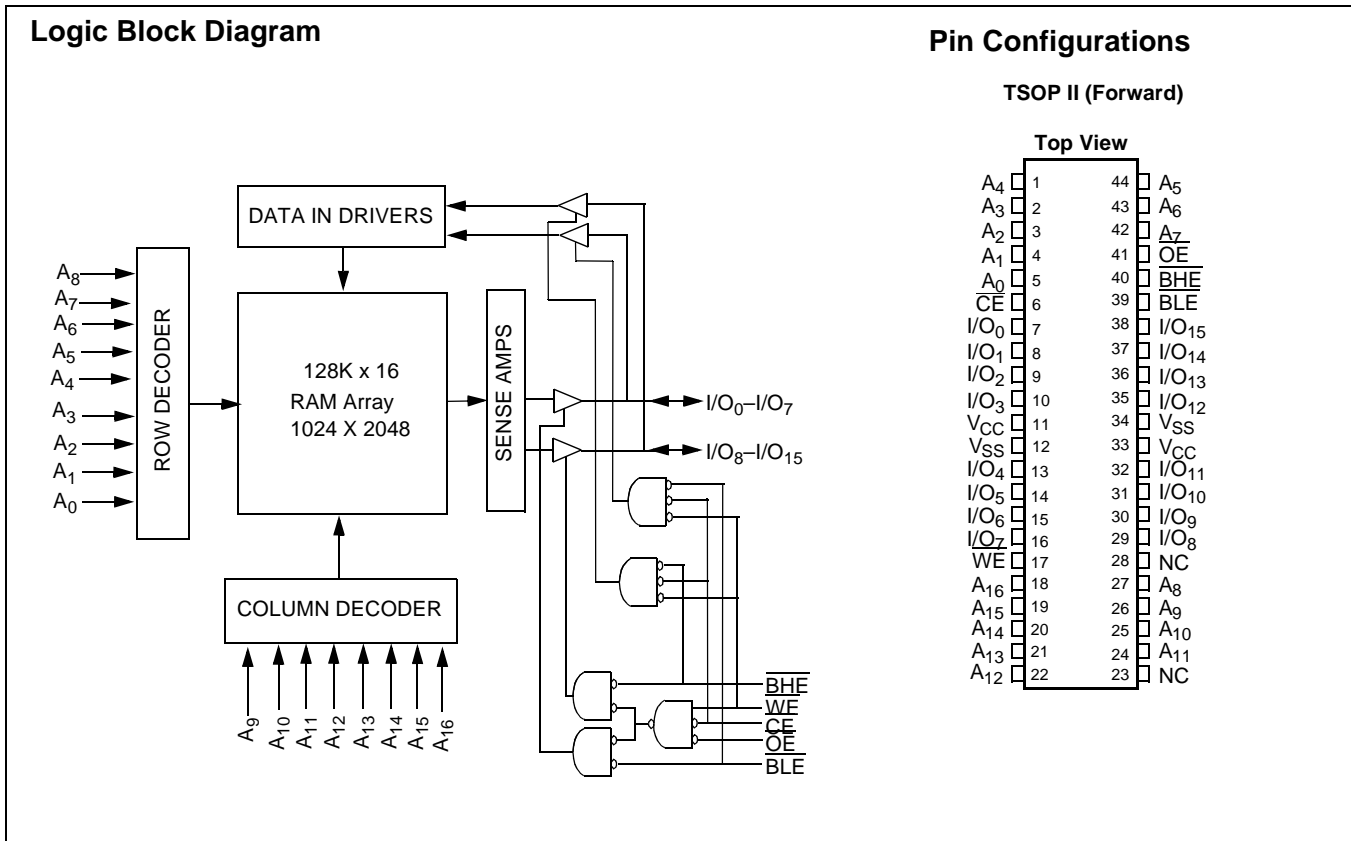
The CY62136V is a high-performance CMOS static RAM organized as 131,072 words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$

HIGH), outputs are disabled ( $\overline{OE}$  HIGH),  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

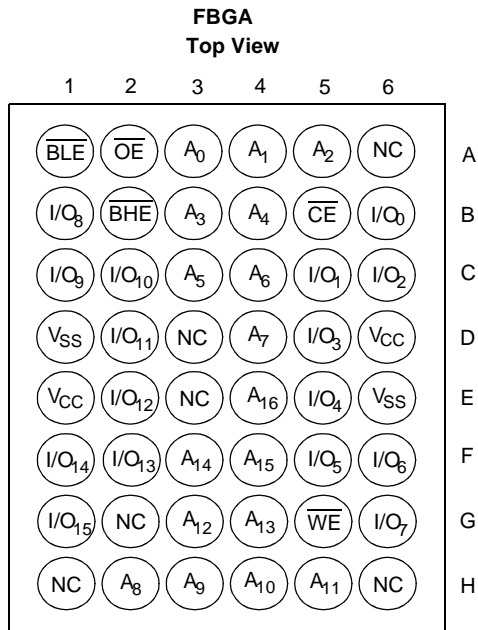
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the Truth Table at the back of this data sheet for a complete description of read and write modes.

The CY62136V is available in 48-ball FBGA and standard 44-pin TSOP Type II (forward pinout) packaging.



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**Pin Configurations (continued)**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential.....	-0.5V to +4.6V

**DC Voltage Applied to Outputs**

in High Z State <sup>[1]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
DC Input Voltage <sup>[1]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current.....	>200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub>
CY62136V	Industrial	-40°C to +85°C	2.7V to 3.6V

**Product Portfolio**

Product	V <sub>CC</sub> Range			Power	Power Dissipation (Industrial)			
	V <sub>CC</sub> (min.)	V <sub>CC</sub> (typ.) <sup>[2]</sup>	V <sub>CC</sub> (max.)		Operating (I <sub>CC</sub> )		Standby (I <sub>SB2</sub> )	
					Typ. <sup>[2]</sup>	Maximum	Typ. <sup>[2]</sup>	Maximum
CY62136V	2.7V	3.0V	3.6V	LL	7 mA	15 mA	1 μA	15 μA

**Notes:**

- V<sub>IL</sub>(min) = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> Typ, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions		CY62136V			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage		V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>CC</sub> = 2.7V	-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1	+1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS levels	V <sub>CC</sub> = 3.6V		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = f <sub>MAX</sub>				100	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , f = 0	V <sub>CC</sub> = 3.6V	LL	1	15	μA

**Capacitance<sup>[3]</sup>**

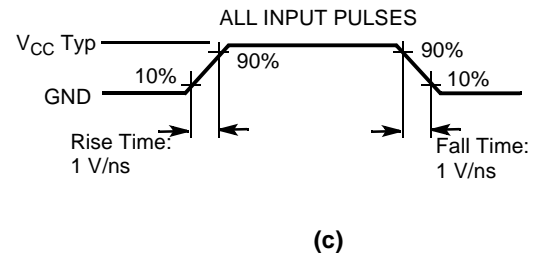
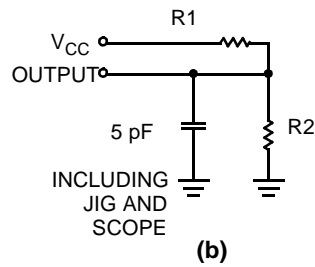
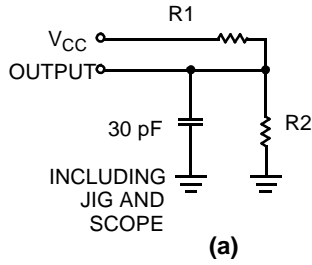
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

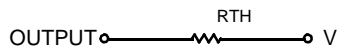
Description	Test Conditions	Symbol	BGA	TSOPII	Unit
Thermal Resistance (Junction to Ambient) <sup>[3]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ <sub>JA</sub>	55	60	°C/W
Thermal Resistance (Junction to Case) <sup>[3]</sup>		θ <sub>JC</sub>	16	22	°C/W

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


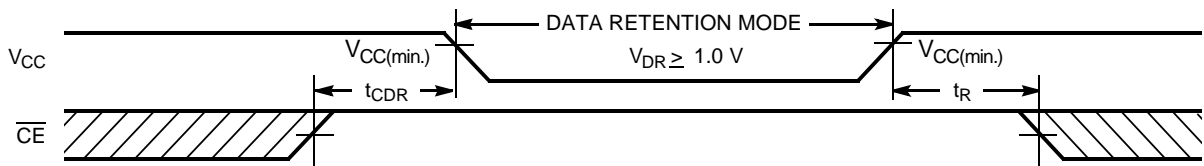
Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.0V	UNIT
R1	1105	Ohms
R2	1550	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75V	Volts

**Data Retention Characteristics (Over the Operating Range)**

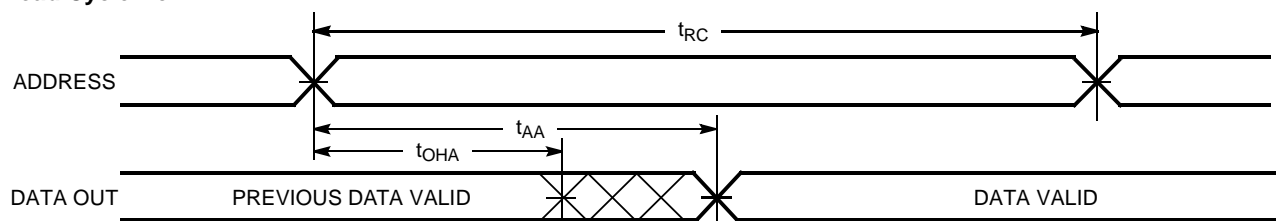
Parameter	Description	Conditions <sup>[5]</sup>	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V No input may exceed V <sub>CC</sub> +0.3V	LL	0.5	7.5	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[4]</sup>	Operation Recovery Time		70			ns

**Data Retention Waveform**

**Notes:**

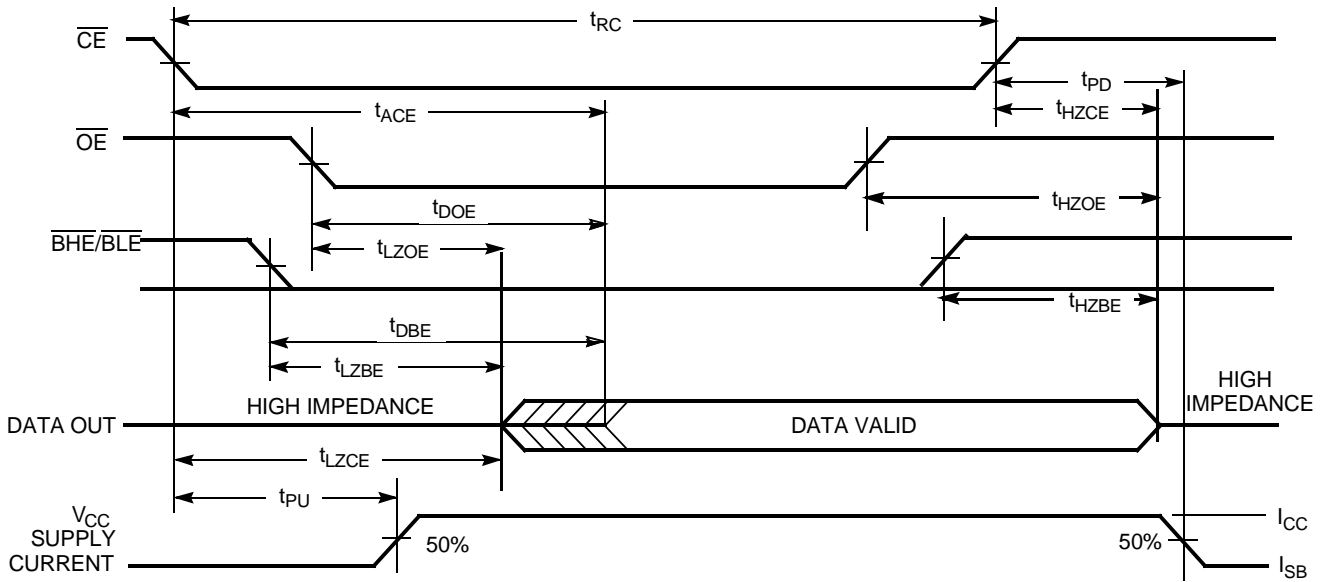
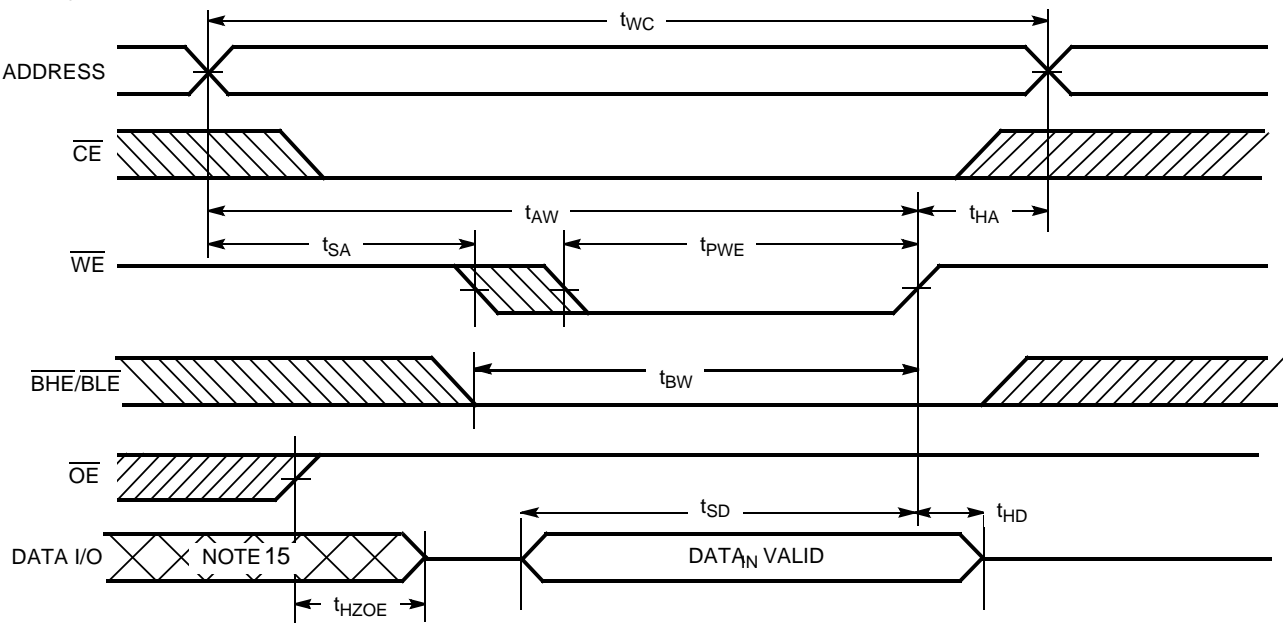
- Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 ms or stable at V<sub>CC(min)</sub> ≥ 100 ms.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC</sub> typ., and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

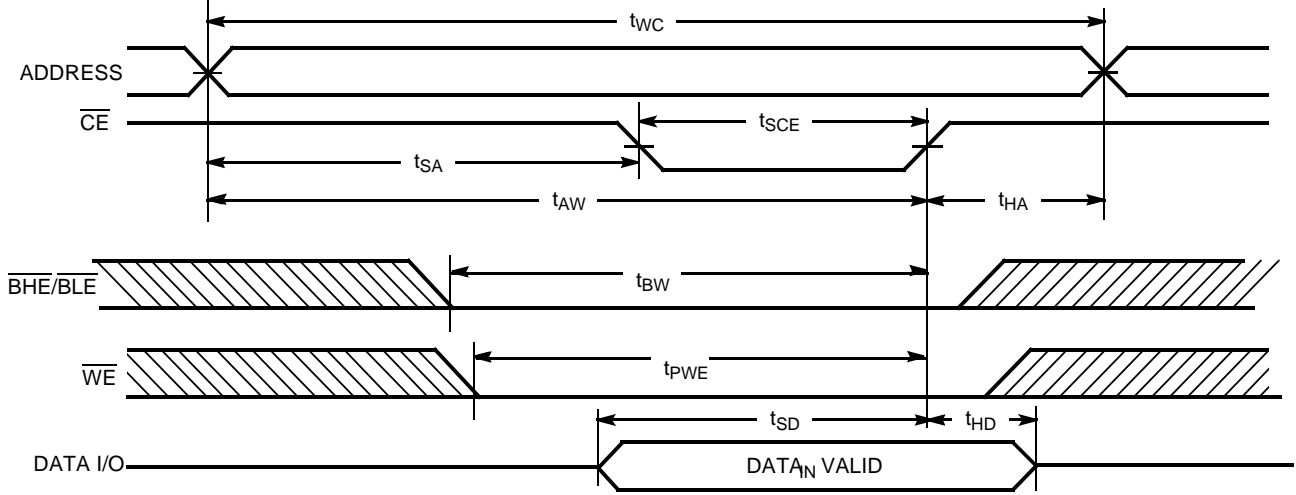
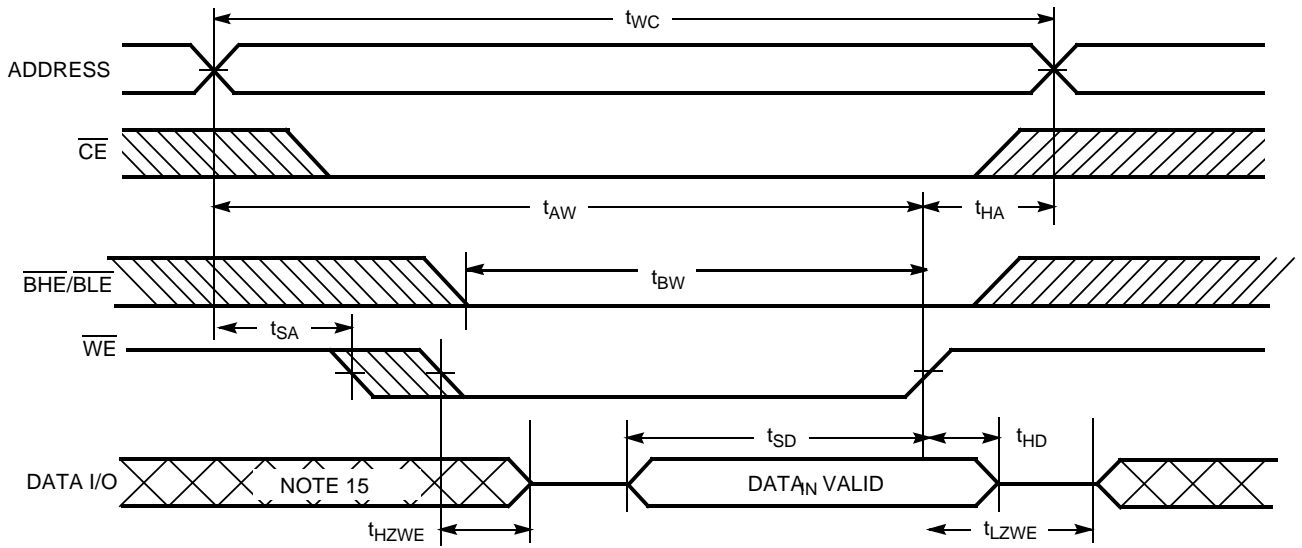
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AA}$	Address to Data Valid		55		70	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		55		70	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		25		35	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		25		25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		25		25	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		55		70	ns
$t_{DBE}$	$\overline{BLE} / \overline{BHE}$ LOW to Data Valid		25		35	ns
$t_{LZBE}$	$\overline{BLE} / \overline{BHE}$ LOW to Low Z <sup>[6, 7]</sup>	5		5		ns
$t_{HZBE}$	$\overline{BLE} / \overline{BHE}$ HIGH to High Z <sup>[8]</sup>		25		25	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>						
$t_{WC}$	Write Cycle Time	55		70		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	45		60		ns
$t_{AW}$	Address Set-Up to Write End	45		60		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	40		50		ns
$t_{BW}$	$\overline{BLE} / \overline{BHE}$ LOW to Write End	50		60		ns
$t_{SD}$	Data Set-Up to Write End	25		30		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		20		25	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		10		ns

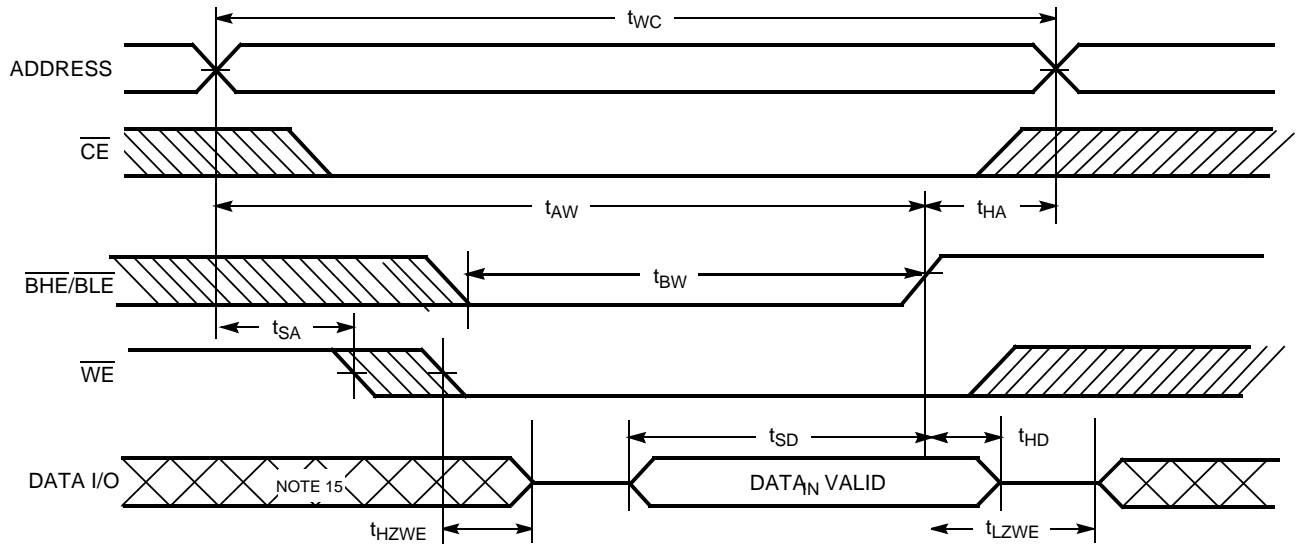
**Switching Waveforms**
**Read Cycle No. 1<sup>[10, 11]</sup>**

**Notes:**

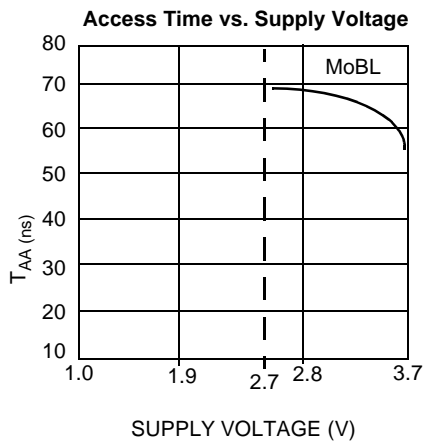
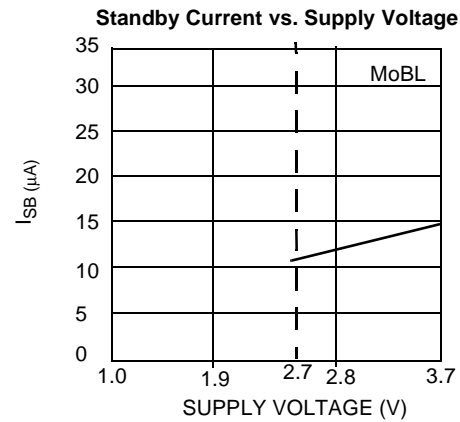
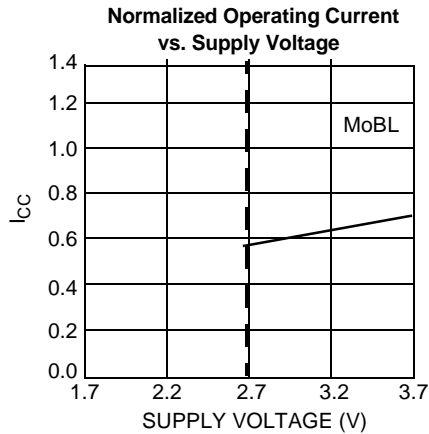
6. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
7.  $t_{LZOE}$ ,  $t_{HZCE}$ , and  $t_{LZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 [11, 12]**

**Write Cycle No. 1 (WE Controlled) [8, 13, 14]**

**Notes:**

12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high impedance if  $OE = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)<sup>[8, 13, 14]</sup>**

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[9, 14]</sup>**


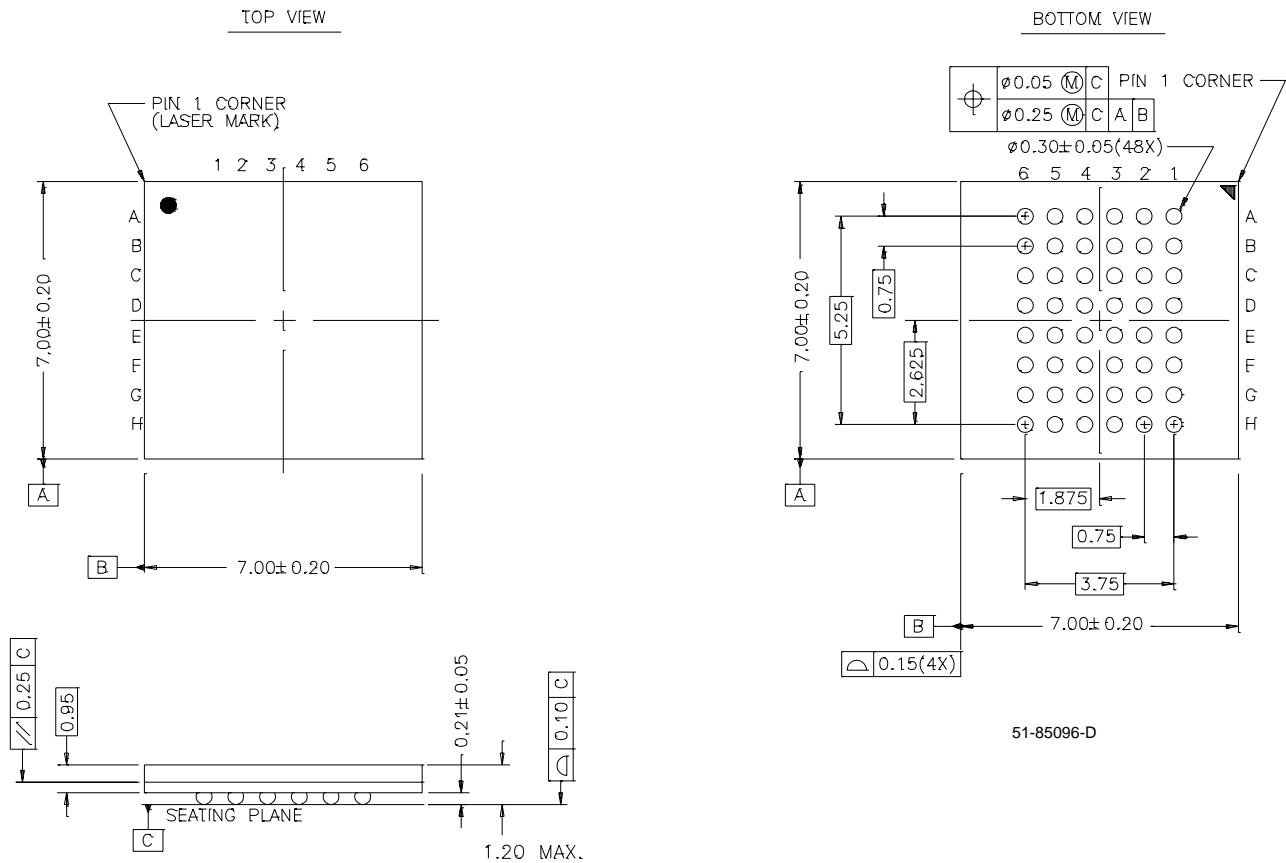
**Switching Waveforms (continued)**
**Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)<sup>[15]</sup>**


**Typical DC and AC Characteristics**

**Truth Table**

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High Z	Write	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136VLL-55ZI	Z44	44-Pin TSOP II	Industrial
	CY62136VLL-55BAI	BA48	48-Ball Fine Pitch BGA	
70	CY62136VLL-70ZI	Z44	44-Pin TSOP II	
	CY62136VLL-70BAI	BA48	48-Ball Fine Pitch BGA	

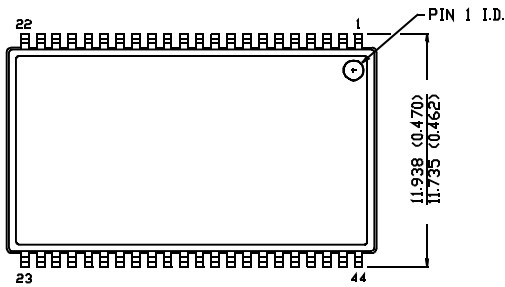
**Package Diagrams**
**48-Ball (7.00 mm x 7.00 mm) FBGA BA48**




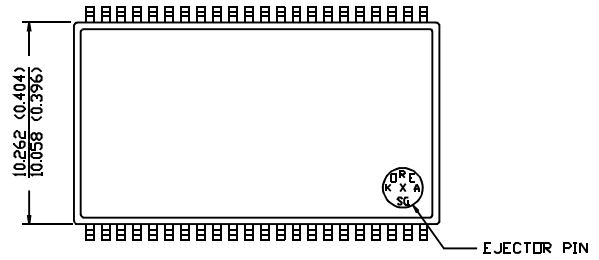
**Package Diagrams** (continued)

**44-Pin TSOP II Z44**

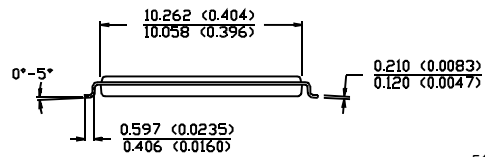
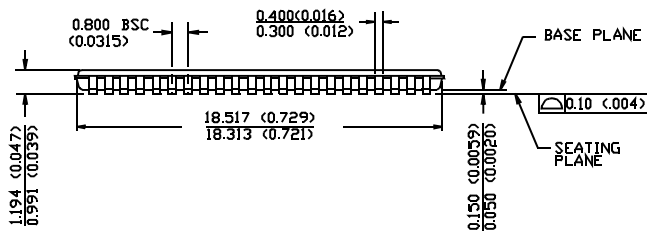
DIMENSION IN MM (INCH)  
 MAX  
 MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A



<b>Document Title: CY62136V MoBL™ 128K x 16 Static RAM</b> <b>Document Number: 38-05087</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Oreg. of Change</b>	<b>Description of Change</b>
**	107347	05/25/01	SZV	Change from Spec #: 38-00728 to 38-05087



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