

# 4M (256K x 16) Static RAM

## Features

- Wide voltage range: 2.7V–3.6V
- Ultra-low active, standby power
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Package available in a standard 44-Pin TSOP Type II (forward pinout) package

## Functional Description<sup>[1]</sup>

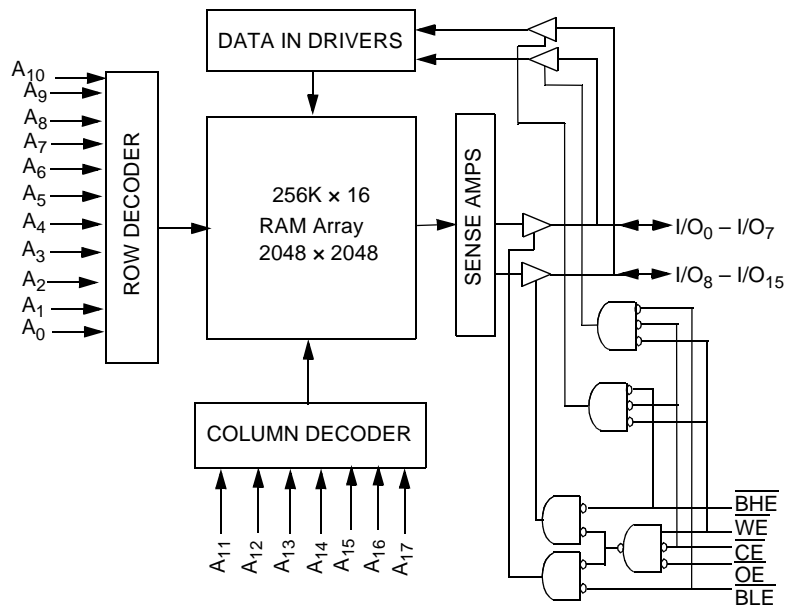
The CY62146V is a high-performance CMOS static RAM organized as 256K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life<sup>®</sup> (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when

deselected ( $\overline{CE}$  HIGH). The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH),  $BHE$  and  $BLE$  are disabled ( $BHE$ ,  $BLE$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $BLE$ ) is LOW, then data from  $I/O$  pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $BHE$ ) is LOW, then data from  $I/O$  pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $BLE$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $BHE$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

## Logic Block Diagram

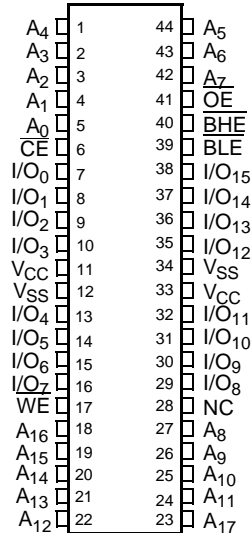


### Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Pin Configurations

**TSOP II (Forward)  
Top View**



### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage to Ground Potential .....	-0.5V to +4.6V
DC Voltage Applied to Outputs in High-Z State <sup>[2]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
DC Input Voltage <sup>[2]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)
Latch-up Current.....	>200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V

### Product Portfolio

Product	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
	V <sub>CC(min.)</sub>	V <sub>CC(typ.)</sub> <sup>[3]</sup>	V <sub>CC(max.)</sub>		Operating I <sub>CC</sub> , (mA)		Standby I <sub>SB2</sub> , (µA)	
					Typ. <sup>[3]</sup>	Maximum	Typ. <sup>[3]</sup>	Maximum
CY62146VLL	2.7	3.0	3.6	70	7	15	2	20

**Notes:**

- V<sub>IL(min.)</sub> = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

**Electrical Characteristics** Over the Operating Range

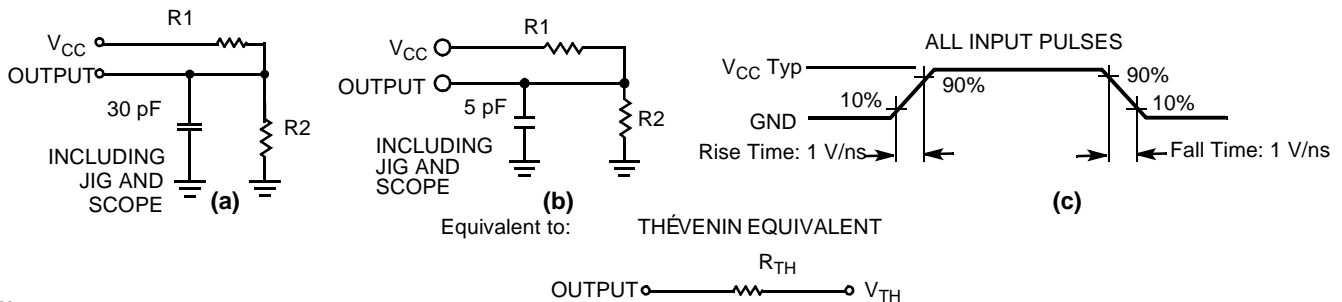
Parameter	Description	Test Conditions	CY62146V-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA, V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 3.6V	2.2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 2.7V	-0.5		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	±1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , CMOS Levels		7	15	mA
		I <sub>OUT</sub> = 0 mA, f = 1 MHz, CMOS Levels		1	2	mA
I <sub>SB1</sub>	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = f <sub>MAX</sub>		2	20	μA
I <sub>SB2</sub>	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	V <sub>CC</sub> = 3.6V			

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC</sub> (typ.)	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

Parameter	Description	Test Conditions	BGA	TSOPII	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) <sup>[4]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	55	60	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case) <sup>[4]</sup>		16	22	°C/W

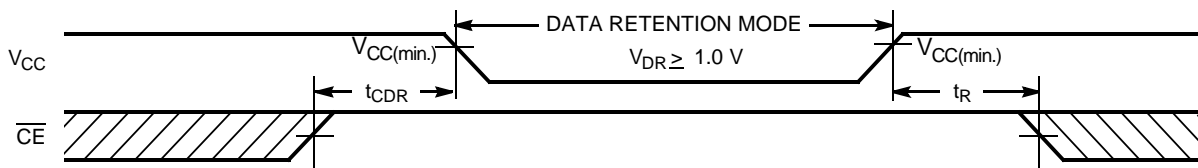
**AC Test Loads and Waveforms**

**Note:**

4. Tested initially and after any design or process changes that may affect these parameters.

Parameter	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75	V

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention)		1.0		3.6	V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 1.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V; No input may exceed V <sub>CC</sub> + 0.3V		1	10	μA
t <sub>CDR</sub> <sup>[4]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[5]</sup>	Operation Recovery Time		70			ns

**Data Retention Waveform**

**Switching Characteristics** Over the Operating Range <sup>[6]</sup>

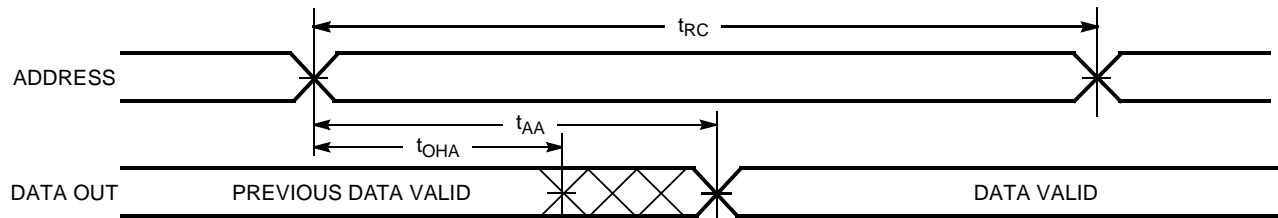
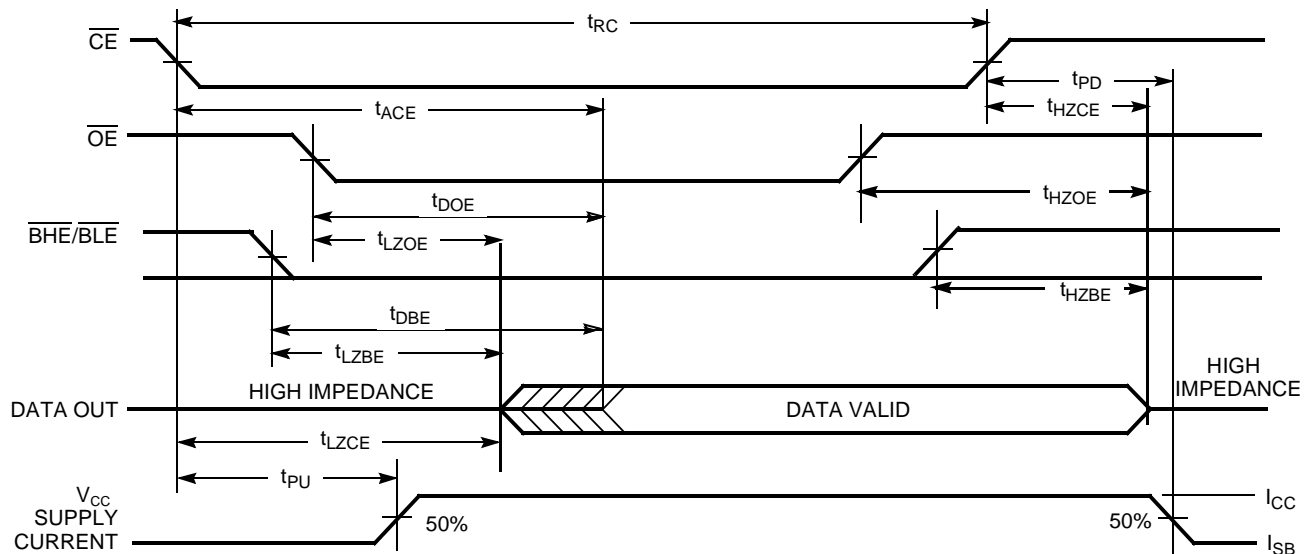
Parameter	Description	70 ns		Unit
		Min.	Max.	
<b>Read Cycle</b>				
t <sub>RC</sub>	Read Cycle Time	70		ns
t <sub>AA</sub>	Address to Data Valid		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		ns
t <sub>ACE</sub>	CE LOW to Data Valid		70	ns
t <sub>DOE</sub>	OE LOW to Data Valid		25	ns
t <sub>LZOE</sub>	OE LOW to Low-Z <sup>[7, 8]</sup>	5		ns
t <sub>HZOE</sub>	OE HIGH to High-Z <sup>[8]</sup>		20	ns
t <sub>LZCE</sub>	CE LOW to Low-Z <sup>[7]</sup>	10		ns
t <sub>HZCE</sub>	CE HIGH to High-Z <sup>[7, 8]</sup>		20	ns
t <sub>PU</sub>	CE LOW to Power-up	0		ns
t <sub>PD</sub>	CE HIGH to Power-down		70	ns
t <sub>DBE</sub>	BHE / BLE LOW to Data Valid		35	ns
t <sub>LZBE</sub>	BHE / BLE LOW to Low-Z	5		ns
t <sub>HZBE</sub>	BHE / BLE HIGH to High-Z		20	ns
<b>Write Cycle<sup>[9, 10]</sup></b>				
t <sub>WC</sub>	Write Cycle Time	70		ns

**Notes:**

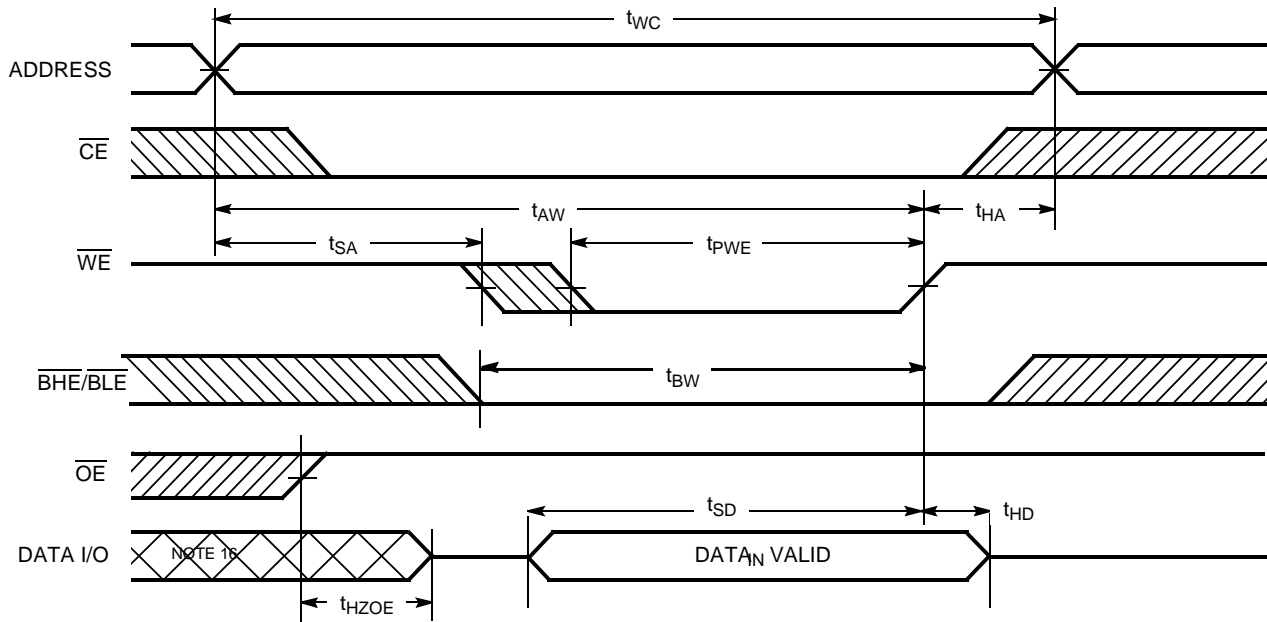
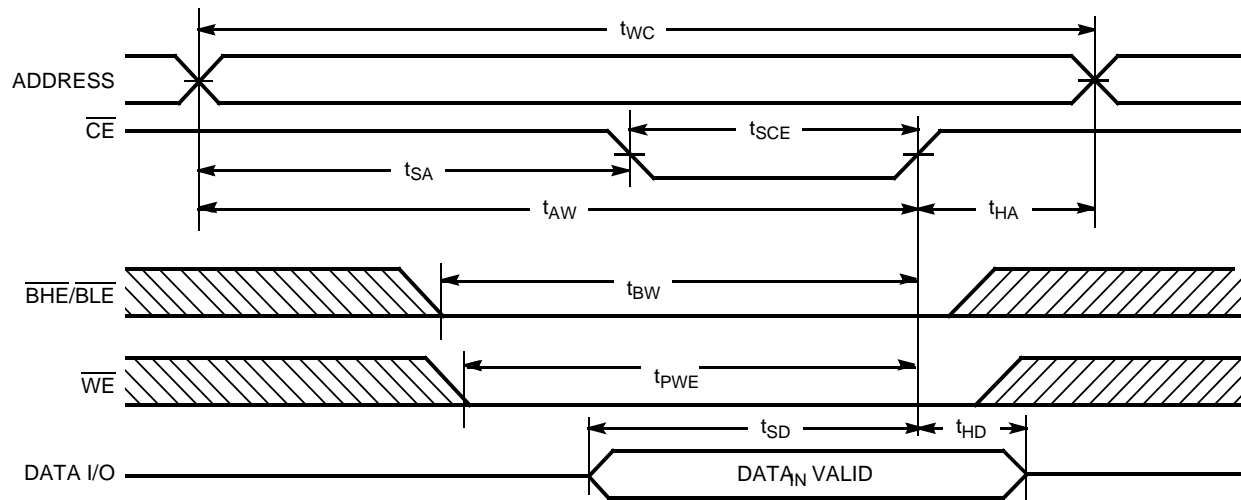
- Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 10 μs or stable V<sub>CC(min.)</sub> ≥ 10 μs.
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to V<sub>CC(typ.)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

**Switching Characteristics** Over the Operating Range (continued)<sup>[6]</sup>

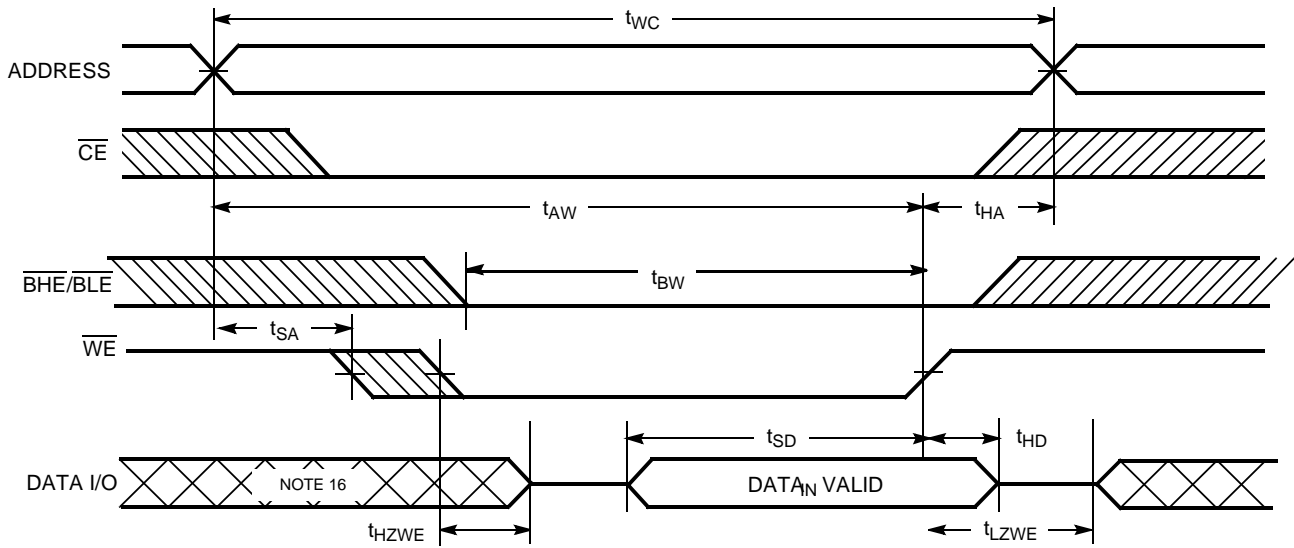
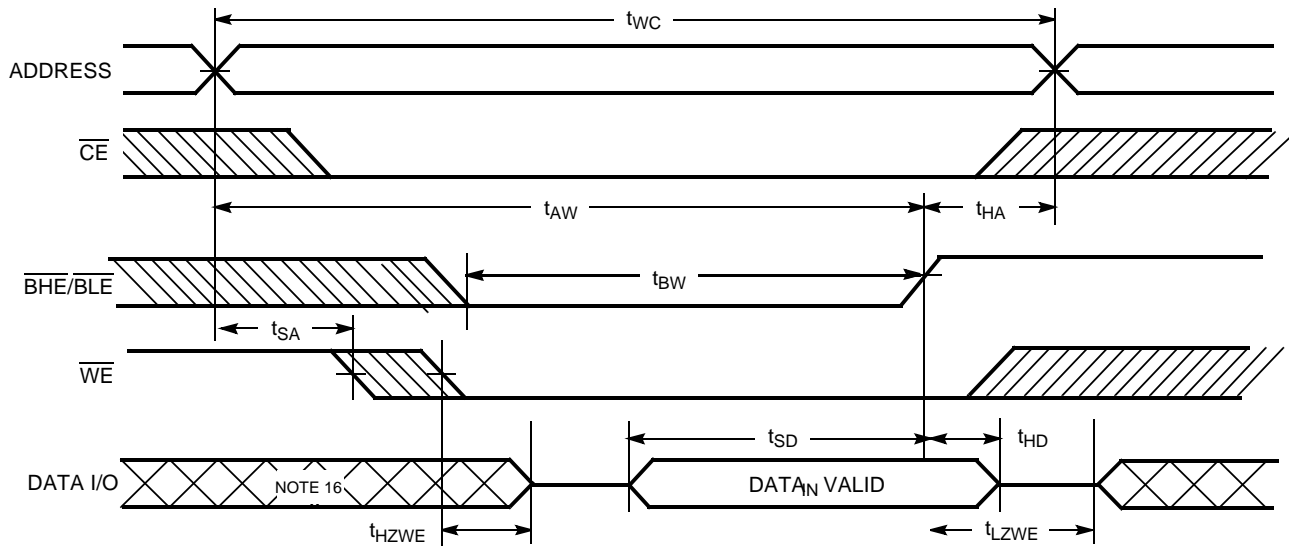
Parameter	Description	70 ns		Unit
		Min.	Max.	
$t_{SCE}$	CE LOW to Write End	60		ns
$t_{AW}$	Address Set-up to Write End	60		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-up to Write Start	0		ns
$t_{PWE}$	WE Pulse Width	40		ns
$t_{BW}$	BHE / BLE Pulse Width	60		ns
$t_{SD}$	Data Set-up to Write End	30		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{HZWE}$	WE LOW to High-Z <sup>[7, 8]</sup>		25	ns
$t_{LZWE}$	WE HIGH to Low-Z <sup>[7]</sup>	10		ns

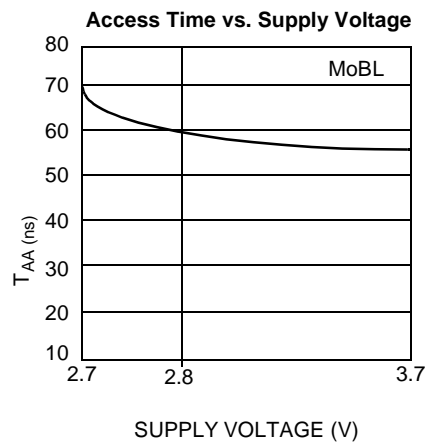
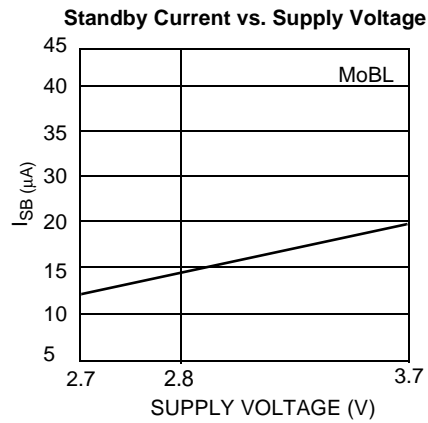
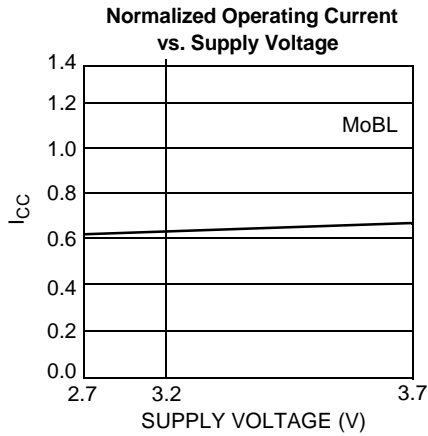
**Switching Waveforms**
**Read Cycle No. 1** <sup>[11, 12]</sup>

**Read Cycle No. 2** <sup>[12, 13]</sup>

**Notes:**

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** <sup>[9, 14, 15]</sup>

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[9, 14, 15]</sup>

**Notes:**

14. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[10, 15]</sup>**

**Write Cycle No. 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>**


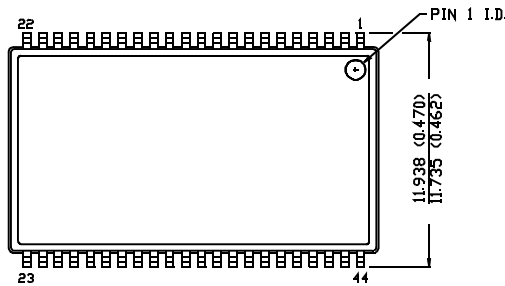
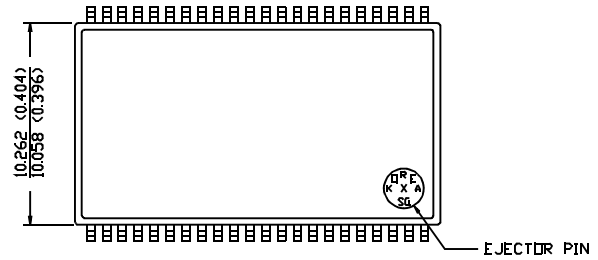
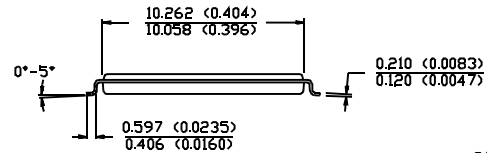
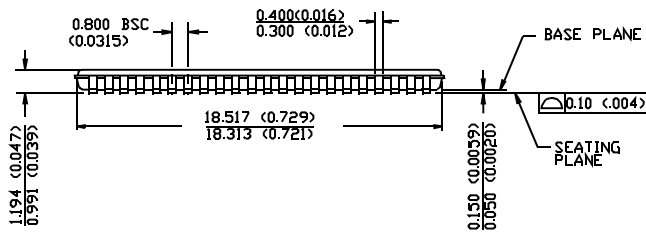
**Typical DC and AC Characteristics**

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out (I/O <sub>0</sub> –I/O <sub>15</sub> )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	H	H	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In (I/O <sub>0</sub> –I/O <sub>15</sub> )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); I/O <sub>8</sub> –I/O <sub>15</sub> in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In (I/O <sub>8</sub> –I/O <sub>15</sub> ); I/O <sub>0</sub> –I/O <sub>7</sub> in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	H	H	High-Z	Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62146VLL-70ZI	Z44	44-pin TSOP II	Industrial

**Package Diagram**
**44-Pin TSOP II Z44**

 DIMENSION IN MM (INCH)  
 MAX  
 MIN

**TOP VIEW**

**BOTTOM VIEW**


51-85087-A

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Document Title: CY62146V MoBL<sup>®</sup> 4M (256K x 16) Static RAM  
Document Number: 38-05159

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109963	10/02/01	SZV	Change from Spec number: 38-00647 to 38-05159
*A	116594	09/04/02	GBI	Added footnote 1. Deleted fBGA package; replacement fBGA package is available in CY62146CV30.



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