



32K x 16 Static RAM

Features

- **High speed**
— $t_{AA} = 12, 15 \text{ ns}$
- **CMOS for optimum speed/power**
- **Low active power**
— 825 mW (max.)
- **Low CMOS standby power (L version only)**
— 2.75 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II and 400-mil SOJ**

Functional Description

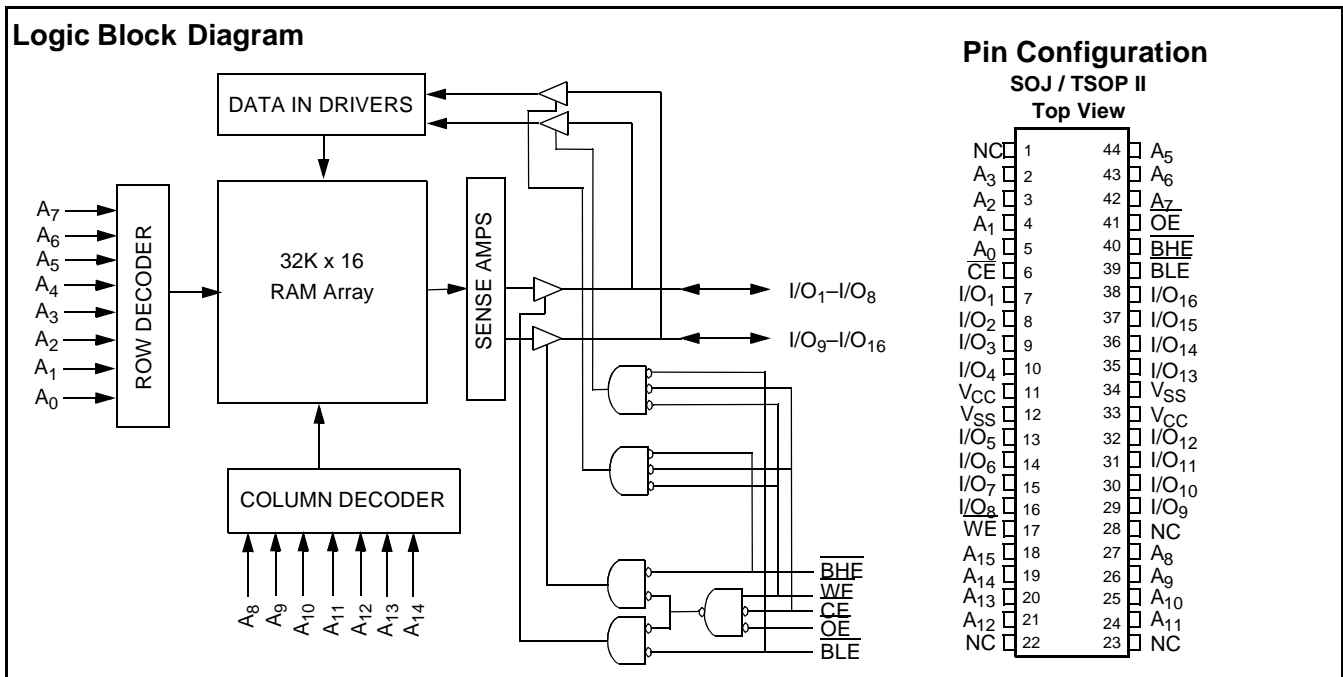
The CY7C1020B is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled ($\overline{BHE}, \overline{BLE}$ HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1020B is available in standard 44-pin TSOP Type II and 400-mil-wide SOJ packages.



Selection Guide

		7C1020B-12	7C1020B-15
Maximum Access Time (ns)	Commercial	12	15
Maximum Operating Current (mA)	Commercial	140	130
Maximum CMOS Standby Current (mA)	Commercial	3	3
	L	0.5	0.5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC}+0.5V
 DC Input Voltage^[1]..... -0.5V to V_{CC}+0.5V

Current into Outputs (LOW) 20 mA
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature ^[2]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

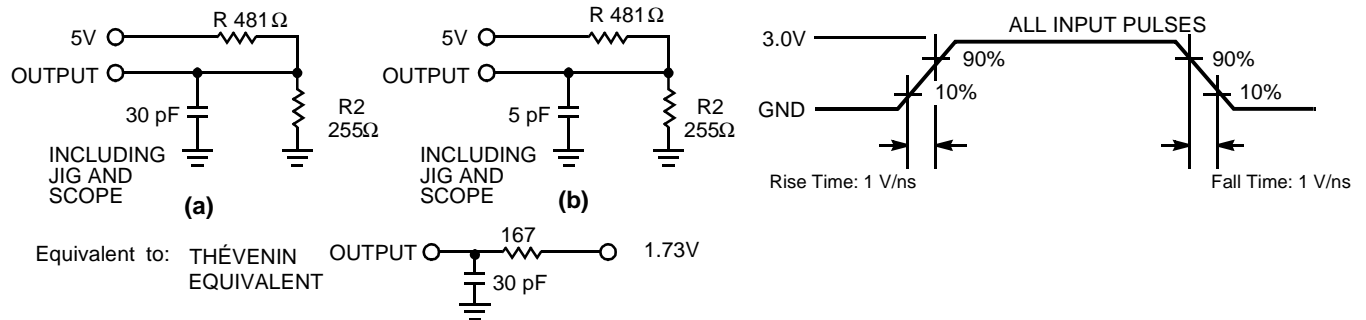
Parameter	Description	Test Conditions	7C1020B-12		7C1020B-15		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V _{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1	+1	-1	+1	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		140		130	mA
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		20		20	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		3		3	mA
			L	0.5		0.5	mA

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the case temperature.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms

Note:

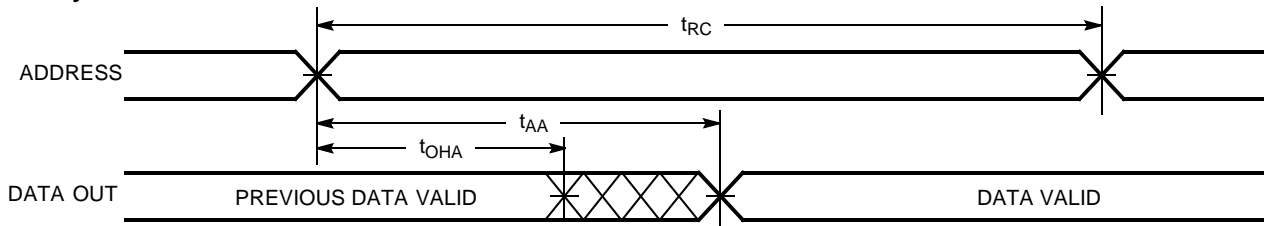
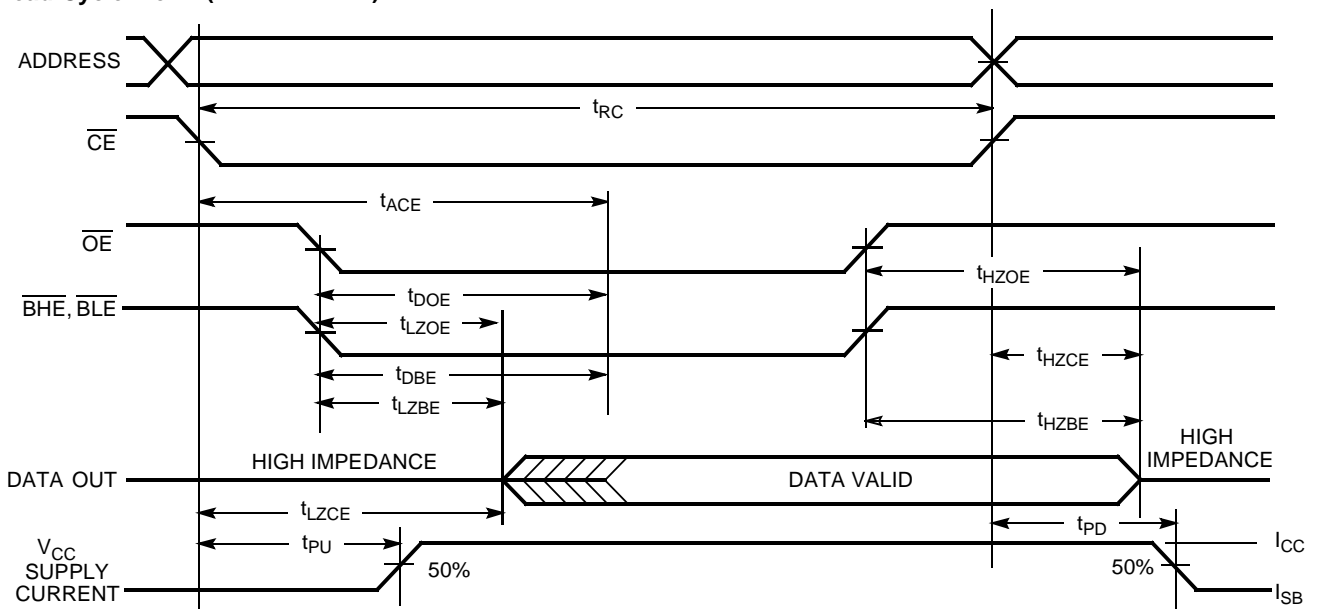
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

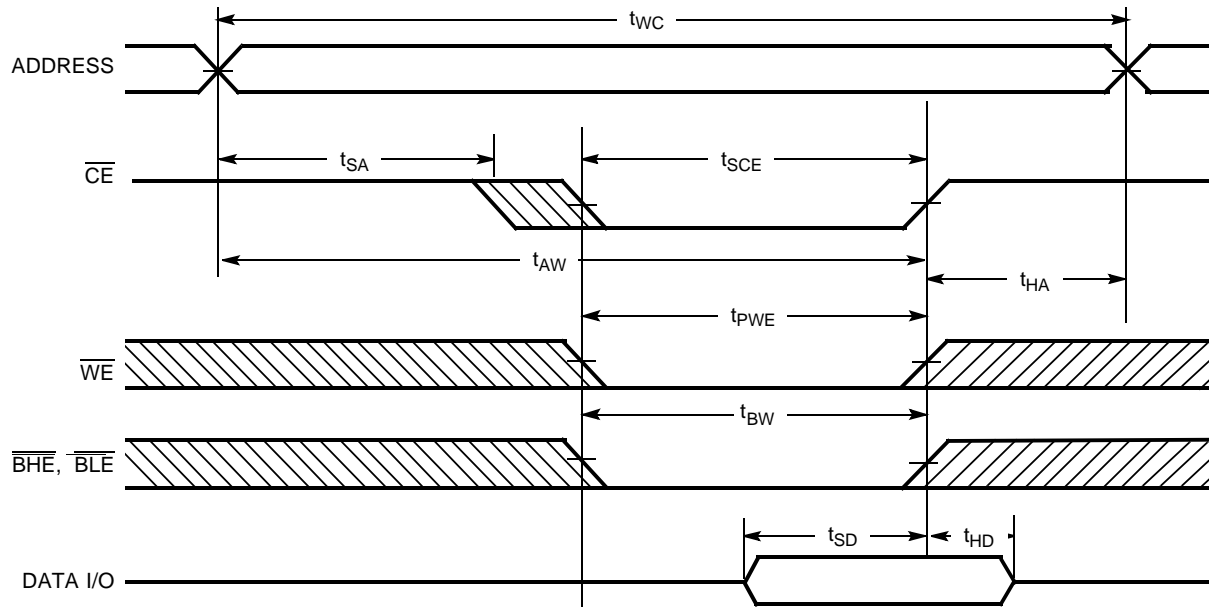
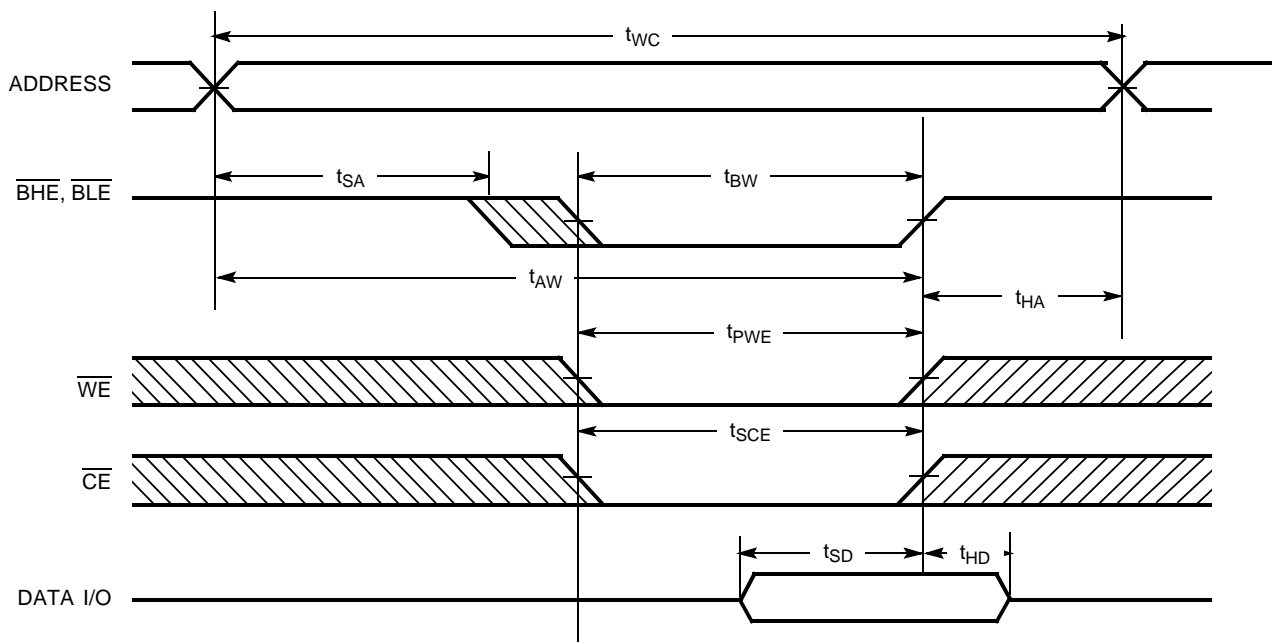
Parameter	Description	7C1020B-12		7C1020B-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	0		0		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	3		3		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		6		7	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		12		15	ns
t_{DBE}	Byte Enable to Data Valid		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		ns
t_{HZBE}	Byte Disable to High Z		6		7	ns
Write Cycle^[8]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	9		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		6		7	ns
t_{BW}	Byte Enable to End of Write	8		9		ns

Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

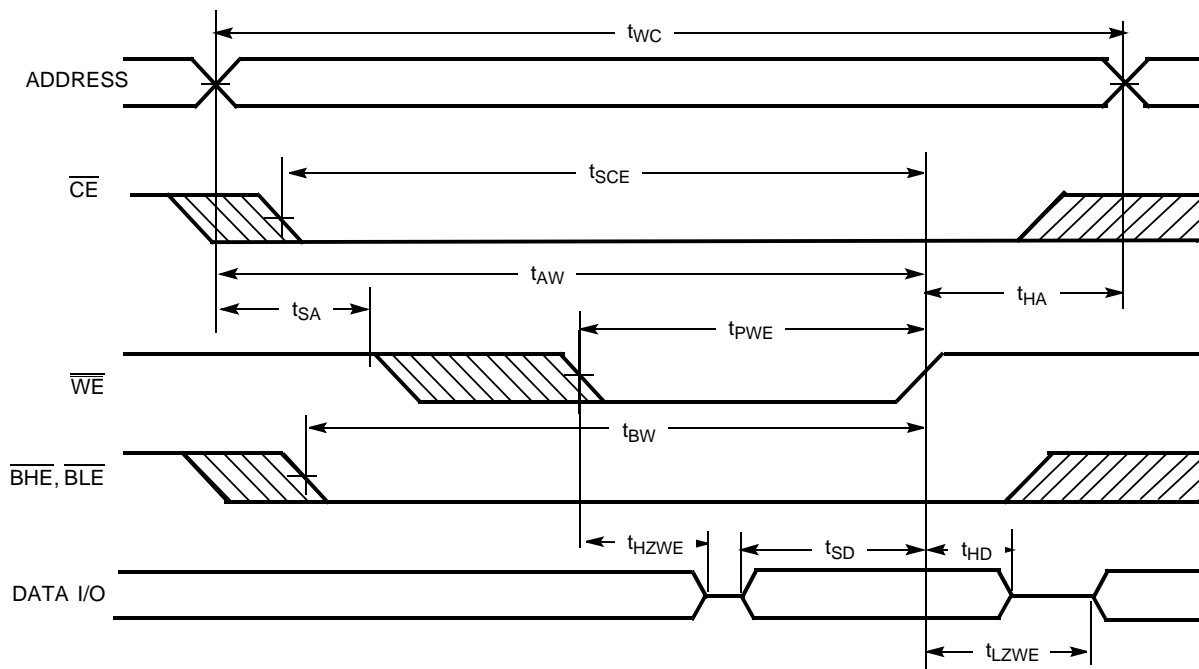
Switching Waveforms
Read Cycle No. 1^[9, 10]

Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]

Notes:

9. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
10. \overline{WE} is HIGH for read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) ^[12, 13]

Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

Notes:

12. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

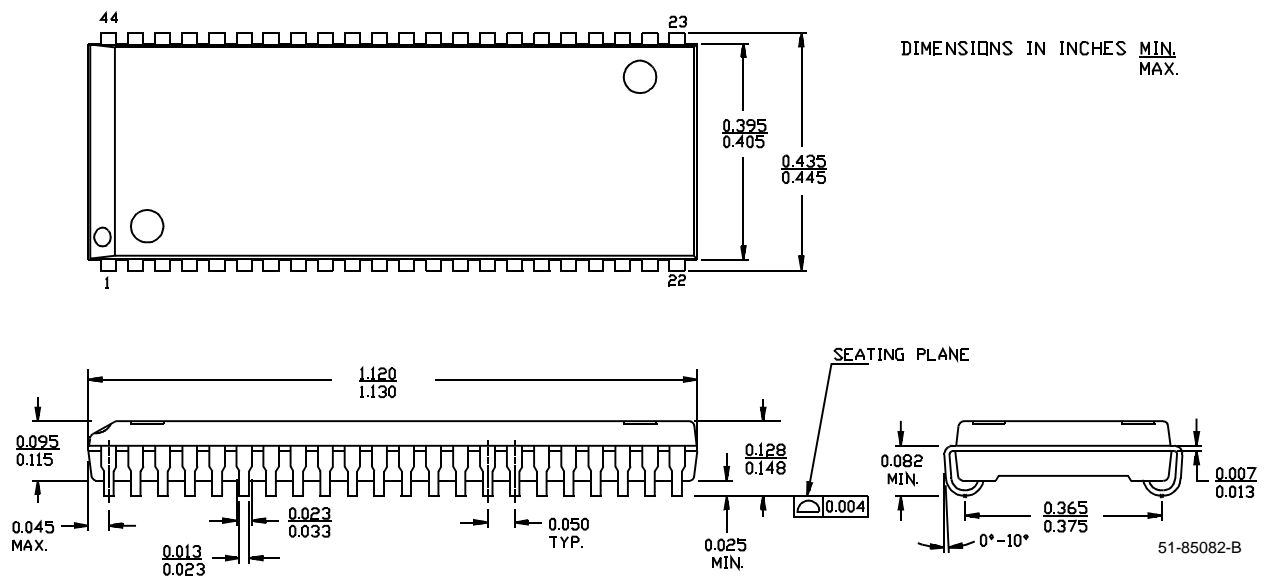
Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled) \overline{OE} LOW

Truth Table

CE	OE	WE	BLE	BHE	I/O ₁ -I/O ₈	I/O ₉ -I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

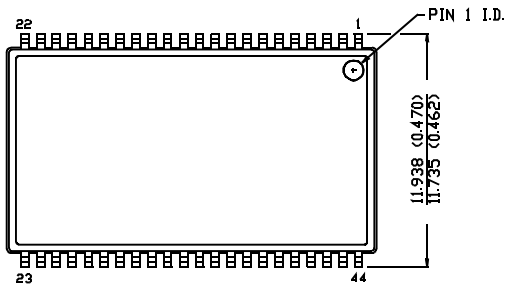
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1020B-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020BL-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020B-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020BL-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1020B-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020BL-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020B-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020BL-15ZC	Z44	44-Lead TSOP Type II	Commercial

Package Diagrams
44-Lead (400-Mil) Molded SOJ V34


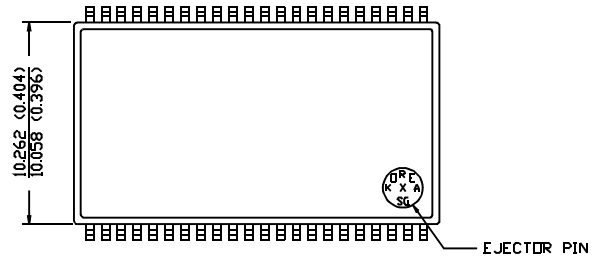
Package Diagrams (continued)

44-Pin TSOP II Z44

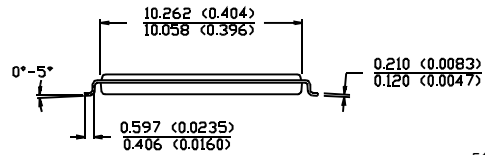
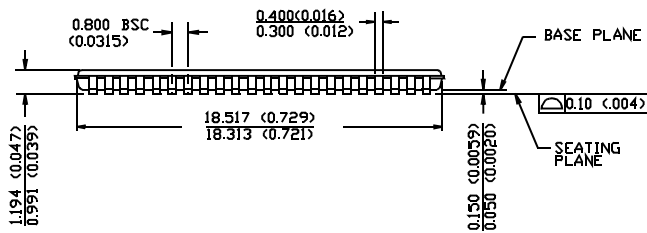
DIMENSION IN MM (INCH)
MAX
MIN.



TOP VIEW



BOTTOM VIEW



51-85087-A

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REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	115439	05/09/02	DSG	New Data Sheet
*A	116869	08/21/02	DFP	Added L-Power Specifications.



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