



1M x 4 Static RAM

Features

- High speed
  - $t_{AA} = 12 \text{ ns}$
- Low active power
  - 935 mW (max.)
- Low CMOS standby power (L version)
  - 2.75 mW (max.)
- 2.0V Data Retention (400  $\mu\text{W}$  at 2.0V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features

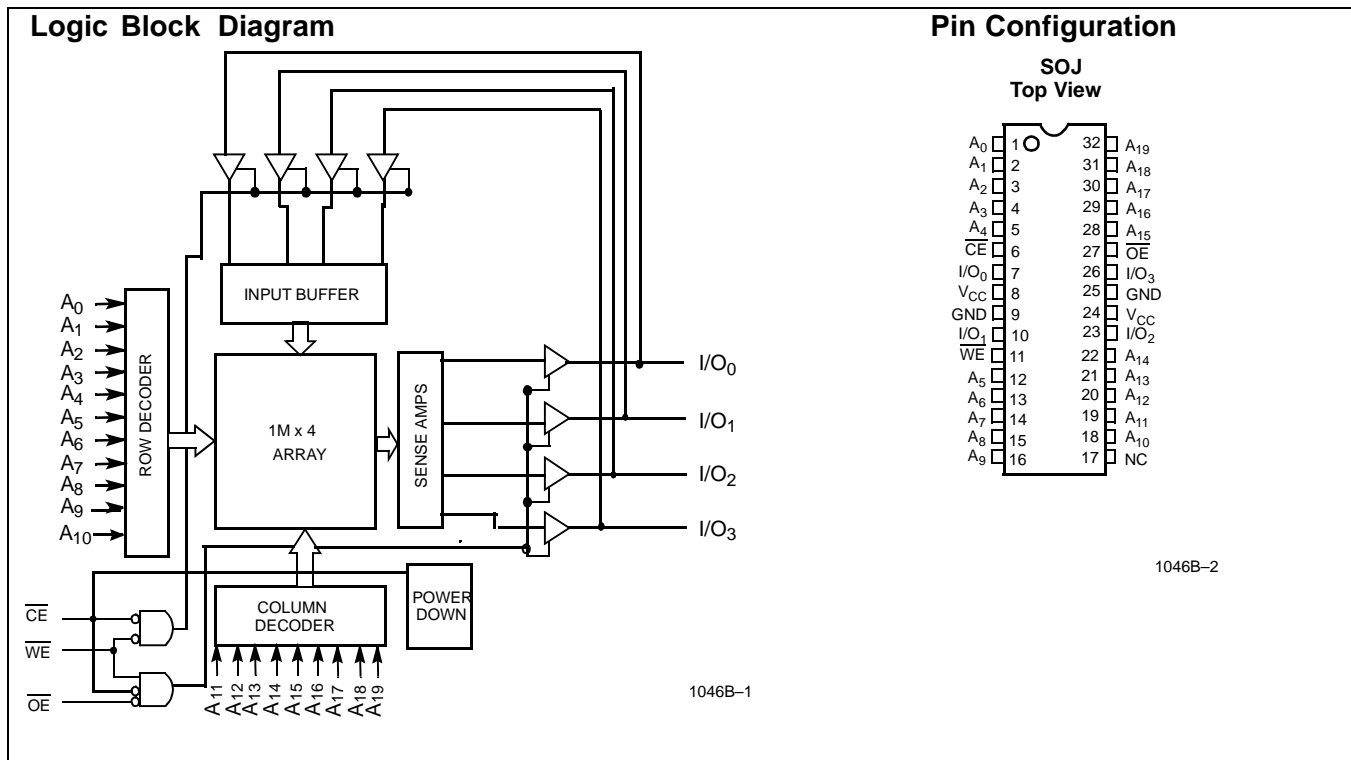
Functional Description

The CY7C1046B is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the four I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{19}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_3$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1046B is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.



Selection Guide

	7C1046B-12	7C1046B-15	7C1046B-20
Maximum Access Time (ns)	12	15	20
Maximum Operating Current (mA)	170	150	130
Maximum CMOS Standby Current (mA)	Com'l	8	8
	L version	0.5	0.5

Shaded areas contain advance information.

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	4.5V–5.5V

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C1046B-12		7C1046B-15		7C1046B-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$		170		150		130	mA
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		20		20		20	mA
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V, f = 0$	Com'l	8		8		8	mA
			L version	0.5		0.5		0.5	

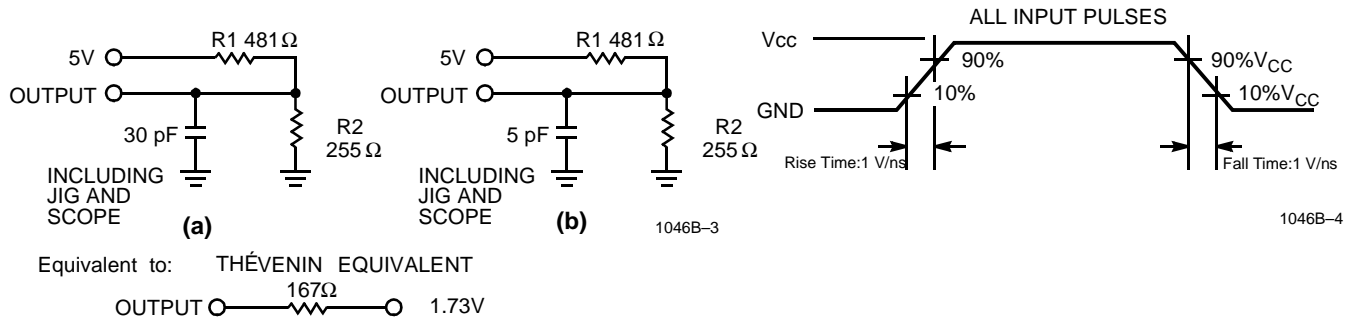
Shaded areas contain advance information.

### Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 5.0V$	6	pF
$C_{OUT}$	I/O Capacitance		6	pF

**Note:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "Instant On" case temperature.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**

**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

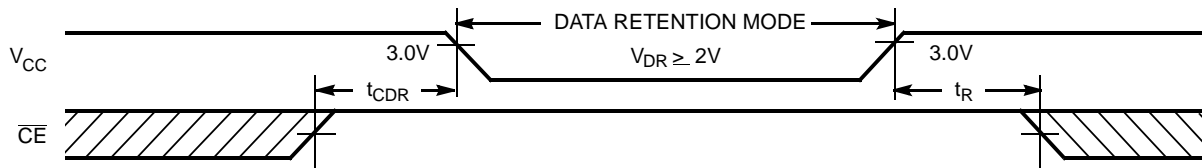
Parameter	Description	7C1046B-12		7C1046B-15		7C1046B-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{\text{power}}$	$V_{\text{CC}}$ (typical) to the first access <sup>[5]</sup>	1		1		1		$\mu\text{s}$
$t_{\text{RC}}$	Read Cycle Time	12		15		20		ns
$t_{\text{AA}}$	Address to Data Valid		12		15		20	ns
$t_{\text{OHA}}$	Data Hold from Address Change	3		3		3		ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to Data Valid		12		15		20	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to Data Valid		6		7		8	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z <sup>[7]</sup>	0		0		0		ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		ns
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to Power-Down		12		15		20	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>								
$t_{\text{WC}}$	Write Cycle Time	12		15		20		ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to Write End	8		10		15		ns
$t_{\text{AW}}$	Address Set-Up to Write End	8		10		15		ns
$t_{\text{HA}}$	Address Hold from Write End	0		0		0		ns
$t_{\text{SA}}$	Address Set-Up to Write Start	0		0		0		ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ Pulse Width	8		10		12		ns
$t_{\text{SD}}$	Data Set-Up to Write End	6		8		10		ns
$t_{\text{HD}}$	Data Hold from Write End	0		0		0		ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns

**Notes:**

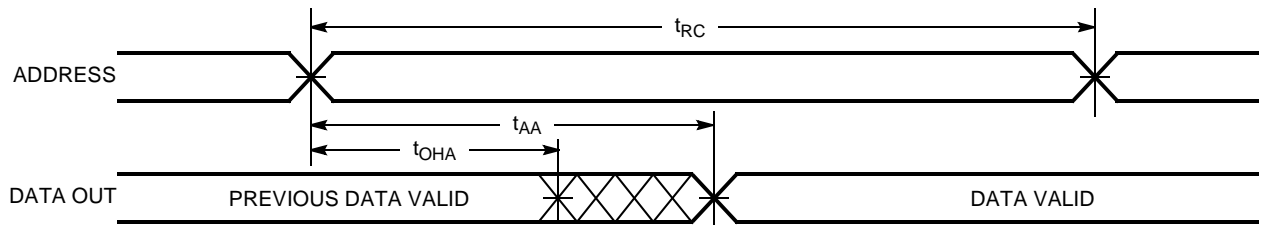
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally.  $t_{\text{power}}$  time has to be provided initially before a read/write operation is started.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Data Retention Characteristics** Over the Operating Range

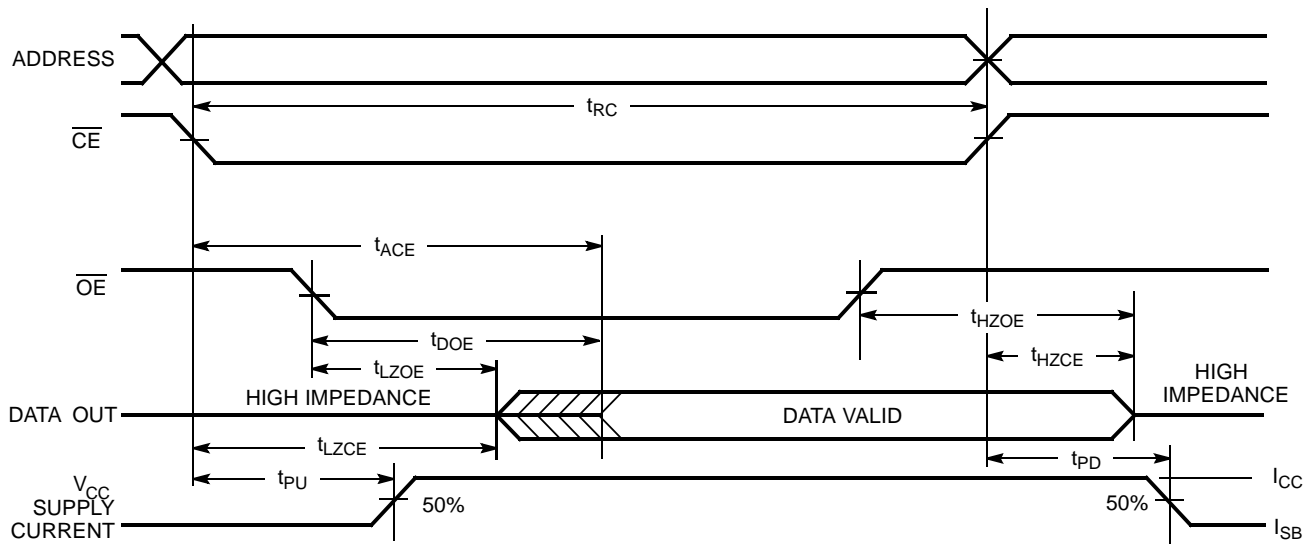
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l		200	$\mu$ A
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0V,$ $CE \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R$	Operation Recovery Time		200		$\mu$ s

**Data Retention Waveform**


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**Switching Waveforms**
**Read Cycle No. 1<sup>[11, 12]</sup>**


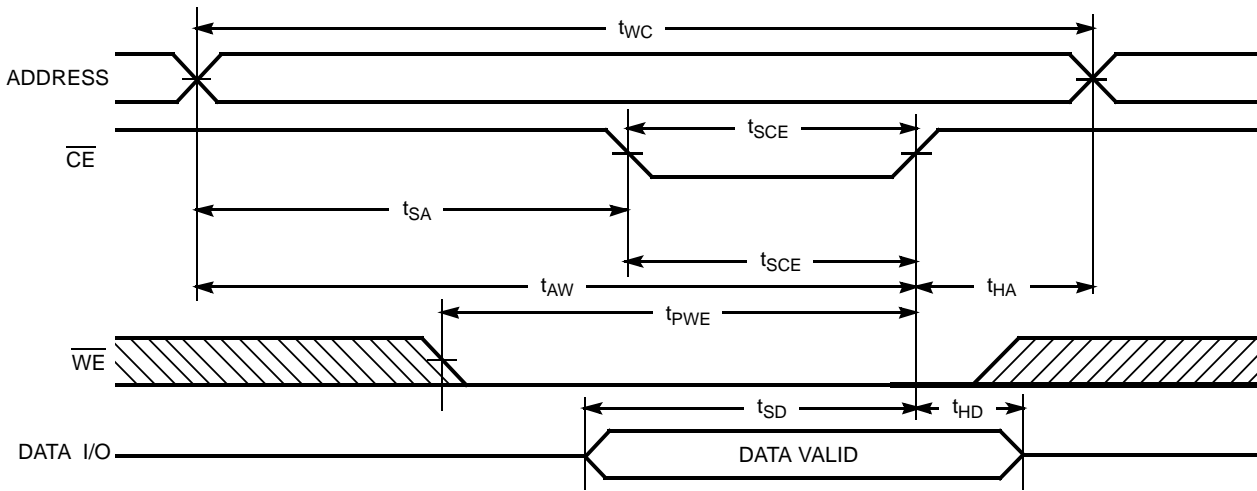
1046B-6

**Read Cycle No. 2 (OE Controlled)<sup>[12, 13]</sup>**


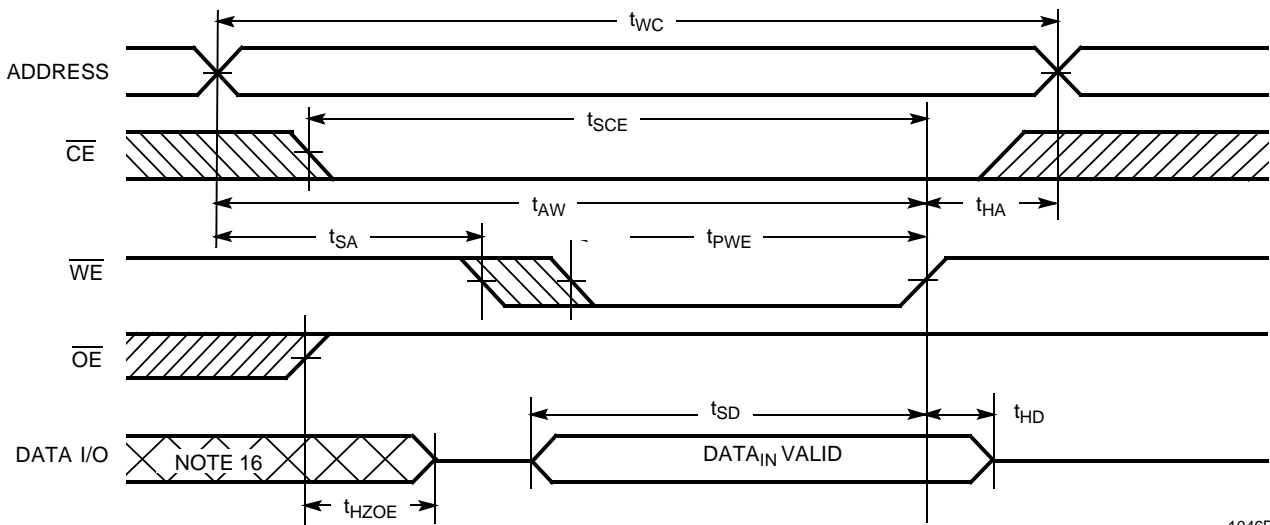
1046B-7

**Notes:**

10. No input may exceed  $V_{CC} + 0.5V$ .
11. Device is continuously selected.  $OE, CE = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[14, 15]</sup>**


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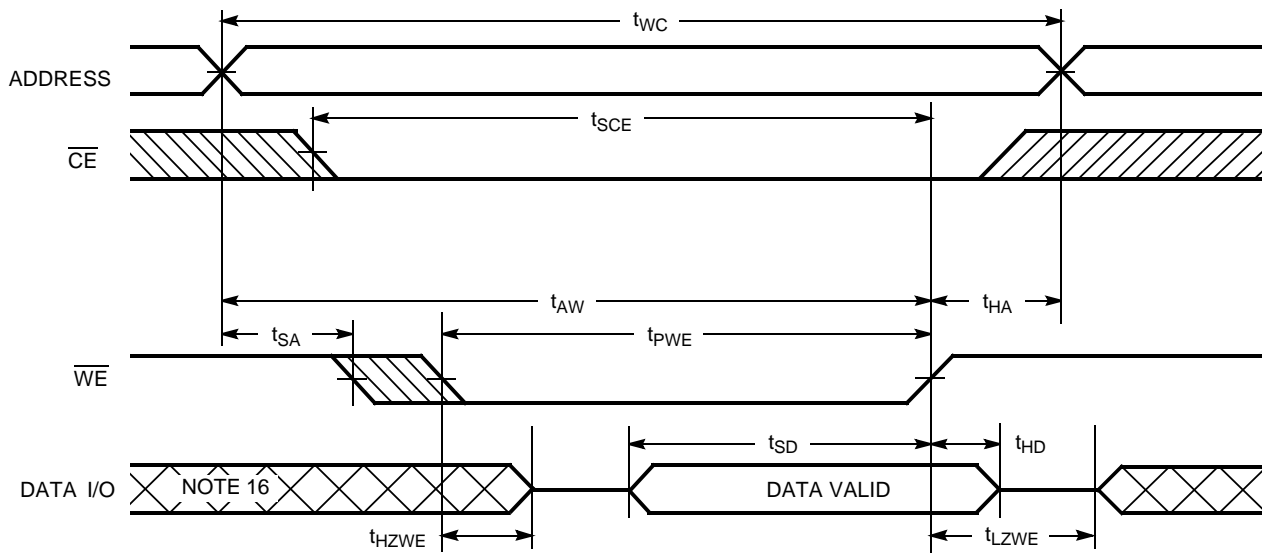
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[14, 15]</sup>**


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**Notes:**

14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[15]</sup>**


1046B-10

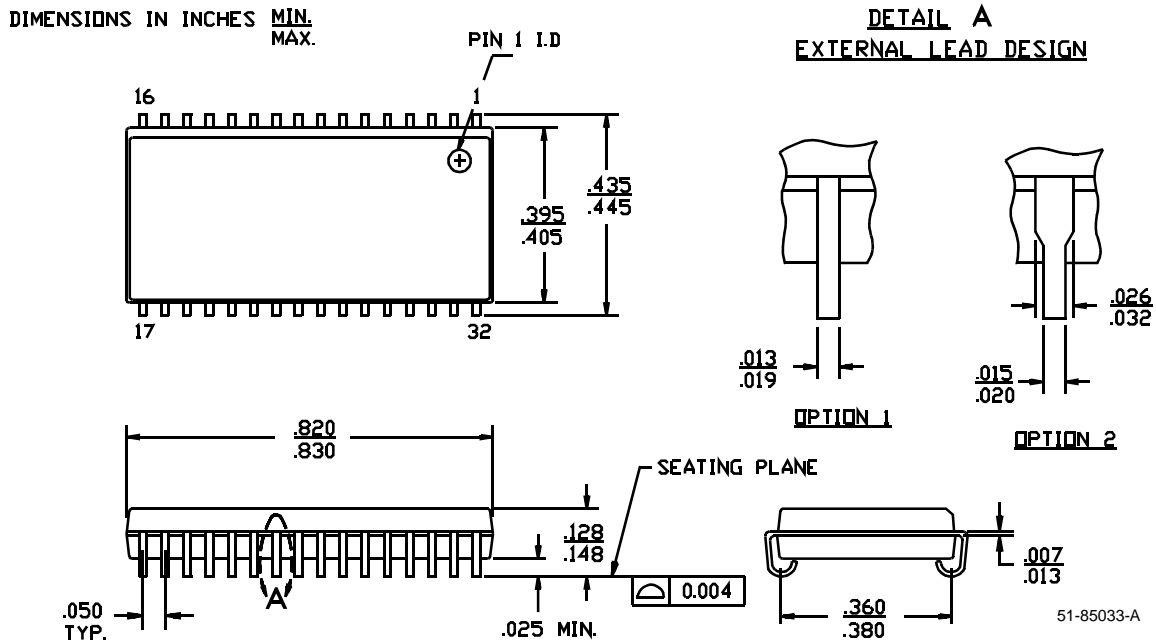
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1046B-12VC	V33	32-Lead (400-Mil) Molded SOJ	Commercial
15	CY7C1046B-15VC	V33	32-Lead (400-Mil) Molded SOJ	
20	CY7C1046B-20VC	V33	32-Lead (400-Mil) Molded SOJ	
12	CY7C1046BL-12VC	V33	32-Lead (400-Mil) Molded SOJ	
15	CY7C1046BL-15VC	V33	32-Lead (400-Mil) Molded SOJ	
20	CY7C1046BL-20VC	V33	32-Lead (400-Mil) Molded SOJ	

Shaded areas contain advance information.

Package Diagram

32-Lead (400-Mil) Molded SOJ V33





<b>Document Title: CY7C1046B 1M x 4 Static RAM</b> <b>Document Number: 38-05144</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	109888	09/22/01	SZV	Change from Spec number: 38-00948 to 38-05144



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