

# 8251/Am9551

Programmable Communication Interface

iAPX86 Family

MILITARY INFORMATION

## DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun, and framing errors detected
- Half- or full-duplex signaling
- Character length of 5, 6, 7, or 8 bits
- Internal or external synchronization
- Odd parity, even parity, or no parity bit
- Modem interface controlled by processor
  - Programmable Sync pattern
  - Fully TTL-compatible logic levels

## GENERAL DESCRIPTION

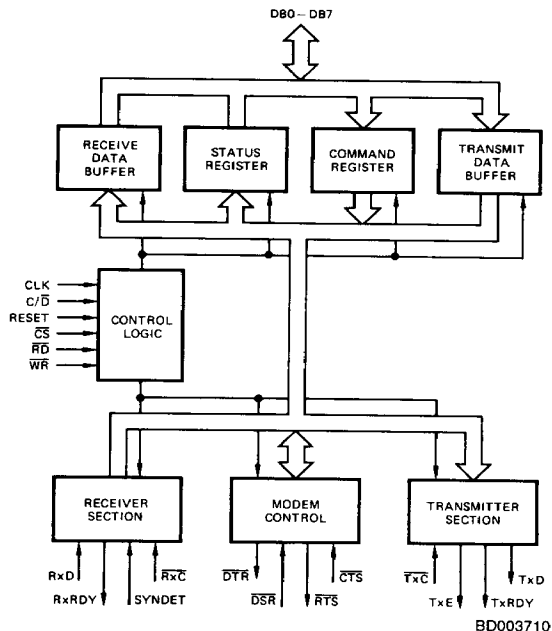
The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream.

Simultaneously, serial data can be received, converted to parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full-duplex mode.

Data, control, operation, and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/Am9551 to service a wide range of communication disciplines and applications.

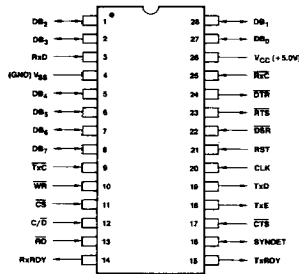
## BLOCK DIAGRAM



Publication # 09233  
Rev. A  
Amendment /0  
Issue Date: November 1987

## CONNECTION DIAGRAM Top View

### DIPs



CD005482

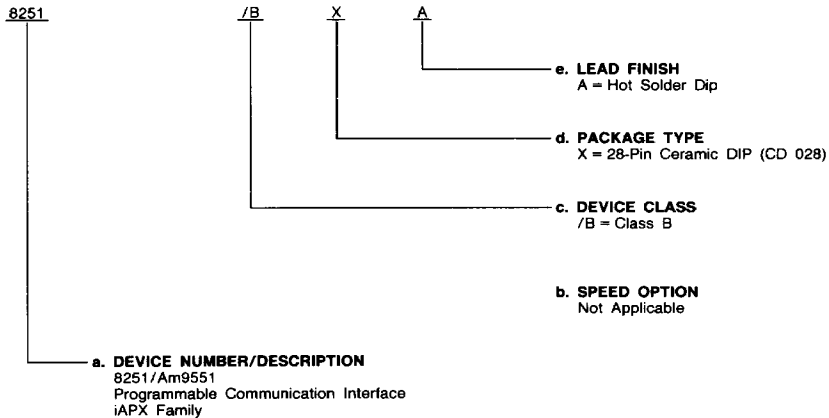
Note: Pin 1 is marked for orientation.

## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
8251	/BXA
AM9551	

### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... -65°C to +150°C  
 V<sub>CC</sub> with Respect to V<sub>SS</sub> ..... -0.5 to +7.0 V  
 All Signal Voltages  
 with Respect to V<sub>SS</sub> ..... -0.5 V to +7.0 V  
 Power Dissipation ..... 1.0 W

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

**OPERATING RANGES**

Military (M) Devices  
 Temperature (T<sub>C</sub>) ..... -55 to +125°C  
 Supply Voltage (V<sub>CC</sub>) ..... 5 V ± 10%

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

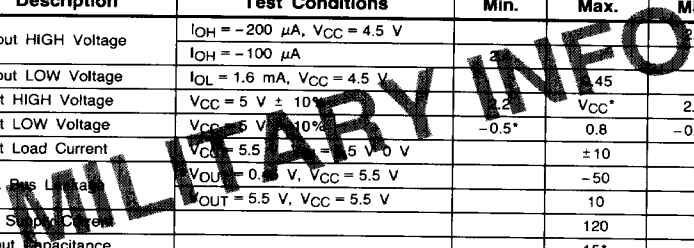
**DC CHARACTERISTICS**

over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	8251		Am9551		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -200 μA, V <sub>CC</sub> = 4.5 V I <sub>OH</sub> = -100 μA	2.4				V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 1.6 mA, V <sub>CC</sub> = 4.5 V		0.45		0.45	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 5 V ± 10%	2.2	V <sub>CC</sub> *	2.2	V <sub>CC</sub> *	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 5 V ± 10%	-0.5*	0.8	-0.5*	0.8	V
I <sub>LI</sub>	Input Load Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5 V = 0 V		±10		±10	μA
I <sub>DL</sub>	Data Bus Leakage	V <sub>OUT</sub> = 0 V, V <sub>CC</sub> = 5.5 V V <sub>OUT</sub> = 5.5 V, V <sub>CC</sub> = 5.5 V		-50		-50	μA
I <sub>CC</sub>	V <sub>CC</sub> Supply Current			120		120	mA
C <sub>O</sub> †	Output Capacitance			15*		15*	pF
C <sub>I</sub> †	Input Capacitance			10*		10*	pF
C <sub>I/O</sub> †	I/O Capacitance	fc = 1.0 MHz, Inputs = 0 V		20*		20*	pF

\* Guaranteed by design; not tested.  
 † Not included in Group A tests.

Notes: 1. I<sub>CC</sub> is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.



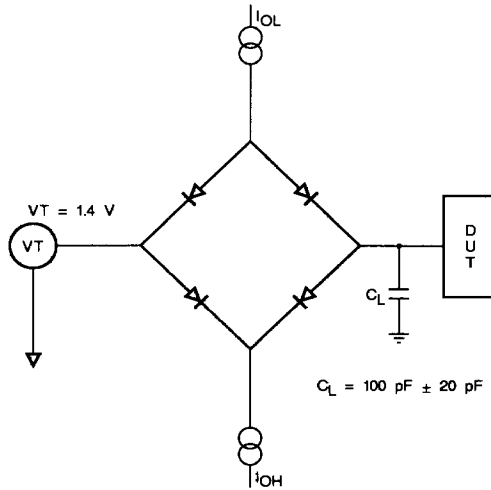
## SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF006490

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

## SWITCHING TEST CIRCUIT



TC003851

This test circuit is the dynamic load of a Teradyne J941.

**SWITCHING CHARACTERISTICS** over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description	8251		Am9551		Unit	
		Min.	Max.	Min.	Max.		
t <sub>AR</sub>	CS, C/D Stable to READ LOW Setup Time	50		50		ns	
t <sub>AW</sub>	CS, C/D Stable to WRITE LOW Setup Time	20		20		ns	
t <sub>CR</sub>	DSR, CTS to READ LOW Setup Time		16		16	t <sub>CY</sub>	
t <sub>CY</sub>	Clock Period	0.420	1.35	0.380	1.35	μs	
t <sub>DF</sub>	READ HIGH to Data Bus Off Delay	25	200	25	200	ns	
t <sub>DTx</sub>	TxC LOW to TxD Delay		1.0		1.0	μs	
t <sub>DW</sub>	Data to WRITE HIGH Setup Time	200		150		ns	
t <sub>ES</sub>	External SYNDET to RxC LOW Setup Time	16		16		t <sub>CY</sub>	
t <sub>HRx</sub>	Sampling Pulse to Rx Data Hold Time (Note 5)	2.0		2.0		μs	
t <sub>IS</sub>	Data Bit (Center) to Internal SYNDET Delay		30		30	t <sub>CY</sub>	
t <sub>φW</sub>	Clock Pulse Width	220	0.6t <sub>CY</sub>	175	0.6t <sub>CY</sub>	ns	
t <sub>RA</sub>	READ HIGH to CS, C/D Hold Time	5.0		5.0		ns	
t <sub>RD</sub>	READ LOW to Data Bus On Delay		350		250	ns	
t <sub>RPD</sub>	Receiver Clock HIGH Time	1x Baud Rate		15		t <sub>CY</sub>	
		16x & 64x Baud Rate	3	3			
t <sub>RPW</sub>	Receiver Clock LOW Time	1x Baud Rate		12		t <sub>CY</sub>	
		16x & 64x Baud Rate	1	1			
t <sub>RR</sub>	READ Pulse Width	430		380		ns	
t <sub>RV</sub>	Time Between WRITE Pulses During Initialization (Note 1)	6.0		6.0		t <sub>CY</sub>	
t <sub>Rx</sub>	Data Bit (Center) to RxRDY Delay		20		20	t <sub>CY</sub>	
t <sub>SRx</sub>	Rx Data to Sampling Pulse Setup Time (Note 5)	2.0		2.0		μs	
t <sub>TPD</sub>	Transmitter Clock HIGH Time	1x Baud Rate		15		t <sub>CY</sub>	
		16x & 64x Baud Rate	3	3			
t <sub>TPW</sub>	Transmitter Clock LOW Time	1x Baud Rate		12		t <sub>CY</sub>	
		16x & 64x Baud Rate	1	1			
t <sub>TX</sub>	Data Bit (Center) to TxD Delay		16		16	t <sub>CY</sub>	
t <sub>TxE</sub>	Data Bit (Center) to TxEMPTY Delay		16		16	t <sub>CY</sub>	
t <sub>WA</sub>	WRITE HIGH to CS, C/D Hold Time	20		20		ns	
t <sub>WC</sub>	WRITE HIGH to TxE, DTR, RTS Delay		16		16	t <sub>CY</sub>	
t <sub>WD</sub>	WRITE HIGH to Data Hold Time	40		40		ns	
t <sub>WW</sub>	WRITE Pulse Width	430		380		ns	
f <sub>Rx</sub>	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	
f <sub>Tx</sub>	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	

- Notes: 1. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND, and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1. t<sub>RV</sub> after internal Reset = 8 \* t<sub>CY</sub>.
2. Reset Pulse Width = 6t<sub>CY</sub> Min.
3. Switching Characteristics parameters are listed in alphabetical order.
4. Clock Rise and Fall times are controlled by the Teradyne J941 tester. Measurement of typical signals generated by the J941 showed t<sub>R</sub> = t<sub>F</sub> = 5 ns.
5. Sampling pulse is internal and not tested; guaranteed by design.