

DCP02 Series

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Miniature, 2W Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- UP TO 89% EFFICIENCY
- THERMAL PROTECTION
- DEVICE-TO-DEVICE SYNCHRONIZATION
- SO-28⁽¹⁾ POWER DENSITY OF 106W/in³ (6.5W/cm³)
- EN55022 CLASS B EMC PERFORMANCE
- UL1950 RECOGNIZED
- JEDEC 14-PIN AND SO-28⁽¹⁾ PACKAGES

APPLICATIONS

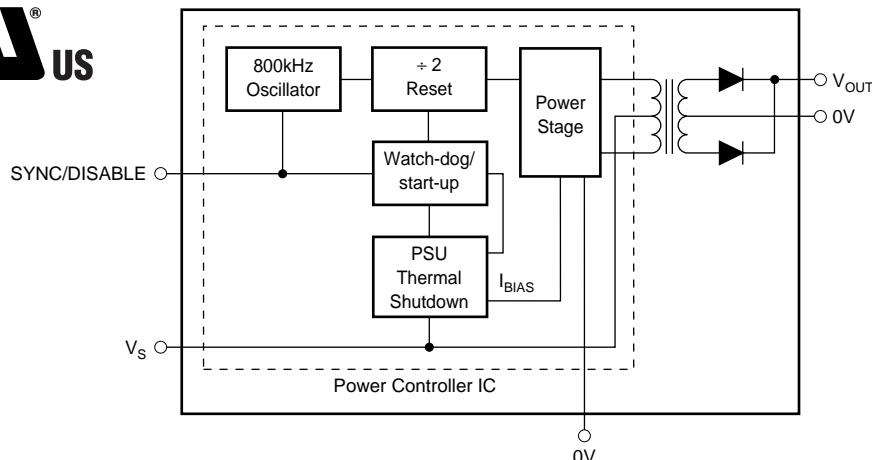
- POINT-OF-USE POWER CONVERSION
- GROUND LOOP ELIMINATION
- DATA ACQUISITION
- INDUSTRIAL CONTROL AND INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The DCP02 series is a family of 2W, unregulated, isolated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCP02 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with power densities of 79W/in³ (4.8W/cm³) for the 14-PDIP, and 106W/in³ (6.5W/cm³) for the SO-28⁽¹⁾. This combination of features and small size makes the DCP02 suitable for a wide range of applications.

NOTE: (1) SO-28 version available January, 2000.



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SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, unless otherwise specified.

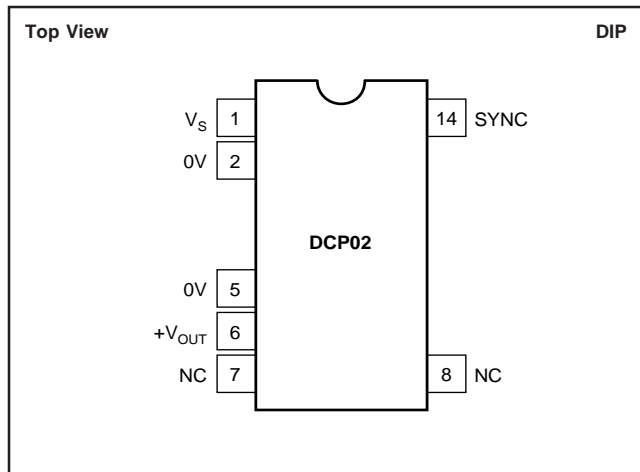
PARAMETER	CONDITIONS	DCP02 SERIES			UNITS
		MIN	TYP	MAX	
OUTPUT Power Ripple	100% Full Load O/P Capacitor = $1\mu\text{F}$, 50% Load		2 20		W mVp-p
INPUT Voltage Range on V_S		-10		10	%
ISOLATION Voltage	1s Flash Test 60s Test, UL1950 ⁽¹⁾	1 1			kVrms kVrms
LINE Regulation			1		%/1% of V_S
SWITCHING/SYNCHRONIZATION Oscillator Frequency (f_{osc}) Sync Input Low Sync Input Current Disable Time Capacitance Loading on Sync Pin	Switching Frequency = $f_{\text{osc}}/2$ $V_{\text{SYNC}} = +2\text{V}$ External	0	800 75 2	0.4	kHz V μA μs pF
RELIABILITY Demonstrated	$T_A = +55^\circ\text{C}$	75			FITS
THERMAL SHUTDOWN IC Temperature at Shutdown Shutdown Current			150 3		$^\circ\text{C}$ mA
TEMPERATURE RANGE Operating		-40		+85	$^\circ\text{C}$

PRODUCT	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			LOAD REGULATION (%)		NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_S			V_{NOM}			10% TO 100% LOAD		I_Q	100% LOAD	C_{ISO}
				75% LOAD ⁽²⁾					0% LOAD		$V_{\text{ISO}} = 750V_{\text{RMS}}$
	MIN	TYP	MAX	MIN	TYP	MAX	TYP	MAX	TYP	TYP	TYP
DCP020503P ⁽³⁾ , U ⁽³⁾	4.5	5	5.5	3.13	3.3	3.46	19	30	18	74	26
DCP020505P, U ⁽⁴⁾	4.5	5	5.5	4.75	5	5.25	14	20	18	80	22
DCP020507P, U ⁽⁴⁾	4.5	5	5.5	6.65	7	7.35	14	25	20	81	30
DCP020509P, U ⁽⁴⁾	4.5	5	5.5	8.55	9	9.45	12	20	23	82	31
DCP020515DP, U ⁽⁴⁾	4.5	5	5.5	± 14.25	± 15	± 15.75	11	20	27	85	24
DCP021205P, U ⁽⁴⁾	10.8	12	13.2	4.75	5	5.25	7	15	14	83	33
DCP021212P	10.8	12	13.2	11.4	12	12.6	7	20	15	87	47
DCP021212DP	10.8	12	13.2	± 11.4	± 12	± 12.6	6	20	16	88	35
DCP021515P	13.5	15	16.5	14.25	15	15.75	6	20	15	88	42
DCP022405P	21.6	24	26.4	4.85	5	5.35	6	10	13	81	33
DCP022405DP	21.6	24	26.4	± 4.75	± 5	± 5.25	6	15	12	80	22
DCP022415DP	21.6	24	26.4	± 14.25	± 15	± 15.75	6	20	16	79	44

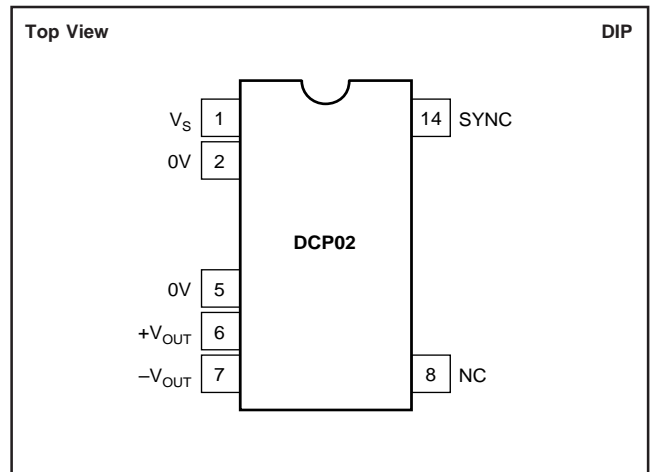
NOTES: (1) During UL1950 recognition tests only. (2) 100% Load Current = $2W/V_{\text{NOM}}$ TYP. (3) DCP020503P and U models available January, 2000. (4) SO-28 version available January, 2000.

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PIN CONFIGURATION (Single-DIP)



PIN CONFIGURATION (Dual-DIP)



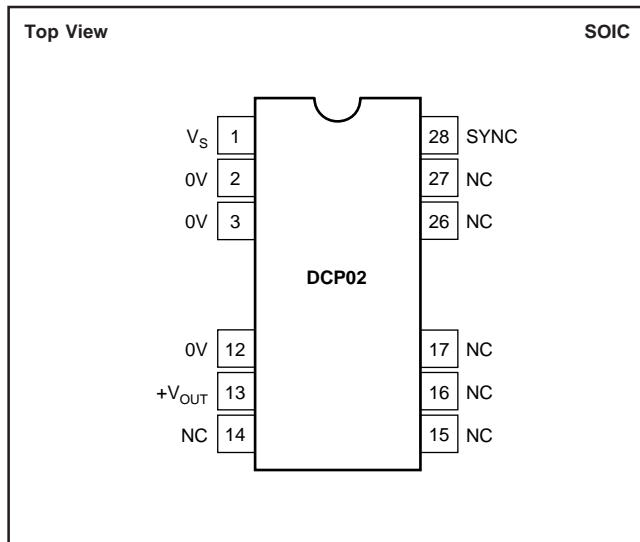
PIN DEFINITION (Single-DIP)

PIN #	PIN NAME	DESCRIPTION
1	V _S	Voltage Input
2	0V	Input Side Common
5	0V	Output Side Common
6	+V _{OUT}	+Voltage Out
7	NC	Not Connected
8	NC	Not Connected
14	SYNC	Synchronization Pin

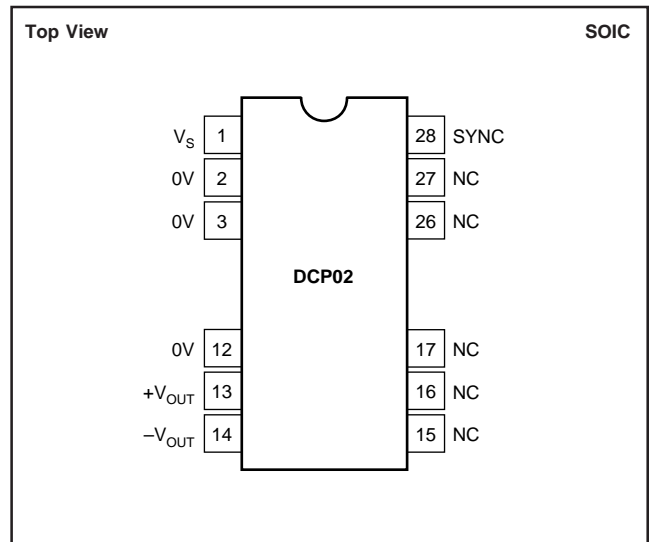
PIN DEFINITION (Dual-DIP)

PIN #	PIN NAME	DESCRIPTION
1	V _S	Voltage Input
2	0V	Input Side Common
5	0V	Output Side Common
6	+V _{OUT}	+Voltage Out
7	-V _{OUT}	-Voltage Out
8	NC	Not Connected
14	SYNC	Synchronization Pin

PIN CONFIGURATION (Single-SOIC)⁽¹⁾



PIN CONFIGURATION (Dual-SOIC)⁽¹⁾



PIN DEFINITION (Single-SOIC)⁽¹⁾

PIN #	PIN NAME	DESCRIPTION
1	V _S	Voltage Input
2	0V	Input Side Common
3	0V	Input Side Common
12	0V	Output Side Common
13	+V _{OUT}	+Voltage Out
14	NC	Not Connected
15	NC	Not Connected
16	NC	Not Connected
17	NC	Not Connected
26	NC	Not Connected
27	NC	Not Connected
28	SYNC	Synchronization Pin

PIN DEFINITION (Dual-SOIC)⁽¹⁾

PIN #	PIN NAME	DESCRIPTION
1	V _S	Voltage Input
2	0V	Input Side Common
3	0V	Input Side Common
12	0V	Output Side Common
13	+V _{OUT}	+Voltage Out
14	-V _{OUT}	-Voltage Out
15	NC	Not Connected
16	NC	Not Connected
17	NC	Not Connected
26	NC	Not Connected
27	NC	Not Connected
28	SYNC	Synchronization Pin

NOTE: (1) SO-28 version available January, 2000.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
5V Input Models	7V
12V Input Models	15V
15V Input Models	18V
24V Input Models	29V
Storage Temperature	-60°C to +125°C
Lead Temperature (soldering, 10s)	270°C

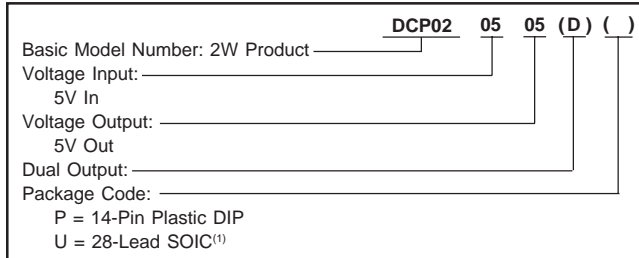


ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION



NOTE: (1) SO-28 version available 1Q00.

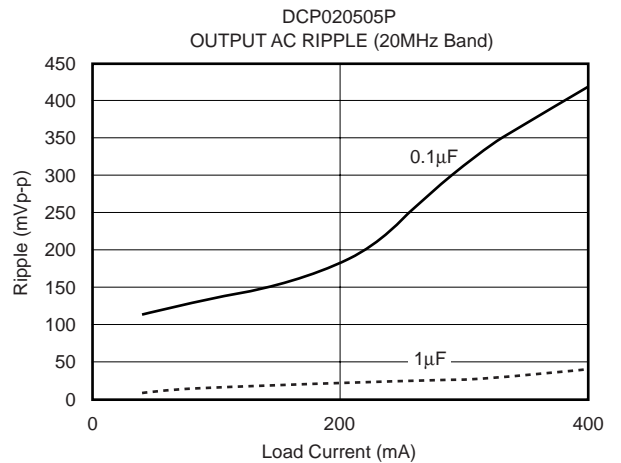
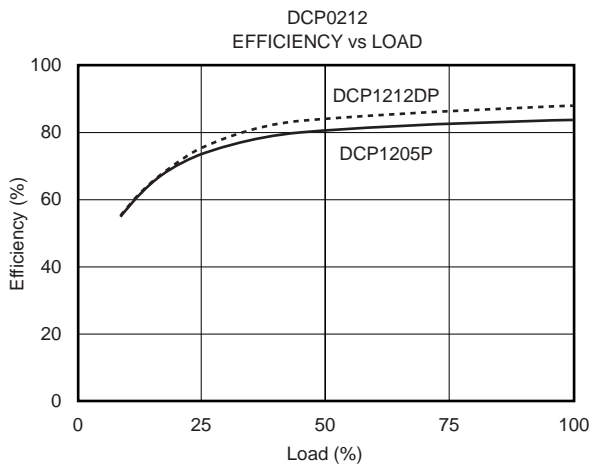
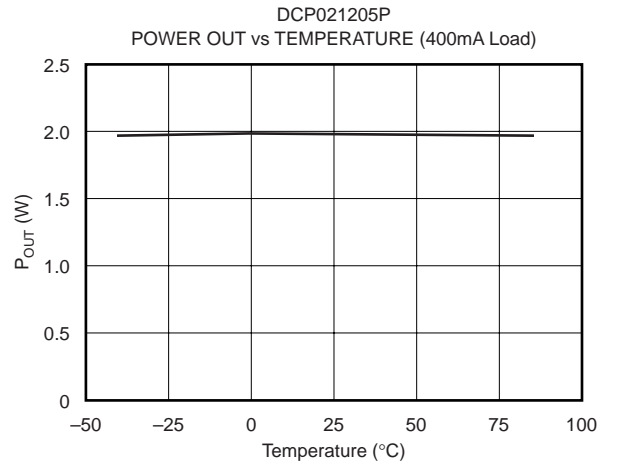
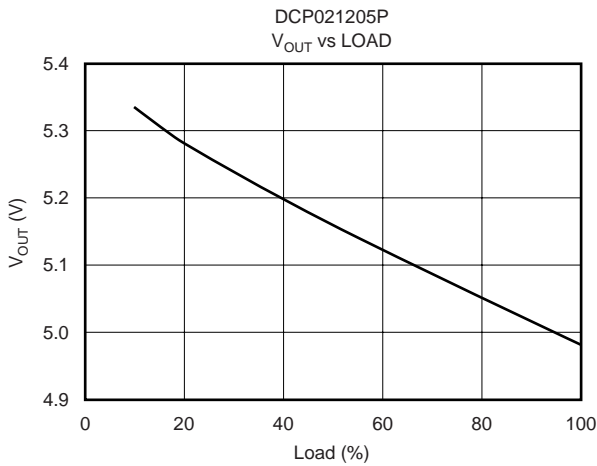
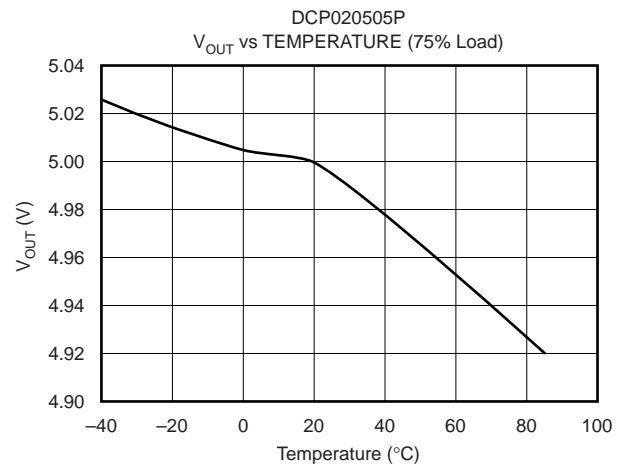
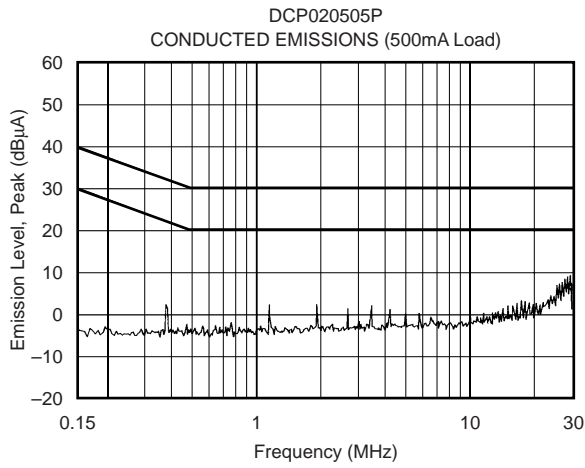
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
Single						
DCP020503P ⁽²⁾	DIP-14	010-1	-40°C to +85°C	DCP020503P	DCP020503P	Rails
DCP020503U ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP020503U	DCP020503U/1K	Tape and Reels
DCP020505P	DIP-14	010-1	-40°C to +85°C	DCP020505P	DCP020505P	Rails
DCP020505U ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP020505U	DCP020505U/1K	Tape and Reels
DCP020507P	DIP-14	010-1	-40°C to +85°C	DCP020507P	DCP020507P	Rails
DCP020507U ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP020507U	DCP020507U/1K	Tape and Reels
DCP020509P	DIP-14	010-1	-40°C to +85°C	DCP020509P	DCP020509P	Rails
DCP020509U ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP020509U	DCP020509U/1K	Tape and Reels
DCP021205P	DIP-14	010-1	-40°C to +85°C	DCP021205P	DCP021205P	Rails
DCP021205U ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP021205U	DCP021205U/1K	Tape and Reels
DCP021212P	DIP-14	010-1	-40°C to +85°C	DCP021212P	DCP021212P	Rails
DCP021515P	DIP-14	010-1	-40°C to +85°C	DCP021515P	DCP021515P	Rails
DCP022405P	DIP-14	010-1	-40°C to +85°C	DCP022405P	DCP022405P	Rails
Dual						
DCP020515DP	DIP-14	010-1	-40°C to +85°C	DCP020515DP	DCP020515DP	Rails
DCP020515DU ⁽²⁾	SOIC-28	217-2	-40°C to +85°C	DCP020515DU	DCP020515DU/1K	Tape and Reels
DCP021212DP	DIP-14	010-1	-40°C to +85°C	DCP021212DP	DCP021212DP	Rails
DCP022405DP	DIP-14	010-1	-40°C to +85°C	DCP022405DP	DCP022405DP	Rails
DCP022415DP	DIP-14	010-1	-40°C to +85°C	DCP022415DP	DCP022415DP	Rails

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DCP020503U/1K" will get a single 1000-piece Tape and Reel. (2) Shaded models available January, 2000.

TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ\text{C}$, unless otherwise noted.



FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP02 offers up to 2W of unregulated output power from a 5V, 12V, 15V, or 24V input source with a typical efficiency of up to 89%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design utilizes an advanced BiCMOS/DMOS process.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400kHz (divide by 2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide by 2 circuit. The oscillator can be synchronized to other DCP02 circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin LOW. The output pins will be tri-stated. This will occur in 2 μ s.

THERMAL SHUTDOWN

The DCP02 is protected by a thermal shutdown circuit. If the on-chip temperature exceeds 150°C, the device will shut down. Once the temperature falls below 150°C, normal operation will resume.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the variation in switching frequencies between the DC/DC converters.

The DCP02 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Significant stray capacitance (> 10pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit. It is also recommended that power and ground lines are star connected.

If synchronized devices are used, it should be noted that, at start up, all devices will draw maximum current simultaneously. This can cause the input voltage to dip and should it dip below the minimum input voltage (4.5V), the devices may not start up. A 2.2 μ F capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the SYNC pins are driven by an external device. Details are contained in a separate applications bulletin (AB-153).

CONSTRUCTION

The DCP02's basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP02 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. As there is no solder within the package, the DCP02 does not require any special PCB assembly processing. This results in an isolated DC/DC converter with inherently high reliability.

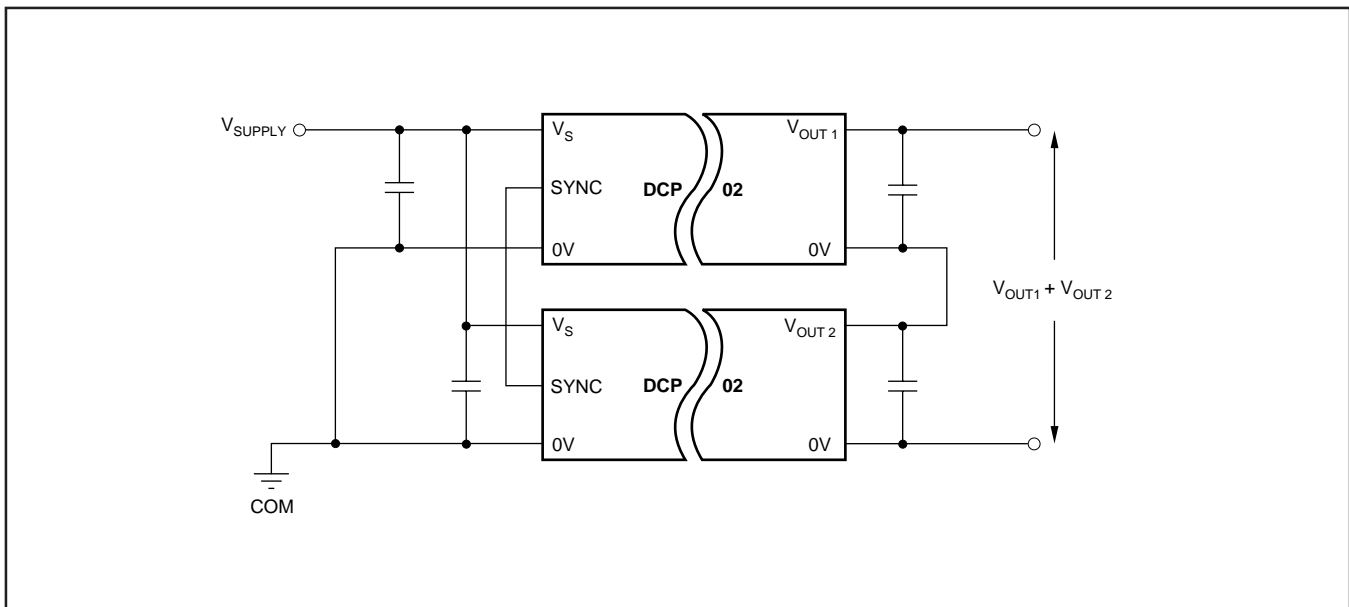


FIGURE 1. Connecting the DCP02 in Series.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP02 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2 μ s. Removal of the pull down will cause the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that a 1 μ F capacitor is used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2 μ F capacitor on the input is recommended.

Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide nonstandard voltage rails. This is possible by utilizing the floating outputs provided by the DCP02's galvanic isolation.

Connect the positive V_{OUT} from one DCP02 to the negative V_{OUT} (0V) of another (see Figure 1). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 will prevent beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, minimizing cost.

The outputs on dual output DCP02 versions can also be connected in series to provide two times the magnitude of V_{OUT} as shown in Figure 2. For example, a dual 15V DCP022415D could be connected to provide a 30V rail.

Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in Figure 3. Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

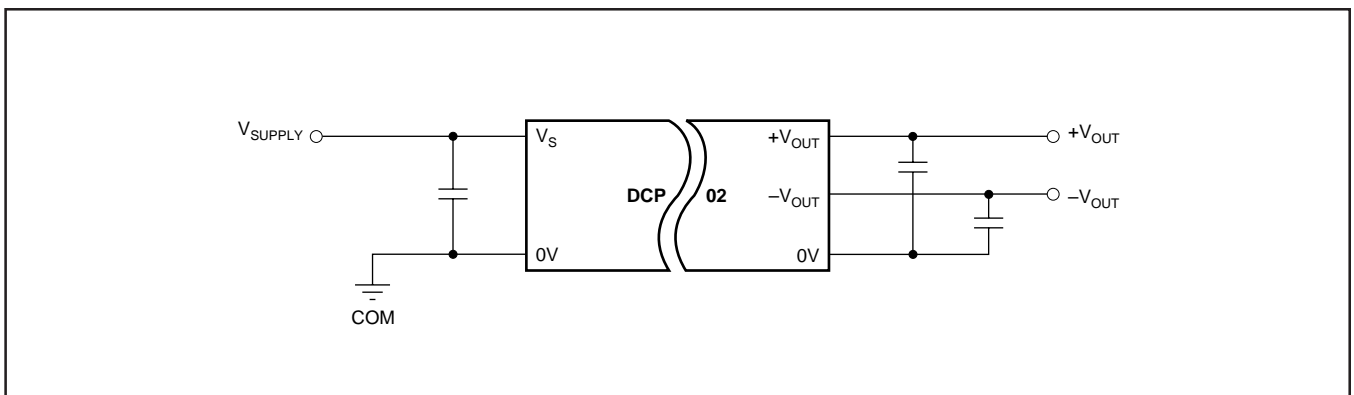


FIGURE 2. Connecting Dual Outputs in Series.

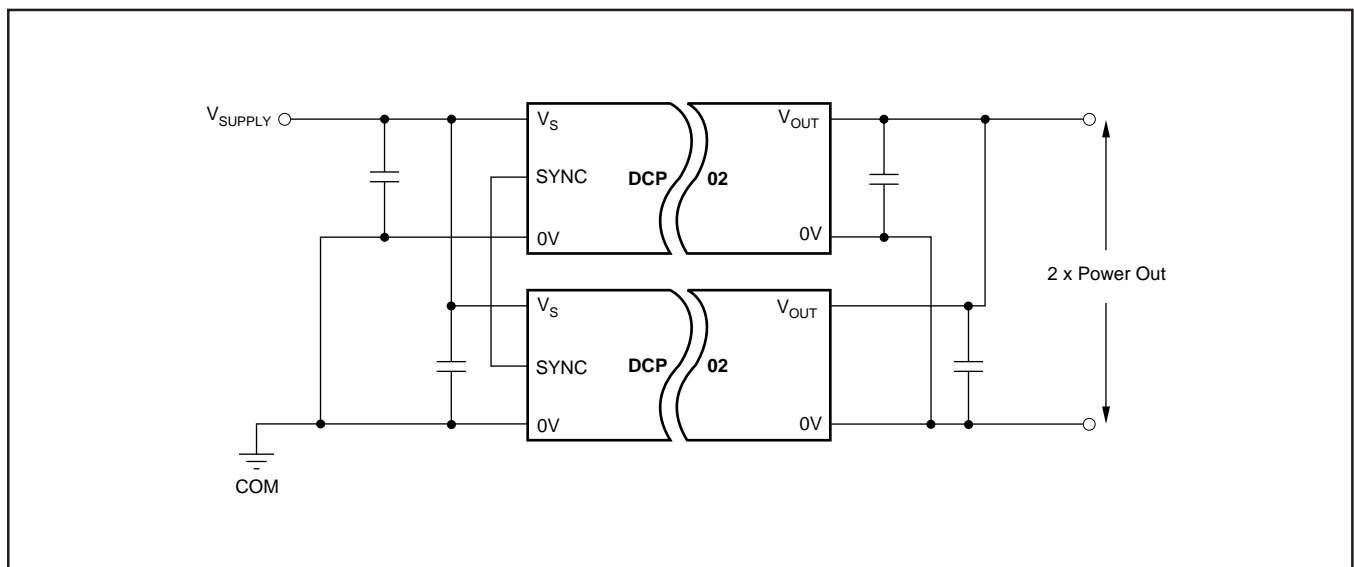


FIGURE 3. Connecting Multiple DCP02s in Parallel.

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