



## Low-Power, High-Speed CMOS Analog Switches

### FEATURES

- 44-V Supply Max Rating
- $\pm 15$ -V Analog Signal Range
- On-Resistance— $r_{DS(on)}$ : 20  $\Omega$
- Low Leakage— $I_{D(on)}$ : 40 pA
- Fast Switching— $t_{ON}$ : 100 ns
- Ultra Low Power Requirements— $P_D$ : 0.35  $\mu$ W
- TTL, CMOS Compatible
- Single Supply Capability

### BENEFITS

- Wide Dynamic Range
- Break-Before-Make Switching Action
- Simple Interfacing

### APPLICATIONS

- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

### DESCRIPTION

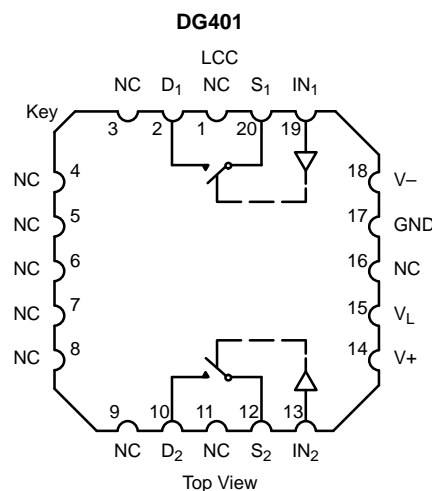
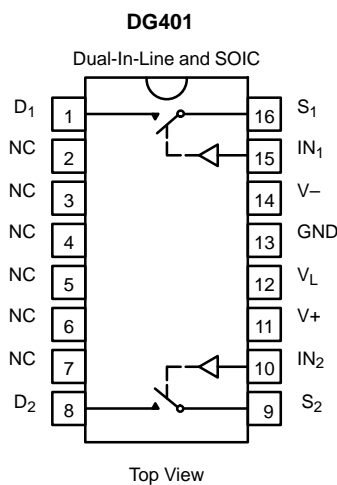
The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35  $\mu$ W, typ) with high speed ( $t_{ON}$ : 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full  $\pm 15$ -V analog range, rivaling JFET performance without the inherent dynamic range limitations.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

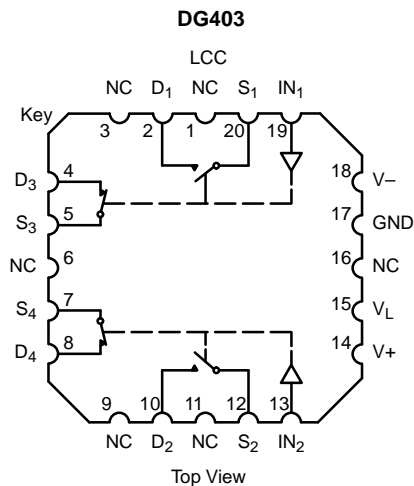
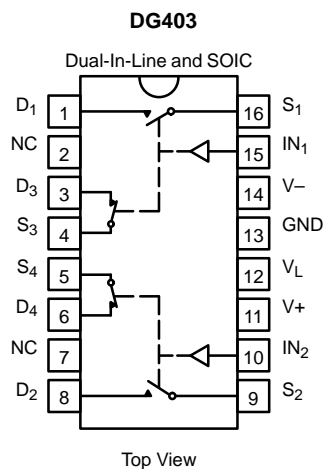


Two SPST Switches per Package

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

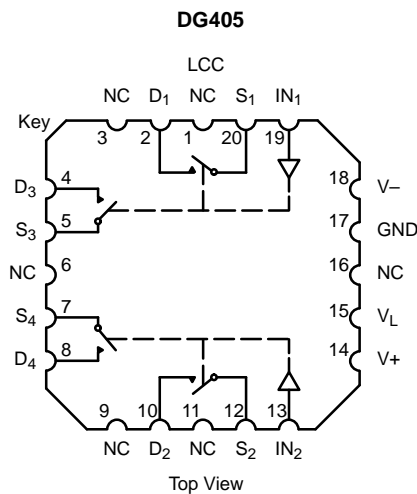
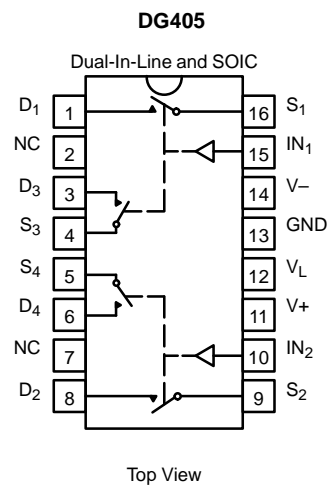
### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Two SPDT Switches per Package

TRUTH TABLE		
Logic	SW <sub>1</sub> , SW <sub>2</sub>	SW <sub>3</sub> , SW <sub>4</sub>
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V



Two DPST Switches per Package

TRUTH TABLE	
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.4 V



ORDERING INFORMATION		
Temp Range	Package	Part Number
<b>DG401</b>		
-40 to 85°C	16-Pin Plastic DIP	DG401DJ
-55 to 125°C	16-Pin CerDIP	DG401AK
		DG401AK/883, 5962-9056901MEA
	LCC-20	DG401AZ/883, 5962-9056901M2A
<b>DG403</b>		
-40 to 85°C	16-Pin Plastic DIP	DG403DJ
	16-Pin Narrow SOIC	DG403DY
-55 to 125°C	16-Pin CerDIP	DG403AK
		DG403AK/883, 5962-8976301MEA
	LCC-20	5962-8976301M2A
<b>DG405</b>		
-40 to 85°C	16-Pin Plastic DIP	DG405DJ
	16-Pin Narrow SOIC	DG405DY
-55 to 125°C	16-Pin CerDIP	DG405AK/883, 5962-8996101EA
	LCC-20	5962-89961012A

**ABSOLUTE MAXIMUM RATINGS**

V+ to V- ..... 44 V  
 GND to V- ..... 25 V  
 V<sub>L</sub> ..... (GND - 0.3 V) to (V+) +0.3 V  
 Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+ plus 2 V)  
 or 30 mA, whichever occurs first  
 Current (Any Terminal) Continuous ..... 30 mA  
 Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA  
 Storage Temperature (AK, AZ Suffix) ..... -65 to 150°C  
 (DJ, DY Suffix) ..... -65 to 125°C  
 Power Dissipation (Package)<sup>b</sup>  
 16-Pin Plastic DIP<sup>c</sup> ..... 450 mW  
 16-Pin CerDIP<sup>d</sup> ..... 900 mW  
 16-Pin SOIC<sup>e</sup> ..... 600 mW  
 LCC-20<sup>f</sup> ..... 900 mW

Notes:

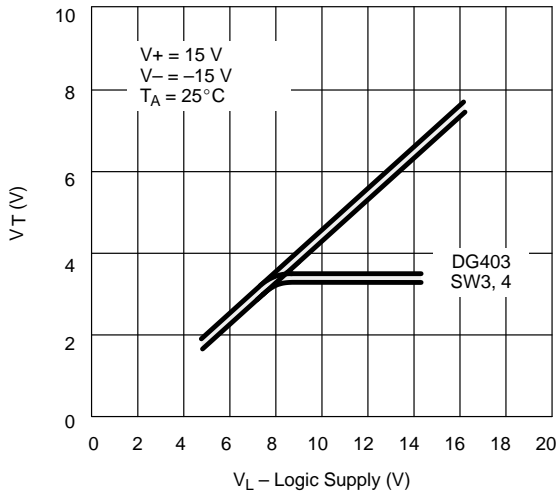
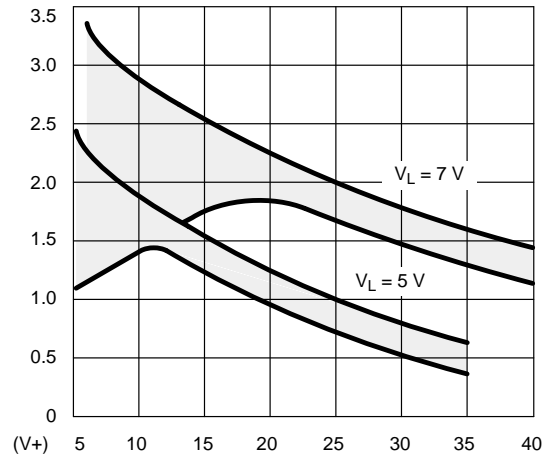
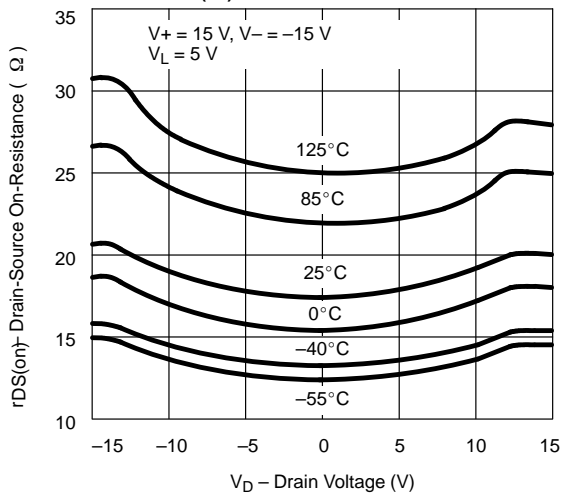
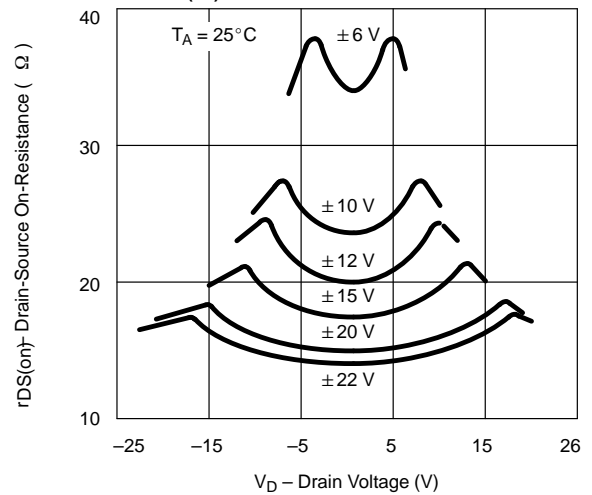
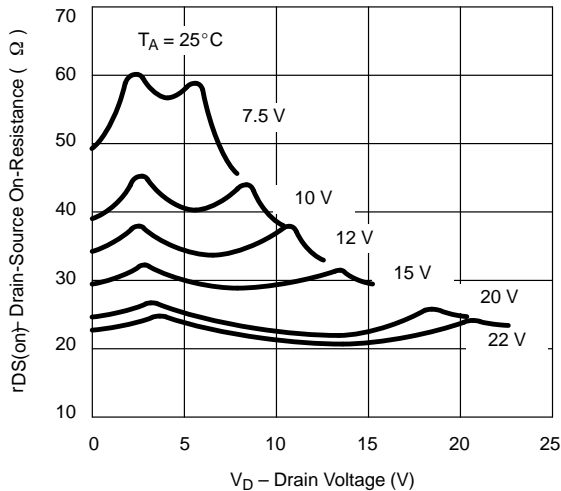
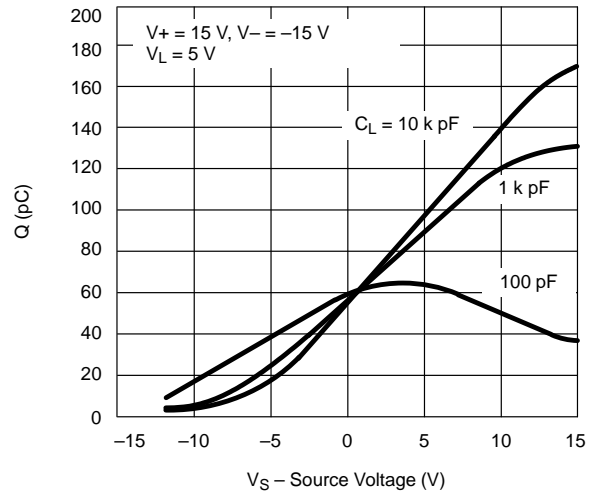
- a. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6 mW/°C above 75°C
- d. Derate 12 mW/°C above 75°C
- e. Derate 7.6 mW/°C above 75°C
- f. Derate 13 mW/°C above 75°C



SPECIFICATIONS <sup>a</sup>									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 10\text{ V}$ $V_+ = 13.5\text{ V}, V_- = -13.5\text{ V}$	Room Full	20		35 45		45 55	$\Omega$
$\Delta$ Drain-Source On-Resistance	$\Delta r_{DS(on)}$	$I_S = -10\text{ mA}, V_D = \pm 5\text{ V}, 0\text{ V}$ $V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$	Room Full	3		3 5		3 5	
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}, V_S = \mp 15.5\text{ V}$	Room Hot	-0.01	-0.25 -20	0.25 20	-0.5 -5	0.5 5	nA
	$I_{D(off)}$		Room Hot	-0.01	-0.25 -20	0.25 20	-0.5 -5	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	Room Hot	-0.04	-0.4 -40	0.4 40	-1 -10	1 10	
<b>Digital Control</b>									
Input Current $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = 0.8 V All Other = 2.4 V	Full	0.005	-1	1	-1	1	$\mu\text{A}$
Input Current $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = 2.4 V All Other = 0.8 V	Full	0.005	-1	1	-1	1	
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ See Figure 2	Room	100		150		150	ns
Turn-Off Time	$t_{OFF}$		Room	60		100		100	
Break-Before-Make Time Delay (DG403)	$t_D$	$R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	12	5		5		
Charge Injection	Q	$C_L = 10,000\text{ pF}$ $V_{gen} = 0\text{ V}, R_{gen} = 0\ \Omega$	Room	60					pC
Off Isolation Reject Ratio	OIRR	$R_L = 100\ \Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	Room	72					dB
Channel-to-Channel Crosstalk	$X_{TALK}$		Room	90					
Source Off Capacitance	$C_{S(off)}$	$f = 1\text{ MHz}, V_S = 0\text{ V}$	Room	12					pF
Drain Off Capacitance	$C_{D(off)}$		Room	12					
Channel On Capacitance	$C_D, C_{S(on)}$		Room	39					
<b>Power Supplies</b>									
Positive Supply Current	$I_+$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	Room Full	0.01		1 5		1 5	$\mu\text{A}$
Negative Supply Current	$I_-$		Room Full	-0.01	-1 -5		-1 -5		
Logic Supply Current	$I_L$		Room Full	0.01		1 5		1 5	
Ground Current	$I_{GND}$		Room Full	-0.01	-1 -5		-1 -5		

Notes:

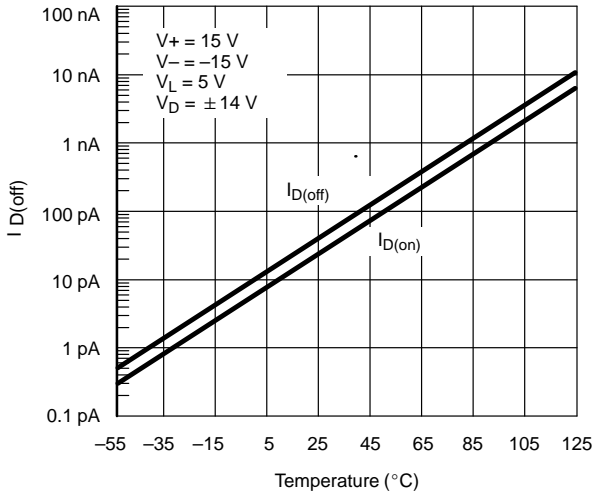
- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**
**Input Switching Threshold vs. Logic Supply Voltage**

**Input Switching Threshold vs. Supply Voltages**

 **$r_{DS(on)}$  vs.  $V_D$  and Temperature**

 **$r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltage**

 **$r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltage ( $V_{-} = 0\text{ V}$ )**

**Charge Injection vs. Analog Voltage**


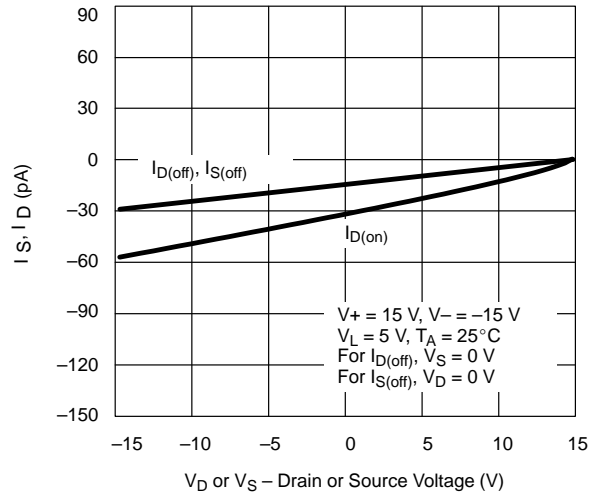


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

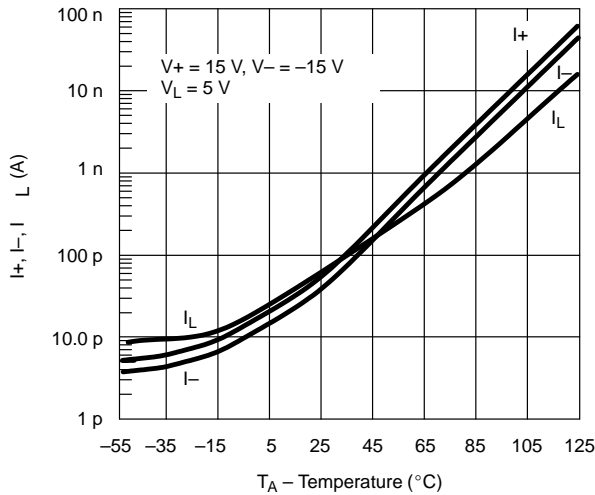
**Leakage Current vs. Temperature**



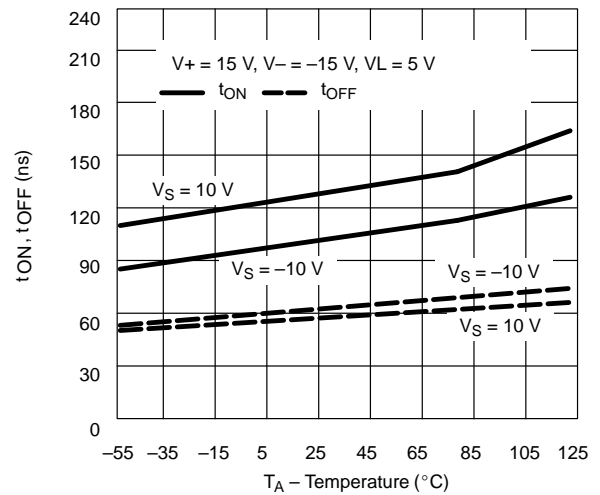
**Leakage Current vs. Analog Voltage**



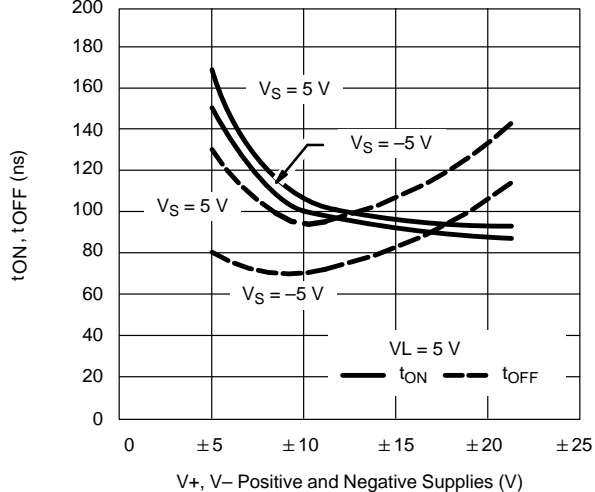
**Supply Current vs. Temperature**



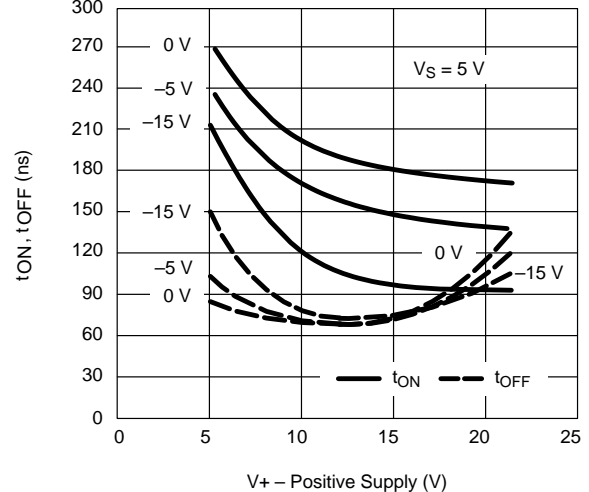
**Switching Time vs. Temperature\***



**Switching Time vs. Power Supply Voltage\***



**Switching Time vs. Positive Supply Voltage\***



\*Refer to Figure 2 for test conditions.

**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

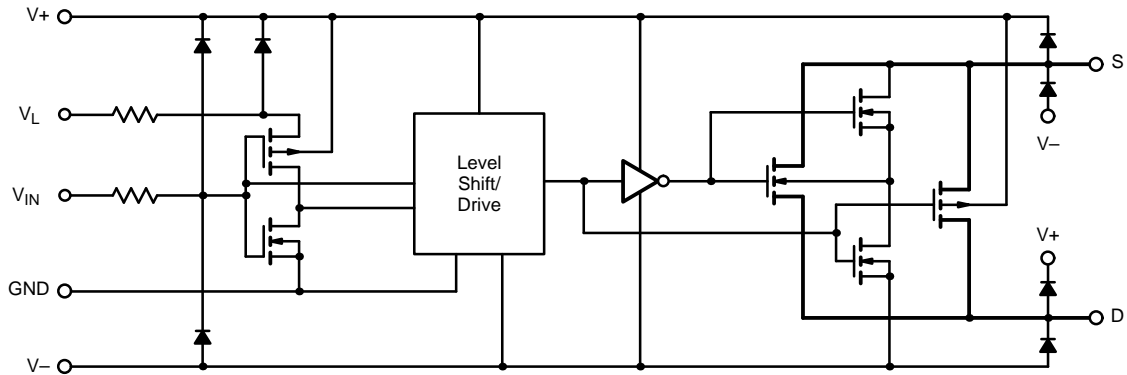
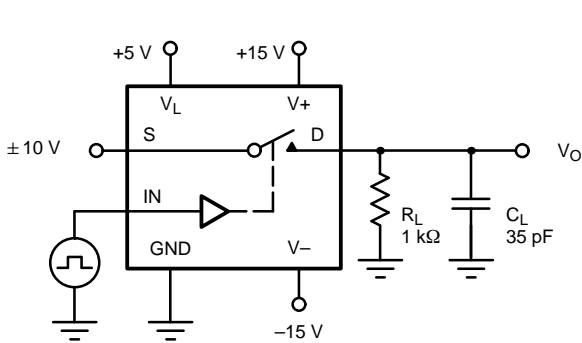


FIGURE 1.

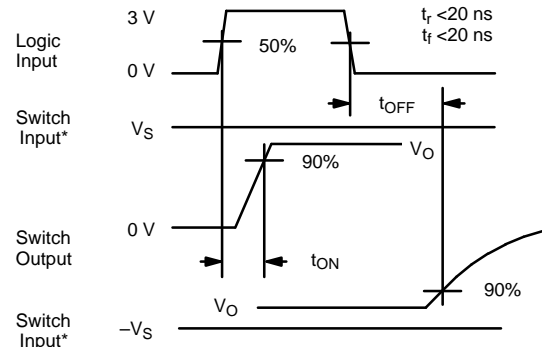
**TEST CIRCUITS**

$V_O$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



$C_L$  (includes fixture and stray capacitance)

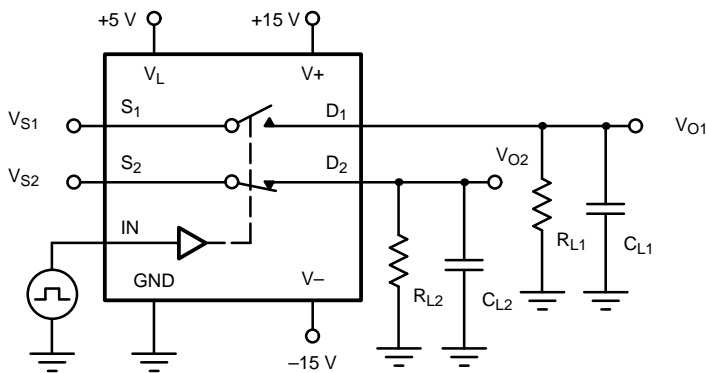
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



\* $V_S = 10\text{ V}$  for  $t_{ON}$ ,  $V_S = -10\text{ V}$  for  $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

FIGURE 2. Switching Time



$C_L$  (includes fixture and stray capacitance)

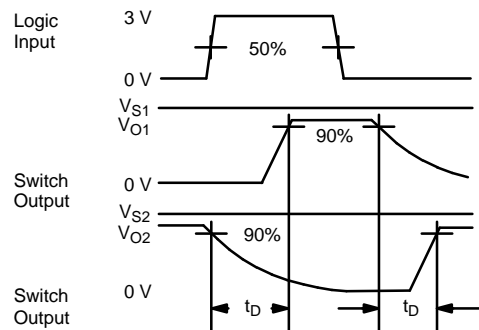


FIGURE 3. Break-Before-Make

**TEST CIRCUITS**

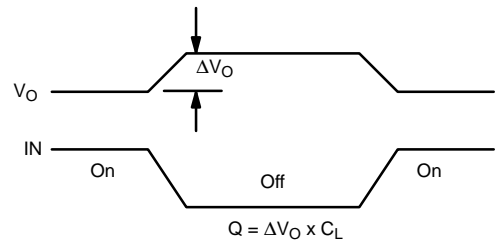
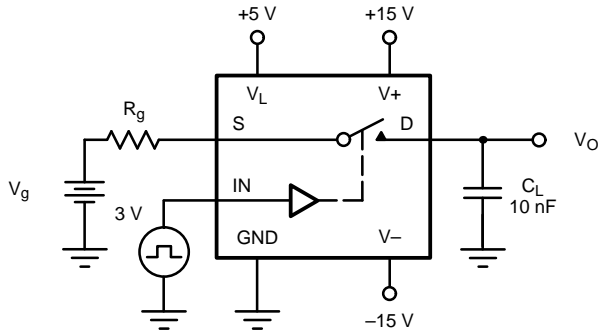


FIGURE 4. Charge Injection

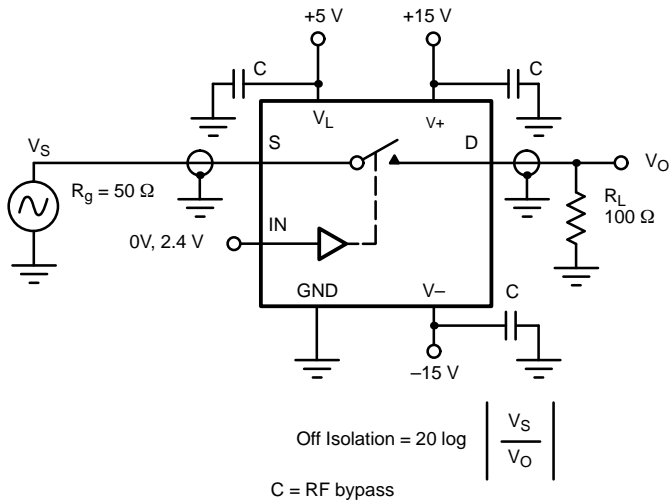


FIGURE 5. Off Isolation

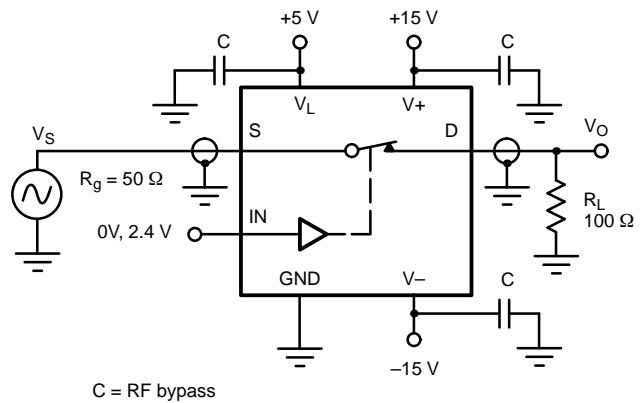


FIGURE 6. Insertion Loss

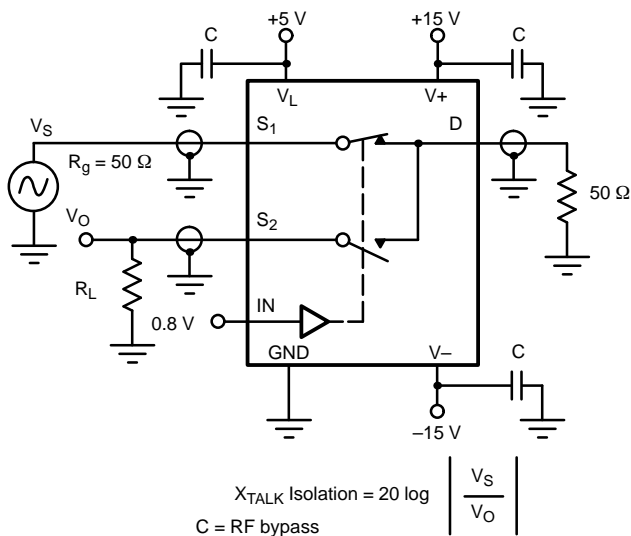


FIGURE 7. Crosstalk

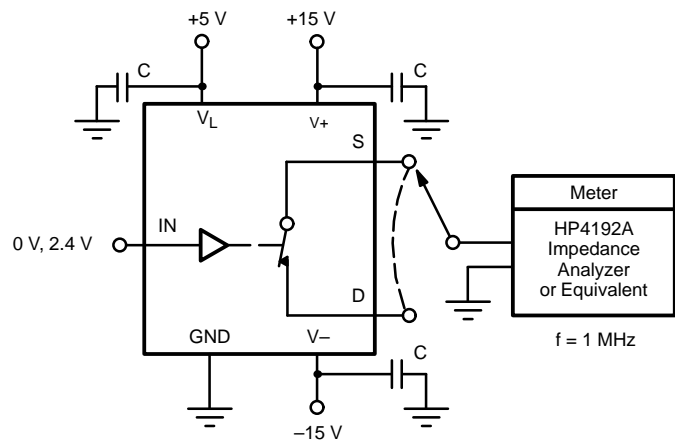
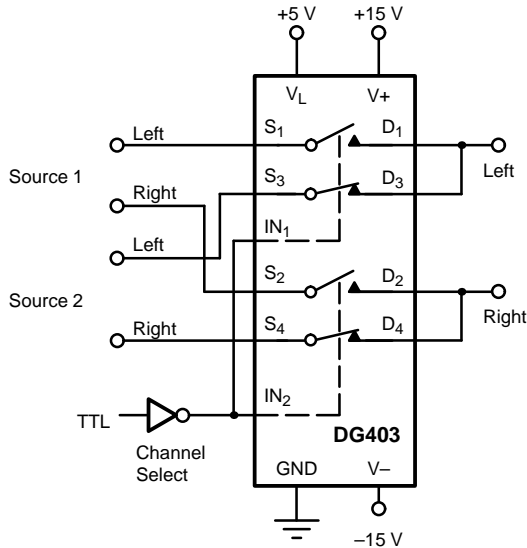
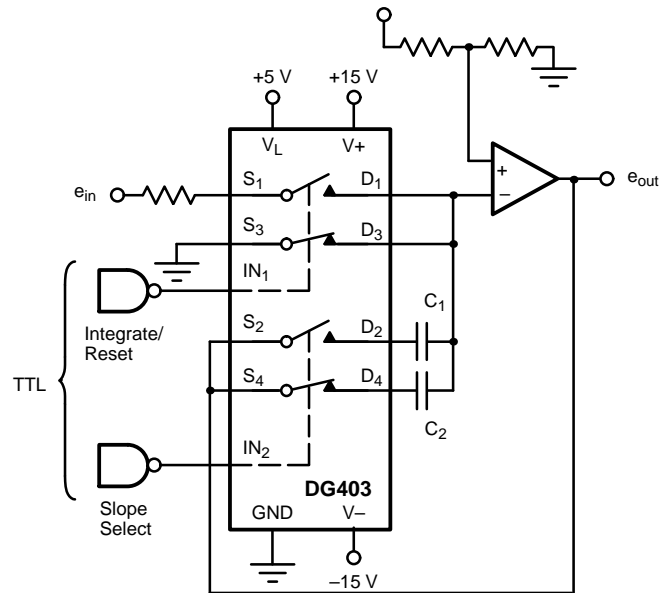


FIGURE 8. Capacitances

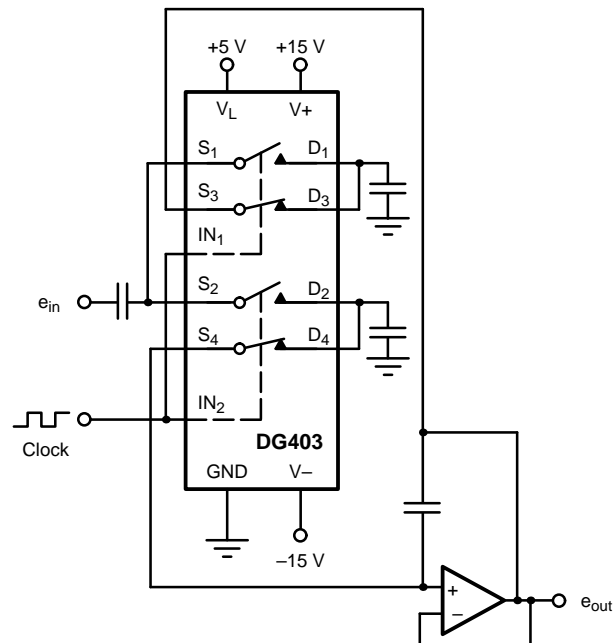
**APPLICATIONS**

**FIGURE 9.** Stereo Source Selector

**FIGURE 10.** Dual Slope Integrator

**Dual Slope Integrators:**

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor  $C_1$  or  $C_2$ . Another one selects  $e_{in}$  or discharges the capacitor in preparation for the next integration cycle.

**Band-Pass Switched Capacitor Filter:**

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.


**FIGURE 11.** Band-Pass Switched Capacitor Filter

**APPLICATIONS**

**Peak Detector:**

$A_3$  acting as a comparator provides the logic drive for operating  $SW_1$ . The output of  $A_2$  is fed back to  $A_3$  and compared to the analog input  $e_{in}$ . If  $e_{in} > e_{out}$  the output of  $A_3$  is high keeping  $SW_1$  closed. This allows  $C_1$  to charge up to the analog input

voltage. When  $e_{in}$  goes below  $e_{out}$   $A_3$  goes negative, turning  $SW_1$  off. The system will therefore store the most positive analog input experienced.

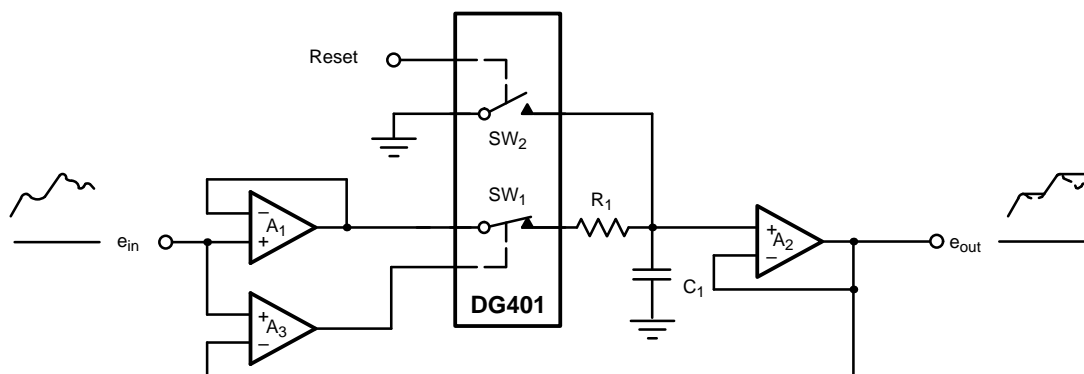


FIGURE 12. Positive Peak Detector



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